3.3.2 Number of research papers published per teacher in the Journals notified on UGC CARE list during the year (2022-2023)

S.NO	Title of paper	Name of the author/s	Department of the teacher	Name of journal	Calendar Year of publication	ISSN number	Link to the recognition in UGC enlistment of the Journal
1	Implementation Of Turbo Decoder For Completing Communication System In IVS	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/8a3b67e10c6fc691e1c0289ca5ecfc57.pdf
2	Implementation Of Cryptography Using Rom Sub Modules And Exclusion Of Shift Rows	Mr.G Srinivas	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/2f398b5805cb6ea287e8d8443233c0aa.pdf
3	Design Of Power Efficient 12T Sram Using Adiabatic Technique For Charge Recovery Application	Mr.G Srinivas	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/983ee5cf84da147528889fa827d21684.pdf
4	Design Of High Order Compression Multiplier For High-Speed DSP Applications	Mr.E Nagesh	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/7b16b0bbce76748afcf36e09601eb150.pdf
5	Design Of High-Speed Area Efficient Mac Unit Using Reversible Logic	Mr.V Guravaiah	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/16da2de01af4a657d6e2687390e41a9d.pdf
6	Improvement Of Memory Data Corrections By Using CRC Technique For Fault Torrent Applications	Mr.B Dasharadha	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/8a4b7adf2386f7d733f91293cbc1e701.pdf
7	Deign Of Multi Data Functional Based Fipflop For High-Speed Data Communication System	Mr.D Suryaprakesh	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/c1e54908047176d5d111bbe0618d4997.pdf
8	Efficient Design for Fixed-Width Adder-Tree	Mr.P.Vijnatha Raju	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/7f251919893764d45daea8930dca9c95.pdf

9	Design of Power and Area Efficient Approximate Multipliers	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/1bb6264d69c7d8eb5fd8851286ebfc3f.pdf
10	Implementation of SRAM Based Error Correction and Detection in Memory System Using LFSR	Mr.V.Nagaraju	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/downloads/view/5/14
11	The Design of Low-Power And High-Speed Full Adder through the exploration of novel XOR and XNOR	Mr.V.Nagaraju	ECE	Industrial Engineering Journal	2022-23	0970-2555	http://www.journal-iiie-india.com/1_july_23/61_online.pdf
12	Design Of Compression Tree Based Wallace tree multiplifier for high speed VLSI application	Mr.G Srinivas	ECE	Industrial Engineering Journal	2022-23	0970-2555	http://www.journal-iiie-india.com/1_july_23/60_online.pdf
13	An Advanced VLSI Architecture For A Three-Operand binary adder for both high speed and area efficient	Mr.P.Vijnatha Raju	ECE	Industrial Engineering Journal	2022-23	0970-2555	http://www.journal-iiie-india.com/1_july_23/59_online.pdf
14	Implementation Of Cryptography Using Rom Sub Modules And Exclusion Of Shift Rows	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/2f398b5805cb6ea287e8d8443233c0aa.pdf
15	Design Of Power Efficient 12T Sram Using Adiabatic Technique For Charge Recovery Application	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/983ee5cf84da147528889fa827d21684.pdf
16	Design Of High Order Compression Multiplier For High-Speed DSP Applications	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/7b16b0bbce76748afcf36e09601eb150.pdf
17	Design Of High-Speed Area Efficient Mac Unit Using Reversible Logic	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/16da2de01af4a657d6e2687390e41a9d.pdf
18	Improvement Of Memory Data Corrections By Using CRC Technique For Fault Torrent Applications	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/8a4b7adf2386f7d733f91293cbc1e701.pdf
19	Deign Of Multi Data Functional Based Fipflop For High-Speed Data Communication System	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/c1e54908047176d5d111bbe0618d4997.pdf

20	Efficient Design for Fixed-Width Adder-Tree	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/7f251919893764d45daea8930dca9c95.pdf
21	Implementation of SRAM Based Error Correction and Detection in Memory System Using LFSR	Dr.S. Kishore Reddy	ECE	International Journal of Engineering Innovations in Advanced Technology	2022-23	2582-1431	https://www.ijeiat.com/images/sliders/d1f407a7dd80af0150ec2070e063e2e0.pdf
22	The Design of Low-Power And High-Speed Full Adder through the exploration of novel XOR and XNOR	Dr.S. Kishore Reddy	ECE	Industrial Engineering Journal	2022-23	0970-2555	http://www.journal-iiie-india.com/1_july_23/61_online.pdf
23	Design Of Compression Tree Based Wallace tree multiplifier for high speed VLSI application	Dr.S. Kishore Reddy	ECE	Industrial Engineering Journal	2022-23	0970-2555	http://www.journal-iiie-india.com/1_july_23/60_online.pdf
24	An Advanced VLSI Architecture For A Three-Operand binary adder for both high speed and area efficient	Dr.S. Kishore Reddy	ECE	Industrial Engineering Journal	2022-23	0970-2555	http://www.journal-iiie-india.com/1_july_23/59_online.pdf
25	Bidirectional Power Control Strategy for Super Capacitor Energy Storage System Based on MMC DC-DC Converter	Mr.M.SHANKAR	EEE	The International journal of analytical and experimental modal analysis	2022-23	0886-9367	https://drive.google.com/file/d/1WsLOUbgF9eeH3P2cE8JG4l0pVsXb8sIT/view
26	DESIGN AND SIMULATION OF MPC WITH FLC BASED HYBRID SYSTEM	Mr.T.KRANTI KUMAR	EEE	The International journal of analytical and experimental modal analysis	2022-23	0886-9367	https://drive.google.com/file/d/1Iz0UucKlHx_m5nFVTSjcwQdyo8ETEK0x/view
27	Applying Hidden Markow Models to Ontology Based IRS for Coherence	Dr. SHAHEBAZ AHMED KHAN	CSE	Journal of Information and Computational Science	2022-23	1548-7741	https://drive.google.com/file/d/1nZYyTTSQMoEjKiuFzNjhfRn2kD5E_me2/view
28	An Improved Fast and Secure CAMEL Based Authenticated Key in Smart Health Care System	Dr.Shaik Shakeer Basha	CSE	UNIVERSAL WISER PUBLISHER	2022-23	http://ojs.wiserpub.com/index.php(SCOPUS INDEXED)	https://ojs.wiserpub.com/index.php/CCDS/article/view/1423/972
29	Optimized Robot Process Automated Path Navigation InTime Varying Networks	Dr.Shaik Shakeer Basha	CSE	Journal of Jilin University (Engineering and Technology Edition)	2022-23	1671-5497	https://jilindaxuexuebao.net/details.php?id=DOI:10.17605/OSF.IO/WX4CV
30	CONCEPTUAL PAPER WORK ON PAY STRUCTURE	Dr.Y.JAYAPRADHA	MBA	JOURNAL OF MANAGEMENT AND ENTREPRENEURSHIP	2022-23	2229-5348	https://xime.org/jme/php/journal.php?bookid=30type=0

31	SUCCESS OF SKILL BASED PAY PLANS	Dr.Y.JAYAPRADHA	MBA	ShodhaSamhita: Journal of Fundamental & Comparative Research	2022-23	2277-7067	https://kksushodhasamhita.org/index.php/sdsa/issue/view/5
32	COMPENSATION MANAGEMENT	Dr.Y.JAYAPRADHA	MBA	International Journal of Early Childhood Special Education (INT-JECSE)	2022-23	1308-5581	https://www.int-jecse.net/article/COMPENSATION+MANAGEMENT_4972/
33	Compensation Reward Management	Dr.Y.JAYAPRADHA	MBA	WEBOLOGY	2022-23	1735-188X	https://www.webology.org/abstract.php?id=4561
34	FUZZY LOGIC CONTROLLER BASED DVR TO COMPENSATE VOLTAGE SAG AND SWELL WITH SRF	Ms.M.RAGINI	EEE	The International journal of analytical and experimental modal analysis	2022-23	0886-9367	https://drive.google.com/file/d/1CwPf5_u7SNaTys4ty4oA-ZH3CqvGHHlO/view
35	A NOVEL BI-DIRECTIONAL EV HYBRID ENERGY STORAGE FOR V2G SYSTEM	Mrs.E.PRASANNA	EEE	Journal of Interdisciplinary Cycle Research	2022-23	0022-1945	https://drive.google.com/file/d/12qPy3Nxdy2sRhfHJFCW4rBLM4-4z5T8w/view
36	A NOVEL PID CONTROLLER BASED D-STATCOM FOR ENHANCING POWER QUALITY WITH PR-FB CONTROLLER	Mr.T.KRANTI KUMAR	EEE	Journal of Interdisciplinary Cycle Research	2022-23	0022-1945	https://drive.google.com/file/d/1aXZH7ZC00ZBiuLVD2Twad_KBGD2gF1Xp/view
37	EXPERIMENTATION AND ANALYSIS OF NATURAL FIBER REINFORCED POLYMER MATRIX COMPOSITE	Dr Ramesh Babu Yeluri	MECH	International Journal of Mechanical Engineering	2022-23	0974-5823	https://www.kalaharijournals.com/resources/MAY_198.pdf
38	EXPERIMENTATION AND ANALYSIS OF NATURAL FIBER REINFORCED POLYMER MATRIX COMPOSITE	Mr.Kolla Sumanth	MECH	International Journal of Mechanical Engineering	2022-23	0974-5823	https://www.kalaharijournals.com/resources/MAY_198.pdf
39	EXPERIMENTATION AND ANALYSIS OF NATURAL FIBER REINFORCED POLYMER MATRIX COMPOSITE	Mr.Mallikanti Venkateswarlu	MECH	International Journal of Mechanical Engineering	2022-23	0974-5823	https://www.kalaharijournals.com/resources/MAY_198.pdf
40	EXPERIMENTATION AND ANALYSIS OF NATURAL FIBER REINFORCED POLYMER MATRIX COMPOSITE	Mr.G Vinod Kumar	MECH	International Journal of Mechanical Engineering	2022-23	0974-5823	https://www.kalaharijournals.com/resources/MAY_198.pdf
41	INVESTIGATION AND CHARACTERIZATION OF GRAPHITE BASED CARBON REINFORCED LAMINATES	Dr. RAMESH BABU YELURI	MECH	International Journal of Research in Engineering and Applied Sciences(IJREAS)	2022-23	2249-3905	https://euroasiapub.org/wp-content/uploads/IJREA3SOct22-RamB.pdf

42	INVESTIGATION AND CHARACTERIZATION OF GRAPHITE BASED CARBON REINFORCED LAMINATES	Mr.Mallikanti Venkateswarlu	MECH	International Journal of Research in Engineering and Applied Sciences(IJREAS)	2022-23	2249-3905	https://euroasiapub.org/wp-content/uploads/IJREA3SOct22-RamB.pdf
43	INVESTIGATION AND CHARACTERIZATION OF GRAPHITE BASED CARBON REINFORCED LAMINATES	Mr.G.VINOD KUMAR	MECH	International Journal of Research in Engineering and Applied Sciences(IJREAS)	2022-23	2249-3905	https://euroasiapub.org/wp-content/uploads/IJREA3SOct22-RamB.pdf
44	12T MEMORY CELLFORAEROSPACEAPPLICATIONS IN NANO SCALE CMOS TECHNOLOGY	Dr.S. Kishore Reddy	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50380&ctype=a
45	12T MEMORY CELLFORAEROSPACEAPPLICATIONS IN NANO SCALE CMOS TECHNOLOGY	Dr G Chandra Shekar	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50380&ctype=a
46	OVERLOADED CDMA CROSSBAR FOR NETWORK-ON- CHIP	Dr.S. Kishore Reddy	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50379&ctype=a
47	OVERLOADED CDMA CROSSBAR FOR NETWORK-ON- CHIP	Mr.D.SuryaPrakesh,	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50379&ctype=a
48	VLSI DESIGN FOR CONVOLUTIVE BLIND SOURCE SEPARATION	Dr.S.Kishore Reddy	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50388&ctype=a
49	VLSI DESIGN FOR CONVOLUTIVE BLIND SOURCE SEPARATION	Dr.Siddhartha Bangaru	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50388&ctype=a
50	Design And Implementation Of Low Power, Area And High Performance 4 Bit Sequence Digital Counter	Dr.S.Kishore Reddy	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50391&ctype=a
51	Design And Implementation Of Low Power, Area And High Performance 4 Bit Sequence Digital Counter	Mr.Vasantha Nagaraju	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50391&ctype=a
52	Design And Implementation Of High Speed Low Power Mux Based Full Adder Using 16nm Technology	Dr.S.Kishore Reddy	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50392&ctype=a

53	Design And Implementation Of High Speed Low Power Mux Based Full Adder Using 16nm Technology	Mr.P.Vijnatha Raju	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50392&ctype=a
54	mplementation Of Weighted Pseudorandom Test Pattern Generator for a Built In Self Test Architecture	Dr.S.Kishore Reddy	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50393&ctype=a
55	mplementation Of Weighted Pseudorandom Test Pattern Generator for a Built In Self Test Architecture	Mr.S.Sagar	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50393&ctype=a
56	Rounding Based Approximate Multiplier For High Speed Yet Energy EfficientDSP Applications	Dr.S.Kishore Reddy	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50394&ctype=a
57	Rounding Based Approximate Multiplier For High Speed Yet Energy EfficientDSP Applications	Dr.Vankayalapati Naga Raju	ECE	Organization Development Journal(ODJ)(SCOPUS INDEX JOURNAL)	2022-23	0889-6402	http://www.journalodj.com/article_view.php?id=50394&ctype=a
58	AN EFFICIENT VLSI ARCHITECTURE TO REMOVE IMPULSE NOISE IN IMAGES USING DECISION	Dr.S.Kishore Reddy	ECE	Journal of Engineering Sciences	2022-23	0377-9254	https://jespublication.com/uploads/2023-V14I10059.pdf
59	AN EFFICIENT VLSI ARCHITECTURE TO REMOVE IMPULSE NOISE IN IMAGES USING DECISION	Mr.G Srinivas	ECE	Journal of Engineering Sciences	2022-23	0377-9254	https://jespublication.com/uploads/2023-V14I10059.pdf

A NOVEL BI-DIRECTIONAL EV HYBRID ENERGY STORAGE FOR V2G SYSTEM

BOMMAKANTI MOUNIKA[1]| E.PRASANNA[2]

[1]PG SCHOLAR, Dept of. ELECTRICAL POWER SYSTEM, Avanthi Institute of Engineering and Technology, Ts, India.

[2]ASSISTANT PROFESSOR, Dept of Electrical and Electronics Engineering, Avanthi Institute of Engineering and Technology, Ts, India.

ABSTRACT: This paper gives a switching bi-directional buck-boost converter (SBBBC) for vehicles- to-grid (V2G) machine. The topology can offer a power bi-directional current route for power alternate among the Li-battery/super capacitor (SC) hybrid power garage machine (HESS) of the electrical automobile and the grid. This topology now no longer best has greenback-enhance capability, however additionally has the feature of power management. In this paper, the country-area averaging approach is used to research the steadiness of the topology in enhance and greenback modes. The manage method is given in line with the state of charge (SOC) of the power garage machine to make certain that the output voltage and current are stable. And the Li-battery is charged in constant current (CC) and constant voltage (CV) mode. The voltage and current controllers are designed within side the frequency area primarily based totally on bode plots. Finally, the electric feasibility of the topology, the suitability of the layout controller and manage method are tested with the aid of using simulation.

KEYWORDS:

Vehicles- to-grid (V2G), SBBBC, State of charge, CC, CV.

I.INTRODUCTION: Electric vehicles have been widely used because of their cleanliness and low impact on the environment [1]. Li-batteries are of critical importance part in energy storage systems of electric vehicle [2]. Although Li-batteries with high energy densities can provide enough energy during steady-state operation, the power densities of Li-batteries are too low to meet the peak power demand [3], [4]. Combining Li-batteries and super-capacitors (SC) to form a hybrid energy storage system (HESS) can solve the problem. The reason is that SC with higher power densities can provide the transient power required by the load [5][17]. Since output voltage peak of the voltage source inverter is less than the dc-link side voltage, it is necessary to use the dc-dc converter to raise the Li-battery voltage [18]. Figure 1 shows the block diagram of HESS. The SC is directly connected to the inverter, which can increase the dynamic response of the HESS during transient peak power demand, while the Li-battery is connected to the DC-link by a bi-directional DC/DC converter [19]. The effect of the bi-directional dc-dc converter in the HESS is to transformer the energy and keeps the dc bus voltage stability. More- over, the converter should

provide bi-directional power flow because the energy storage system and the grid require energy exchange [20].

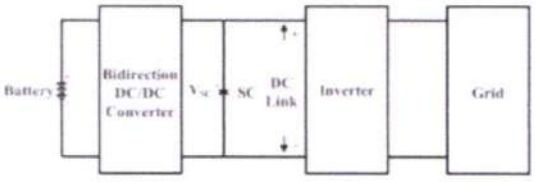


FIGURE 1. The block diagram of HESS.

AHESS topology is mentioned in articles [3] and [5]. In the topology of [3] and [5], the Li-battery can be connected to the SC via a bi-directional dc-dc half-bridge or directly to the DC bus via a diode. This two-stage converter can make full use of the power capacity of the SC but the boost ratio is low. A buck-boost converter for a plug-in hybrid electric vehicle is proposed in paper [21] and [22], respectively. However, the converter mentioned in the paper [21] cannot achieve a bi- directional flow of energy between the grid and the energy storage device. The converter mentioned in the paper [22] has many switching devices, large losses and complicated control. A high voltage gain bi-directional dc-dc converter is given in article [23]. This topology can operate under zero voltage switching conditions and reduces switching and conduction losses. However, this topology has many switching states and the operation is complicated. In [13] and [24], hybrid energy storage systems for electric vehicles based on Z-source inverters (ZSI) and quasi-Z-source inverters (qZSI) were proposed. These two topologies have the boost capability, and provide a bi-directional energy flow path. Moreover, the reliability of the hybrid energy storage system is enhanced due to the characteristics that allow the inverter to shoot-through. These two topologies can increase power density [25]. The control strategies proposed in [13] and [24] is complex, and the topologies have multiple passive components between the SC and the DC bus, which will greatly increase the size of the device.

II.PROPOSED SYSTEM: This paper proposes a switching bi-directional buck-boost converter (SBBBC) and its appropriate control strategy, which is used in the HESS for vehicles-to-grid (V2G) system. The converter allows shoot-through of two switches of any phase, with anti-electromagnetic interference capability. Meanwhile, since there are three switches in the DC side, the SC and Li-battery can fulfill bi-directional power flow. Furthermore, the small-signal model of the topology is established by state space averaging method and the stability of the system is analyzed. The control strategy is given according to the state of charge (SOC) of the energy storage system and the operating state of the circuit. The performance of the proposed converter and control strategy are verified through simulation results.

A. PROPOSED TOPOLOGY

Figure 2 shows the proposed SBBBC with HESS, which consists of five parts: Li-battery, switching bi-directional buck-boost circuit, SC, full bridge inverter and gird. The switching bi-directional buck-boost circuit has an inductor, a SC and the additional three switches (SD1, SD2, SD3). Since the gate signals of switches SD2 and SD3 are the same and complementary to the gate signal of switch SD1, one gate signal can control these three additional switches. This

unique SBBBC network allows the system works on the buck and boost modes, and it can provide bi-directional powerflow.

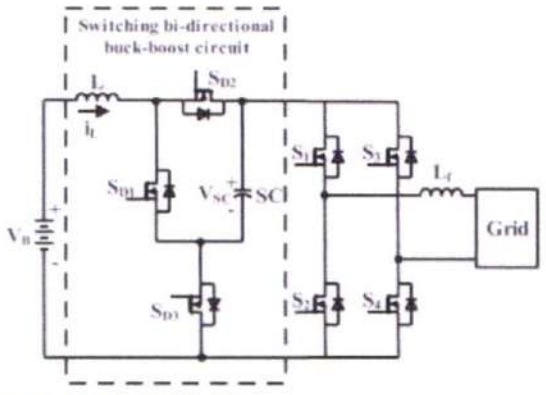


FIGURE 2. The proposed SBBBC.

TABLE 1. Switch combination and inverter output voltage.

N	U_{SC}	S_{B1},S_{B2},S_{B3}	S_1,S_3	S_2,S_4	state
1	0	0 1 1	0 0	1 1	zero state
2	0	0 1 1	1 1	0 0	zero state
3	$-U_{SC}$	0 1 1	0 1	1 0	active state
4	U_{SC}	0 1 1	1 0	0 1	active state
5	0	1 0 0	1 1	X X	shoot-through state
6	0	1 0 0	X X	1 1	shoot-through state

Note:X is 0 or 1.

B. MODULATION METHOD

In the proposed converter, there are three switching-states include active state, zero state and shoot-through state respectively, as shown in Table 1. All switches of full bridge inverter are operated in the SPWM mode to modulate output volt- age. The switching bi-directional buck-boost circuit uses the shoot-through duty to achieve buck-boost voltage. The duty cycle is calculated by:

$$\begin{cases} d = m\sin(\theta) \\ d_s = const \qquad (d_s \le 1-d) \\ d_0 = 1-d-d_s \end{cases} \tag{1}$$

Where m is the modulation index of the inverter; Θ is the vector angle of the output voltage; d, ds, d0 are the duty cycles of the output voltage active state, shoot-through state and zero voltage state, respectively.

III. MODELING AND ANALYSIS OF THE PROPOSE CONVERTER

The proposed converter can provide bi-directional power flow among SC, Li-battery and grid, as shown in Figure 2. And the converter can work in boost mode and buck mode.

A. BOOST MODE:

During boost mode, the proposed converter boosts the low Li- battery voltage to high dc-link voltage. There are three work states: zero state, active state and shoot-through state.

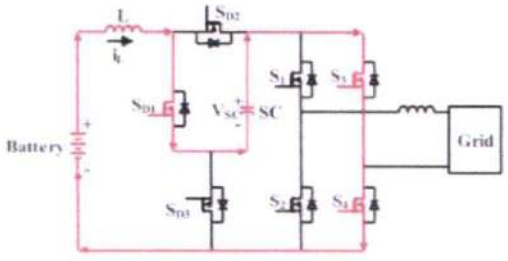


FIGURE 3. Flow path in shoot-through state of boost mode.

1) SHOOT-THROUGH STATE

In shoot-through state, the switches SD1 and S3 &S4 (S1 &S2) are turned ON while switches SD2 and SD3 are simultaneously turned OFF, as shown in Figure 3. In this state, the power is transferred from the Li-battery and SC to the inductor L. The state equation is given by:

$$\begin{cases} L\dfrac{di_L}{dt} = -(R_L + R_C)i_L + V_{SC} + V_B \\ C\dfrac{dV_{SC}}{dt} = -i_L \end{cases} \tag{2}$$

Where VB is the Li-battery voltage; VSC is the SC voltage; IL is the current through the inductor L; RL and RC are parasitic resistances of the inductor L and SC, respectively.

2) ACTIVE STATE

In active state, both switches SD2 and SD3 are turned ON while switches SD1 is

PRINCIPAL
Avanthi Institute of Engg. & Tech.
Gunthapally (V), Abdullapurmet (Mdl.), R.R. Dist.

simultaneously turned OFF, as shown in Figure 4. In this state, the Li-battery VB and inductor L charge SC and power is transferred from the Li-battery VB and inductor L to the grid. The state equation can be calculated as follows:

$$\begin{cases} L\dfrac{di_L}{dt} = -(R_L + R_C)i_L - V_{SC} + V_B + R_C i_O \\ C\dfrac{dV_{SC}}{dt} = i_L - i_O \end{cases} \quad (3)$$

where i_O is the output current.

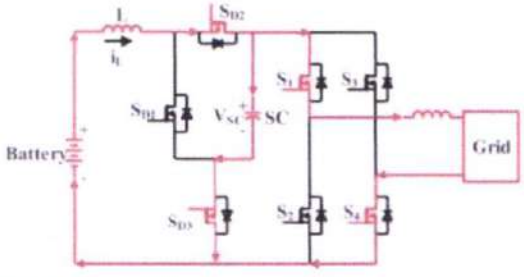


FIGURE 4. Flow path in active state of boost mode.

3) ZERO STATE

In zero state, both switches SD2 and SD3 and S1 & S3 (S2 &S4) are turned ON while switches SD1 is simultaneously turned OFF, as shown in Figure 5. The state equation can be calculated as follows.

$$\begin{cases} L\dfrac{di_L}{dt} = -(R_L + R_C)i_L - V_{SC} + V_B \\ C\dfrac{dV_{SC}}{dt} = i_L \end{cases} \quad (4)$$

From equations (2) to (4), due to the average value of the inductor voltage and the capacitor current should be zero in one switching period of Ts, the voltage gain and current gain of the proposed converter in boost mode are as follows [26]:

$$\frac{V_{SC}}{V_B} = \frac{(1 - 2D_{boost})Z_H}{(1 - 2D_{boost})^2 Z_H + (2D_{boost}R_C + R_L)m} \quad (5)$$

$$i_L = \frac{m}{1 - 2D_{boost}} i_O \quad (6)$$

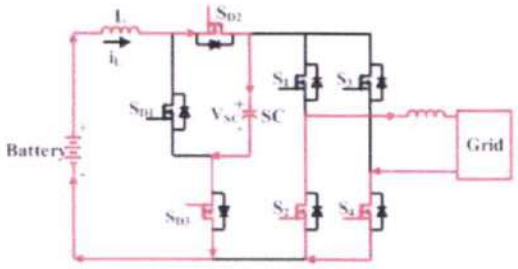


FIGURE 5. Flow path in zero state of boost mode.

IV.SIMULATION RESULTS

The SBBBC was simulated to verify the feasibility and dynamic performance. The simulation parameters are shown in Table 2.

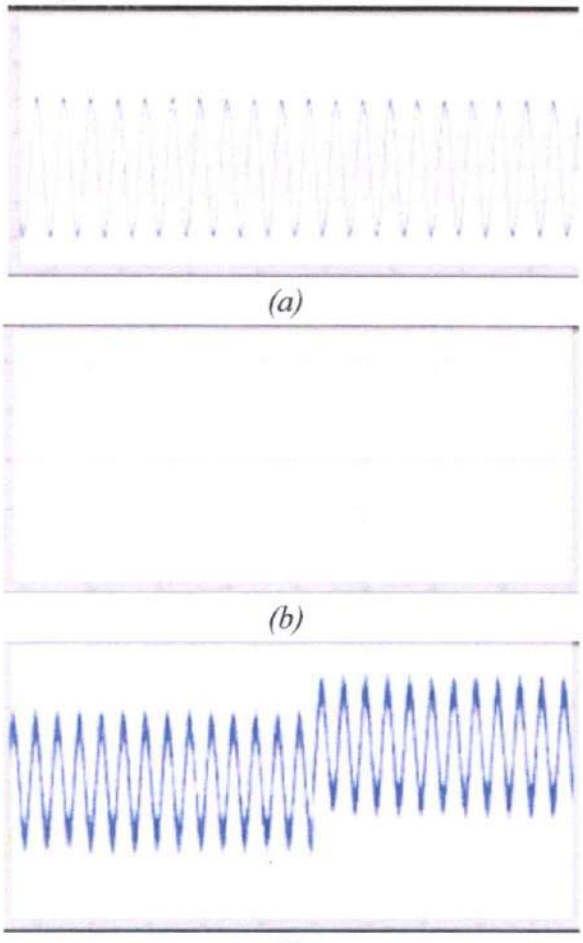
TABLE 2. Design papameters.

Parameter	Value	Unit
Li-battery voltage V_B	100	V
SC voltage V_{sc}	200	V
grid voltage V_G	100	V
grid voltage frequency	50	Hz
inductor L	2	mH
filter inductor L_f	2	mH
supercapacitor SC	2	F
parallel capacitance of the Li-battery C_1	470	μF
parasitic resistors R_2	800	mΩ
parasitic resistors R_C	25	mΩ
parasitic resistors R_{C2}	51	mΩ
internal resistance of the Li-battery R_B	100	mΩ
switching frequency f_s	5	kHz

Figure 1 shows the simulation waveforms when the SBBBC is operating in boost mode. To make the grid cur- rent clear, the amplitude of the grid current is amplified 10 times. The current injected into the grid is in phase with the grid voltage to achieve a unit power factor. As shown in Figure 19(b), when the shoot-through duty cycle ds is 0.25, the proposed converter boosts the 100V Li-battery voltage to 200V SC voltage, which meets the voltage gain given by equation (5). At t D 0:5, the reference current IG_ref of the grid current controller changes from 4A to 5A. At this time, the Li-battery current increases and the output power of the Li-battery increases, this can achieve a fast response of the grid current. The capacitor voltage remains constant and

the energy required by the grid is provided by the Li-battery.

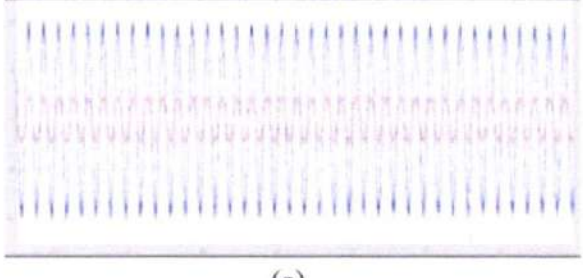
Case_1:V2G Mode



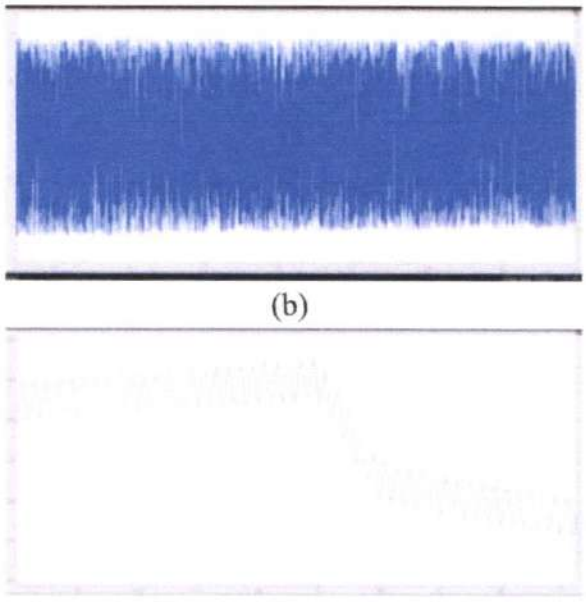
(a) (b) (c)

Fig.1. Simulation results of the proposed system. (a) Grid voltage and grid current. (b) Battery discharge voltage and SC voltage. (c) Battery discharge current.

Case_2 G2V Mode



(a)



(b)

(c)

Simulation results of the proposed system. (a) Grid voltage and grid current. (b) Battery charging current. (c) SC voltage.

V.CONCLUSION

This paper presents a SBBBC for V2G system. The proposed converter not only has high voltage gain and immunity to electromagnetic interference, but also provides bidirectional energyflow path. In this paper, different working modes of the SBBBC are discussed in detail and the small signal model of the converter is established. The zero-pole diagram of the system was drawn, the dynamic characteristics of the system were analyzed and its stability was proved. This paper proposes control strategies for V2G and G2V modes, which implement energy management of the HESS. The controller is designed in the frequency domain, so that the controller has good dynamic performance. Finally, the correctness of the theory and the feasibility of the control strategy have been verified through simulations results.

REFERENCES

[1] F. Naseri, E. Farjah, and T. Ghanbari, ``An efcient regenerative braking system based on battery/supercapacitor for electric, hybrid and plug-in hybrid electric vehicles with BLDC motor," IEEE Trans. Veh. Technol., vol. 66, no. 5, pp. 37243738, May 2017.

[2] S. G. Wirasingha and A. Emadi, ``Classication and review of control strategies for plug-in hybrid electric vehicles," IEEE Trans. Veh. Technol., vol. 60, no. 1, pp. 111122, Jan. 2011.

[3] J. Cao and A. Emadi, ``A new battery/ultraCapacitor hybrid energy storage system for electric, hybrid, and plug-in hybrid electric vehi- cles," IEEE Trans. Power Electron., vol. 27, no. 1, pp. 122132, Jan. 2012.

[4] O. Hegazy, J. V. Mierlo, and P. Lataire, ``Analysis, modeling, and imple- mentation of a multidevice interleaved DC/DC converter for fuel cell hybrid electric vehicles," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 44454458, Nov. 2012.

[5] A. Khaligh and Z. Li, ``Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art," IEEE Trans. Veh. Technol., vol. 59, no. 6, pp. 28062814, Jul. 2010.

[6] M. Ortuzar, J. Moreno, and J. Dixon, ``Ultracapacitor-based auxiliary energy system for an electric vehicle: Implementation and evaluation," IEEE Trans. Ind. Electron., vol. 54, no. 4, pp. 21472156, Aug. 2007.

[7] L. Gao, R. A. Dougal, and S. Liu, ``Power enhancement of an actively controlled battery/ultracapacitor hybrid," IEEE Trans. Power Electron., vol. 20, no. 1, pp. 236243, Jan. 2005.

[8] L. Solero, A. Lidozzi, and J. A. Pomilio, ``Design of multiple-input power converter for hybrid vehicles," IEEE Trans. Power Electron., vol. 20, no. 5, pp. 10071016, Sep. 2005.

[9] M.-E. Choi, S.-W. Kim, and S.-W. Seo, ``Energy management optimization in a battery/supercapacitor hybrid energy storage system," IEEE Trans. Smart Grid, vol. 3, no. 1, pp. 463472, Mar. 2012.

A NOVEL PID CONTROLLER BASED D-STATCOM FOR ENHANCING POWER QUALITY WITH PR-FB CONTROLLER

B.RAMYA[1]| T.KRANTHI KUNAR[2]

[1]PG SCHOLAR, Dept of. ELECTRICAL POWER SYSTEM, Avanthi Institute of Engineering and Technology, Ts, India.

[2]ASSISTANT PROFESSOR, Dept of Electrical and Electronics Engineering, Avanthi Institute of Engineering and Technology, Ts, India.

ABSTRACT: In this project we propose PID controller based solar system fed shunt active power filter for enhancing power quality. In recent years nonlinear loads are explore the distorted waveforms that affect the distribution system. In this proposed system consist of grid, non linear loads and shunt active power filter with solar system. SAHF mitigate the line current harmonics, reactive power and poor power factor. The SAHF system is made up of a three-leg Voltage Source Converter and DC power from a PV module. The first stage of this two-stage system is a DC-DC step-up converter that uses the maximum power point tracking (MPPT) algorithm. The P&O algorithm is used to extract the maximum power. PID controller and Hysteresis are used to calculate reference current. The PWM -VSI is driven by a current controller. To reduce harmonics and reactive power, the proposed PV-based SAHF is used with a diode rectifier load.

I.INTRODUCTION

Petroleum products had been the essential stockpile of solidarity for a really long time, however it accompanies various difficulties as they have confined supply, are expendable and can't be reused. As per IEEE notable 512-2014, most electric supplies Works sufficiently in the event that the entire harmonics truly does never again surpass 5% [4]. Inactive channels were utilized outstandingly to moderate the harmonic anyway it accompanies a few deficiencies. It causes reverberation issue locally and furthermore will quite often be muddled in design if the scope of harmonics to be dispensed with will increment. PV based absolutely APF is earning respect as it can eliminate harmonics from the changed DC result of the PV module. Establishment expense of PV framework is very inordinate, so extricating greatest Power from it is far prudent. For guaranteeing the most extreme exhibition of PV gadget, it is incorporated with MPPT calculation. Demonstrating of PV gadget with MPPT methods are expressed.

II.LITARATURE SURVEY

1)Extensive Approach to Modeling and Simulation of Photovoltaic Arrays

This paper proposes a strategy for showing and reenactment of photovoltaic bunches. The fundamental objective is to track down the limits of the nonlinear I-V condition with the aide of changing the twist at 3 spots: open circuit, most outrageous power, and short out. Given these three factors, which can be given through all business show datasheets, the methodology reveals the quality I-V condition for the single-diode photovoltaic (PV) model which consolidate the effect of the series and equivalent assurances, and ensures that the

PRINCIPAL
Avanthi Institute of Engg. & Tech.
Guntihapally (V), Abdullapurmet (Mdl.), R.R. Dist.

most force of the version fits with the best force of the authentic bunch. With the limits of the transformed I-V condition, you could construct a PV circuit structure with any circuit test framework through the use of fundamental number related blocks.

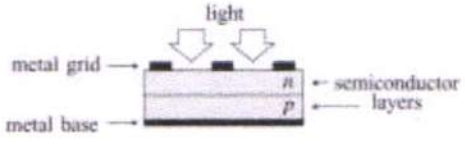


Fig. 1. Physical structure of a PV cell.

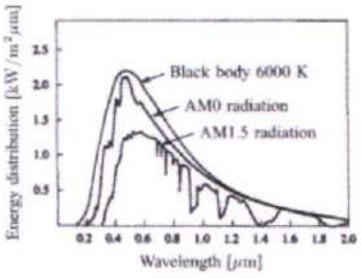


Fig. 2. Spectral distribution of the black body radiation and the Sun radiation in the extraterrestrial space (AM0) and on Earth's surface (AM1.5). *Source: Möller* [2].

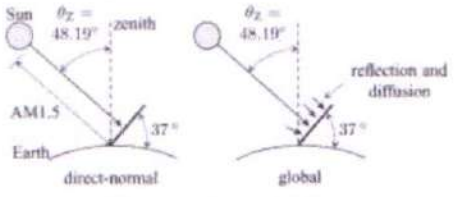


Fig. 3. Illustration of the AM1.5 path and the direct-normal and global incident radiations on a Sun-facing surface at 37° tilt.

The hour of the direction of the sun radiates (given in wide arrangement of airs) is appeared through the x coefficient of AMx described as

$$x = \frac{1}{\cos \theta_z} \qquad (1)$$

Where θz is the viewpoint of the Sun concerning the apex, as displayed in Fig. 3. A bigger x relates to a more extended bearing and a more prominent air mass among the Sun and the floor of the earthbound PV gadget. The in vogue AM1.Five conveyances compare to the range of the sun radiation with a sun point of view θz = forty eight.19◦. Fig. 3 shows the meanings of the AM1.5 course and the direct regular and worldwide radiations.

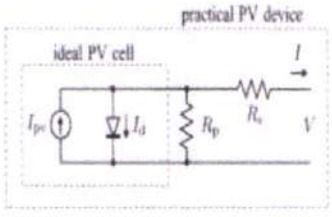


Fig. 4. Single-diode model of the theoretical PV cell and equivalent circuit of a practical PV device including the series and parallel resistances.

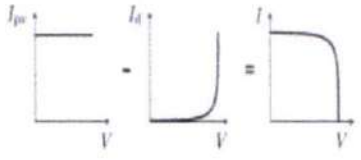


Fig. 5. Characteristic *I–V* curve of the PV cell. The net cell current *I* is composed of the light-generated current I_{pv} and the diode current I_d.

III.PROPOSED SYSTEM

This paper consolidates the PV module with shunt enthusiastic strength line conditioner and examines its general exhibition essentially founded on unique boundaries. For separating the reference current on the spot genuine strength hypothesis is utilized as this arrangement of rules reference infused current with supply voltage. It draws a dc foreordained voltage both via PI regulator or fuzzy great judgment regulator. To change over the reference current extricated and dc contemporary consumed by means of the channel out to exchanging entryway beat, through beat width balance hysteresis regulator is utilized. For following the most extreme working element

of the PV module, P&O calculation is utilized.

3.1 PV AND SAHF MODEL

The result from the PV module is DC which is then connected to a DC upgrade converter, to make voltage stage fitting for the SAHF machine. Shunt AHF ends up being a successful approach to disposing of harmonics through infusing an AC contemporary having importance equivalent in light of the fact that the harmonic anyway with stage moved through 100 eighty°, thus dropping the stockpile current from any harmonic.

A. Generalized PV Model

A photograph voltaic device comprises up of sun module which changes over gentle strength from sun oriented to electrical power through picture electric effect. The same circuit chart of sun cell is given in Fig. 1(a), here Rse and Rs addresses the series and shunt opposition. - V and P-V attributes are portrayed in Fig. 1(b) and Fig.1(c) separately. The element Vmp, Imp and Pmax addresses the greatest power point of the PV cell at which the cell has most proficiency.

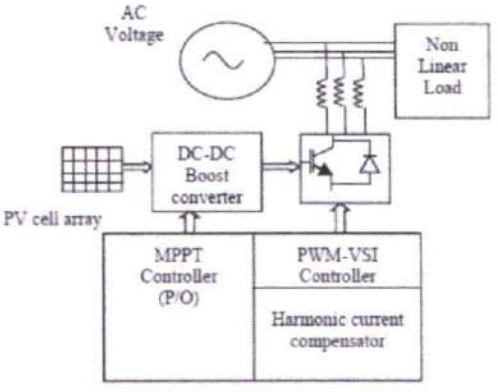


Fig 3. Block diagram of PV- APF system

A. DC-DC Boost Converter

DC boost converter incorporates IGBT that is constrained by a PWM signal produced via MPPT regulator. It incorporates strength putting away factors, guide and an inductor. At the point when the switch recruited utilizing IGBT is shut the cutting edge passes through the inductor and costs it through creating an attractive region. At the point when the switch is open the ongoing declines. The attractive discipline produced will decrease in power to protect load current. Subsequently the extremity of the inductor will turn around. As an outcome the two resources becomes in assortment and consequently developing the voltage charging the capacitor through diode. The result of the DC increment converter is

$$V_o = V_s\{1/(1-D)\} \qquad (3.1)$$

B. DC-AC Converter

In this model a three section bidirectional dc/ac converter is utilized, it incorporates six leg switches. Three palms of the inverter are bogged down with 100 twenty° to produce a three segment AC convey. The semiconductor switches of the 3 hands VSI is gated through PWM beats produced by means of SAHF regulator. For

removing the reference current PI regulator is used. The 3 levels of the convey front line are assessed with the help of unit sine vector layout that is in portion with the stock voltage. The unit sine vector layout is given as:

$$u_{sa} = V_{sa} / V_{sm} = \sin \omega t$$
$$u_{sb} = V_{sb} / V_{sm} = \sin(\omega t - 120^0)$$
$$u_{sc} = V_{sc} / V_{sm} = \sin(\omega t + 120^0) \quad (3.3)$$

PI regulator assesses Imax, the worth of top reference contemporary. The assessed level contemporary increases with the result of unit sine layout to supply leaned toward reference current:

$$i_{sa}^* = I_{max}^* u_{sa}$$
$$i_{sb}^* = I_{max}^* u_{sb}$$
$$i_{sc}^* = I_{max}^* u_{sc}$$

To create exchanging beat of PWM-VSI hysteresis regulator is utilized, hysteresis regulator changes unexpectedly between two levels depending upon the resistance hysteresis band as:

IV. SIMULATION RESULTS

PV-SAHF framework is analyzed in matlab/simulink programming program. The PV cluster powers SAHF which produces remunerating current from the reference current separated from the mains. P-V and I-V qualities of PV exhibit at 25° and forty five ° C cell temperatures is demonstrated in fig. 4 (b) and fig.4 (a) separately. The point got inside the diagram relates to most power element of PV exhibit. A P/O MPPT basically based regulator works at this component for ideal effectiveness of PV exhibit machine. From the attributes it very well might be resolved that with blast in temperature the short out current will increment anyway the open circuit voltage diminishes.

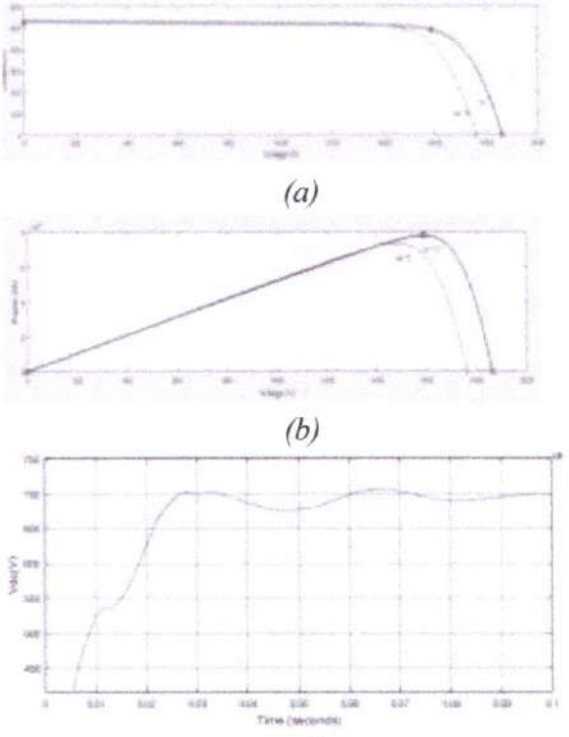
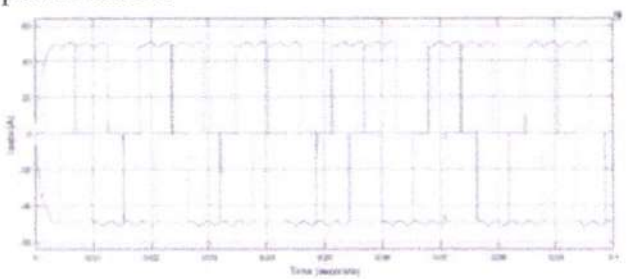


Fig. 4. (a) I-V (b) P-V characteristics of PV array and (c) Vdc

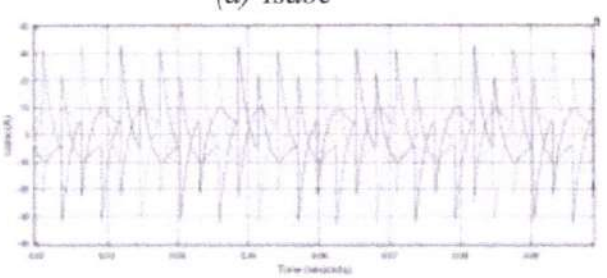
Fig.5 (a) shows the source current of the stockpile mains without the reconciliation of symphonious channel in shunt design, it tends to be seen from the figure that source current contains higher request consonant parts notwithstanding key parts due to non straight burden. The PWM-VSI creates the remunerating current to relieve the consonant parts as displayed in Fig.5 (b). The remunerating current having a similar extent of as that of consonant parts however stage moved to 180°, drops the harmonic. The source current after the mix of SAHF is shown is Fig.5 (c), it very well may be seen that the source current becomes sinusoidal

accordingly turning out to be liberated from harmonic.

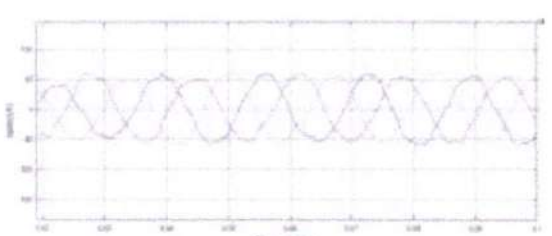
The shunt SAHF framework mitigates the harmonic as well as further develop power factor. Fig. 6 portrays that after the association of SAHF framework the source current turns out to be liberated from harmonic as well as further develops the power factor.



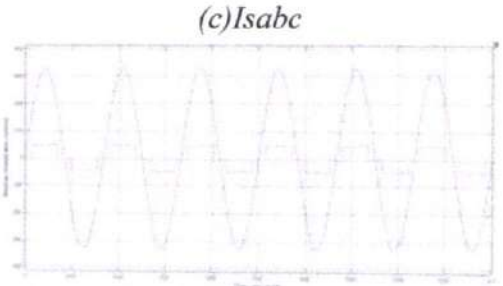
(a) Isabc



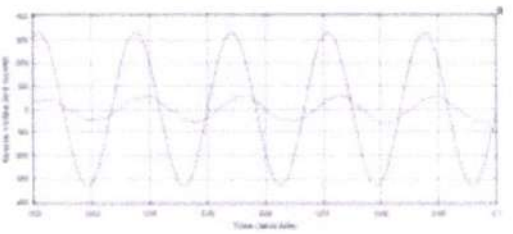
(b)Icabc



(c)Isabc



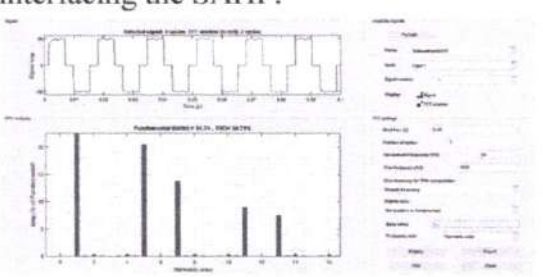
(a)



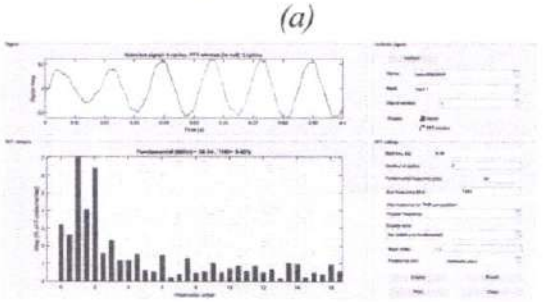
(b)

PQ enhancement is conventional system

Fig.7 shows the size of consonant current present in the source current when associating the SAHF in level of the principal part, it tends to be seen from Fig.7 (a) odd symphonious part is available in the source current when remuneration isn't given, though Fig.7 (b) shows that the odd harmonics are decreased to a palatable level in the wake of interfacing the SAHF.



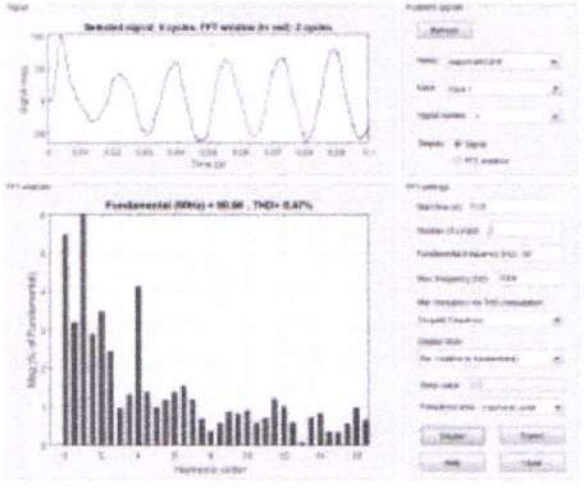
(a)



(b)

THD representation of conventional systems

PRINCIPAL
Avanthi Institute of Engg. & Tech.
Guntihapally (V), Abdullapurmet (Mdl.), R.R. Dist.



PROPOSED SYSTEM THD REPRESENTATION

In conventional system we getting THD is around 9.4% but in case our proposed system we get 8.47% THD

V.CONCLUSION

The exhibition of shunt active harmonic filter gadget controlled through PV cluster framework is examined. A P&O principally based MPPT strategy that is speedier similar to the time region technique has been successfully applied with Boost converter. The SAHF is applied with PWM-VSI regulator. A versatile hysteresis regulator is applied to give the changing pulse width to PWM-VSI. For reference current extraction PID regulator is utilized. PID oversee approach has been applied to control the reference current by controlling the dc voltage got from PV cluster contraption. The possibility of SAHF and attributes of symphonious component and compensation current are referenced. The general presentation of PV-SAHF framework is dissected under unmistakable working situation in Matlab/Simulink climate and it very well may be seen that the symphonious parts come appropriately under careful IEEE liked. The shunt design of SAHF framework not handiest mitigates the harmonics anyway likewise further develops the power factor. The proposed setup is less expensive and less hard to accumulate as the expected quantities of sensors are decreased.

VI.REFERENCES

1)L. Hassaine, Emilio Olías, "Digital power factor control and reactive power regulation for grid-connected photovoltaic inverter", Renewable Energy 34 (2009) 315 321.

2)Najib Hamrouni , "New control strategy for 2-stage grid-connected photovoltaic power system," Renewable Energy,vol. 33, no. 10, pp. 2212 2221, 2008".

3)Marcelo Gradella Villalva , " **Comprehensive Approach to Modeling and Simulation of Photovoltaic Arrays"** IEEE. Trans. PowerElectron., vol. 24, no. 5, pp. 1198 1208, May 2009.

Cloud Computing and Data Science
http://ojs.wiserpub.com/index.php/CCDS/

UNIVERSAL WISER PUBLISHER

Research Article

An Improved Fast and Secure CAMEL Based Authenticated Key in Smart Health Care System

Syed Khasim[1*], Shaik Shakeer Basha[2]

[1]Department of Computer Science & Engineering, Dr. Samuel George Institute of Engineering & Technology, Markapur, Prakasam Dt, 523316, Andhra Pradesh, India
[2]Department of Computer Science & Engineering, Avanthi Institute of Engineering & Technology, Gunthapalli, Abdullahpurment Mandal, Hyderabad, 501512, Telangana, India
Email: khasim716@gmail.com

Received: 23 March 2022; **Revised:** 09 June 2022; **Accepted:** 01 July 2022

Abstract: Seeing as Smart Healthcare Systems provide cloud services for storing patient health records, data security and privacy are critical to the company's success, and patients do not want their identities to be revealed. The authentication procedure requires disclosing users' personal data, such as a username and password, on the authentication server in order to protect their identities. The patient's privacy may be invaded if the patient can be observed or linked to by the patient's unfortunate foes. As a result, we propose in this paper a system that gives patients anonymity, protection, and privacy of sensitive healthcare data from the Authorization Service and enemies. A camel-based rotating panel signature program was used in our proposed work to provide anonymity to health records while also adding extra security to the network layer. The effectiveness of the programs was assessed using theoretical analysis, which revealed that the program has a range of security characteristics and is resistant to multiple attacks.

Keywords: Smart Healthcare Systems, anonymous authentication, Camel algorithm, anonymity

Abbreviations

ECC	Elliptic Curve Cryptography
RSA	Rivest-Shamir-Adleman
PCs	Personel Computers
SAGE	Scheme Against Global Eavesdropping
WBANs	Wireless Body Area Networks
CLS	Certificate less Signature
PKI	Public Key Infrastructure
VLR	Verifier Local Revocation
CSP	Cloud Service Provider
RS	Registration Server

DOI: https://doi.org/10.37256/ccds.3220221423

1. Introduction

With cloud computing expanding in popularity, many healthcare institutions are turning to it for a variety of reasons. Healthcare practitioners with substantial savings and computations are motivated to utilize cloud-based servers since cloud computing offers several benefits such as scaling and cost savings [1]. Many advancements in embedded systems, biosensors, and wireless networks have resulted in the outstanding development of wearable sensors in the human body to collect all health records such as blood pressure and heart rate in recent years. Hospitals offer their services via cloud servers, where data are evaluated in order to improve the data quality and the health of the sensors that are delivered here for data processing [2]. Figure 1 shows an example of a smart cloud-based healthcare system for patient identification and anonymous service access in smart healthcare systems. At the same time, we must solve some of the difficulties associated with sharing data on unreliable cloud servers, such as losing patient control over data, health, and privacy violation, and putting patient privacy and the cloud system for health care [3]. We need to create mechanisms to preserve users' privacy, eliminate the risks of losing physical control over data, and secure access to patients' data in a virtual environment from harmful users while maintaining their confidentiality and integrity. Due to the higher processing power, traditional techniques of safeguarding an individual's privacy may not be sufficient. Users' online actions are extremely risky since they can be used to examine cloud servers or eavesdrop on surfing histories and location footprints. Our solution includes an authentication procedure that allows patients to be identified across all health services [4].

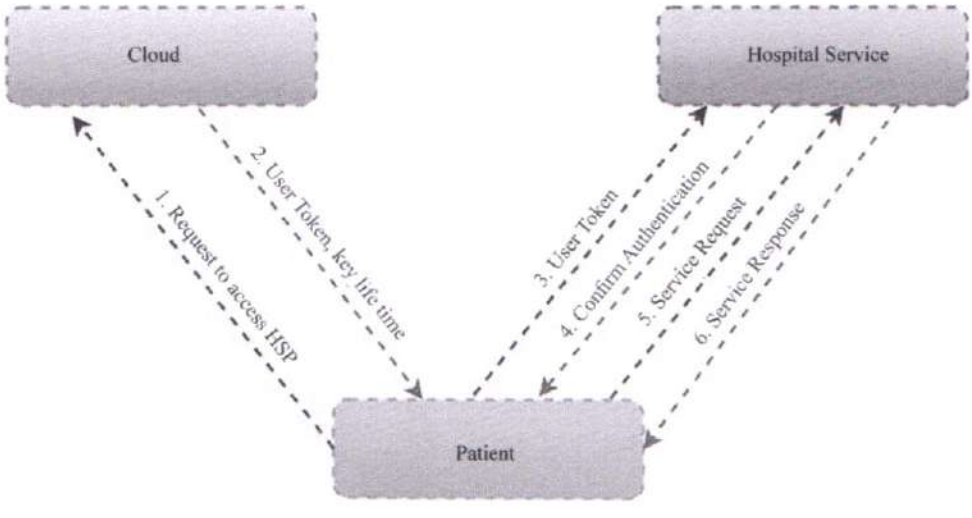


Figure 1. Smart Healthcare Systems for Patient authorization and anonymous service access. The operation of the proposed scheme is strong and attractive on cloud servers to store and hide the identities of patients giving priority to their privacy.

In recent years, a slew of privacy protection accreditation methods has been presented. Cloud servers, on the other hand, are incapable of safeguarding users' personal or sensitive data. When using internet services, offers a number of risks. When using cloud services in health systems, patients do not want to divulge their identities. Patients are hesitant to trust such apps unless the system guarantees complete privacy and security. Data that has been saved could be useful [5]. As a result, the program must be trustworthy and secure. Personal information, such as usernames, histories, and biometric traits, may be used to compromise a patient's identity and extract information from concealed forms, such as evaluating patient preferences or Internet traffic. The following is a list of goals for our work that we would like to attain [6].

Without giving any personal information, the patient is unanimously approved by the authorization server.

• Multiple requests from the same patient cannot be linked through an authorization server, but the patient can be identified through auditory, for example.

• The user in the middle, the computer, is immune to attacks such as back attacks and auditory attacks.

• Sending communications can be verified by the recipient.

The rest of the paper is organized as follows: Section 2 discussed a literature review of previous authentication secure health care system models. Section 3 discusses the proposed method. Section 4 shows and describes the test results of the proposed work. Finally, Section 6 completes the conclusion of proposed work.

2. Related work

This section elaborates on the various issues using different techniques of secure health care modules. In bunch signature, without uncovering the partial character, any substantial gathering part permits to sign quite a few messages in the interest of the gathering. Though, the bunch supervisor has rights to uncover the personality of the endorser when made trouble. Most of the gathering marks depend on customary cryptography like ECC, RSA, and discrete logarithm. On the off chance that quantum PCs arise, these plans would be effectively broken. The new character puts together, gathering marks based on respect to bilinear guides with some security properties. In this plan, the length of the marks is free and the size of the gathering pubic key on the size of the gathering. The plan was appropriate for huge gatherings where the gathering part can sign many messages utilizing a similar key pair. This plan has downsides. The personality based validation frameworks experience the ill effects of the key escrow issue. The key expected to encode or decode is held, and retained so that under particular conditions, an approved party might access the key. As the escrow specialist holding all the cryptographic keys, the key escrow frameworks are considered a security hazard and may spill data or a single disappointment point. Additionally, when a client's private key is compromised, it turns out to be exceptionally difficult to renounce the client [7].

The e-Health framework is imagined as a promising way to deal with further developing medical services through data innovation, where security just as protection is essential for an enormous scope organization and its prosperity. This paper tended to on a solid protection saving Scheme against Global Eavesdropping, named SAGE, for e-Health frameworks. The proposed SAGE can accomplish the substance situated security additionally the logical protection against a solid worldwide enemy. The SAGE has been exhibited effective as far as transmission delay. This plan had a significant disadvantage that it was unreasonable because of substantial computational overhead when straightforwardly applied to the conveyed medical care frameworks. The plan couldn't bear the weight calculations [8].

The proposed mysterious confirmation conspires in cloud climate for s-wellbeing. The reception of an e-Health Cloud has various advantages, particularly sharing, putting away, permitting, and trading data between different clinical establishments, decreasing expense, accessibility of data, lessening costs, quick administrations, and so on Furthermore, saving character protection is a critical test of safety in all conditions just as establishes especially an intense worry in cloud conditions. It puts to the main goal of the client while utilizing administrations. Without a doubt, a significant boundary to the reception or utilization of cloud clients is dread of security misfortune in the cloud worker, especially in an e-Health cloud where clients show restraint toward touchy information or data. Clients/patients may don't have any desire to reveal their characters to the Cloud Service Provider when utilizing its administrations. An approach to secure them is making them unknown to the workers. This paper proposed a versatile and adaptable methodology for patients' personality security to ensure an e-Health Cloud through a mysterious verification plot. This plan depends on blind marks which permit patients to devour cloud benefits namelessly over the world. The framework slacked to give any insights concerning client enlistment and denial. Conversation insights concerning security investigation are not given [9].

In research on application, arranged plan about Wireless body region organizations (WBANs). That is generally utilized telemedicine, which can be used for home medical care and continuous patients checking. In WBANs, the sensor hubs assemble the customer's physiological information. Send it to the clinical focus, the customers communicate it to the clinical focus, the customers' very own information/data is touchy and there are a lot of safety dangers in the additional body corresponds. Henceforth, the security and security of customers' physiological information should be ensured and guaranteed first. Many existing validation conventions for WBANs neglected to consider the key update stage. This paper proposes proposed a proficient verified key arrangement conspire for WBANs in addition to adding the key update stage in improving the security of the plan. In the confirmation stage, to decrease the calculated cost, meeting keys are produced during the enlistment stage and kept covertly. The plan was more productive and dependent

on bilinear pairings yet the repudiation cycle was not plainly characterized if there should arise an occurrence of debate [10].

Wireless Body Area Networks (WBANs) is assistance, which is proficiently utilized at present for giving productive and got medical care administrations. This paper included Certificate less over the remote organization plot for the security reason. Furthermore, a couple of safety conventions are being utilized in both end client and specialist organizations. This plan was proposed to carry out the mysterious light-weight confirmation convention. A WBAN client can without much of a stretch access the telemedicine framework through this convention. Utilizing WBAN administrations, the doctor gets refreshed and the constant data of the patient. The Certificate less Signature (CLS) conspire is nearly used to exceptionally satisfying the security saving needs in WBAN by certificate less encryption likewise intended to dispense with the downsides of the PKI based plan and it doesn't need personality based encryption and computerized authentication, i.e., no key escrow issue. CLS allocated the security by giving private keys to the patient due to that it is inconceivable for the outsider or the aggressor to get to the private data of specific meetings that occurred during validation measure. The plan additionally gave enormous disadvantage of denial method itemizing inappropriately [11].

An unknown verification conspires for remote organizations utilizing Verifier Local Revocation (VLR) bunch signature plot. In the progression of information driven advancements and the Internet of Things in gathering and dispersing tangible information, security and protection turn out to be generally significant and helpful needs. This worry is a direct result of tactile information ordinarily communicated on remote organizations to-ward server farms which is effectively or for the most part noticed for the objective l of organization traffic investigation. Also, the gathered information in server farm can be handily gotten two from different clients, programmers too, if the framework doesn't manage any legitimate security system. In this proposed unknown validation arrangement of blending bases verifier-nearby disavowal bunch signature plot that confirms remote hubs (i.e., sensor hubs) of a specific advantage gathering to the door hub in communicating information. An extra accomplishment is a mysterious verification for getting information to the server farm. Where the plan helpless against replay assaults additionally a noxious Group Manager can imitate a client [12]. The Table 1 shows the various smart health care secure systems comparisons between 2018 to 2022, due to its impact this proposed work has been started to implement.

Table 1. Comparison of Smart Health Care Secure System

Reference	Year	Description
[13]	2018	The need for a dependable end-to-end communication process it-based healthcare applications are discussed, as well as the development of communication technologies that can meet these requirements. Bacterial infections, heart disease, musculoskeletal injuries, and neuromuscular disorders are all represented in the study.
[14]	2019	A comprehensive examination of IoT-based software and systems in smart medical systems is offered. To provide meaningful insight into modern healthcare systems, various apps and services is explained in terms of their major goals and fields of application.
[15]	2021	A table summarizes the standards, specs, benefits, and drawbacks of the most recent WBAN-based healthcare applications. At the end of this paper, open concerns and major obstacles are tackled after mentioning it-based health care services and applications.
[16]	2021	The design of smart health systems is discussed, as well as the main requirements for these systems. Future directions and open topics are discussed at the conclusion of this study to ensure that smart healthcare systems evolve enough and quickly.
[17]	2022	Traditional healthcare system needs are discussed, as well as an overview of the smart healthcare infrastructure and the current state of new technologies employed in smart healthcare systems. The primary applications and services, as well as the obstacles of smart healthcare, are explored to provide a thorough understanding of the system's requirements and functions.

3. Proposed methodology

The camel-based system was utilized in the suggested anonymous authentication scheme to prevent users from acting as unreliable authentication servers in smart cloud-based healthcare applications.

In the event of harmful activity, the suggested approach provides a means for detecting privacy violations with the least amount of risk. Each group has an expiration date and members are reminded to update their keys on a regular basis to speed up the authorization process. When a member's key is returned, they must reveal their previous credentials. Furthermore, anonymous authentication techniques are commonly seen as lonesome. By connecting to a physical location or a person, a cloud service provider operating on the Internet can connect subsequent requests through an IP address. As a result, the software used Camel, which gives network-level anonymity to users while reducing the amount of data available to the cloud service provider. Camel's hidden service cannot be reached anonymously.

It completes anonymous authentication processes with minimum information, allowing neighboring links to be connected to the service provider. Instead of using a direct connection, Internet users connect a series of virtual tunnels to shield the camel network from traffic analytics attacks, which can be used to infer who is talking to whom on the public network.3 The camel, which is connected to the middle relay terminals via a relay terminal, transports traffic from the middle relay terminals to the exit terminals, preventing the entry and exit terminals from becoming acquainted.

The exit nodes, on the other hand, route traffic to the customer's desired destination. The encryption key for encryption is known by each node. We engaged Camel to work on the server side of our project, and there is a plan to run two secret services, which points to a strategy that uses elements of the CSP and RS protocols. The camel on the customer page can be used to encrypt internet traffic as a proxy application. It can cover the entire world by jumping via a succession of computers.

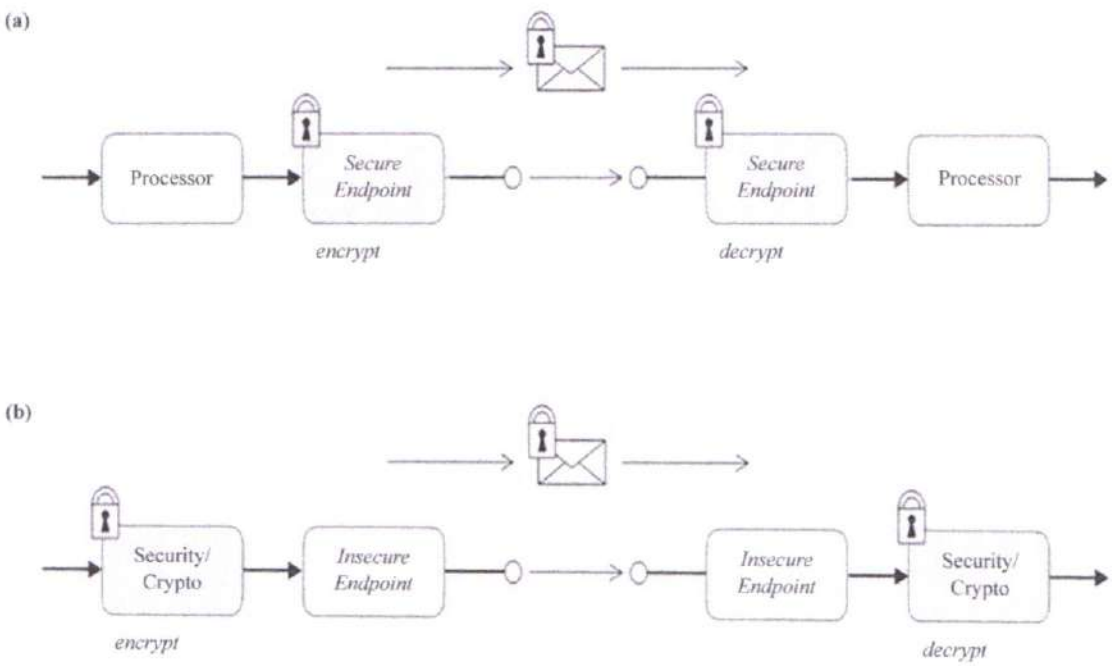


Figure 2. (a) and (b) Apache Camel Security Architecture [18]

Figure 2 The Camel algorithm provides a variety of security options and levels that can be used on Camel routes. These many types of security can be employed in conjunction with one another or on their own. It is simple to create Digital Signatures for Exchanges using Camel cryptographic endpoints and Cryptographic extension. Camel provides a pair of customizable endpoints that work together to establish an exchange signature in one part of the workflow and

then verify the signature in another section of the workflow [18].

Part (a) of the endpoint security diagram depicts a message exchanged between two routers with secure endpoints. The producer endpoint on the left establishes a secure connection with the consumer endpoint on the right (usually using SSL/TLS). In this instance, both endpoints provide security. With endpoint security, it is typically possible to perform some form of peer authentication and sometimes authorization.

The payload security part (b) depicts a message transmitted between two routers with vulnerable endpoints. Use a payload processor that encrypts the message before transmitting and decrypts it after it is received to secure the communication from unauthorized spying in this situation.

3.1 *Proposed design architecture*

3.1.1 *Architecture description*

a) Trento: Trent introduced as a facility, is confided in the party that re-appropriated its foundation to CSP. Liable for introduction, disavowal, key age, and evaluation.

b) Cloud Service Provider: CSP offers types of assistance to clients of key trading. It is an unbelieved element that can acquire a lot of data of the client during confirmation measure where data given by Trent and RS. The client may be ready to conceal their personality from CSP.

c) Registration Server: RS just does the enrollment interaction of the client to start framework entrance. It trades data to Trent and CSP according to mentioned.

d) User/Patients: User gets to the cloud administrations from CSP with approved records to RS. Client solicitations to CSP for administrations without revealing their personality with trading some keys given from Trent (Figure 3).

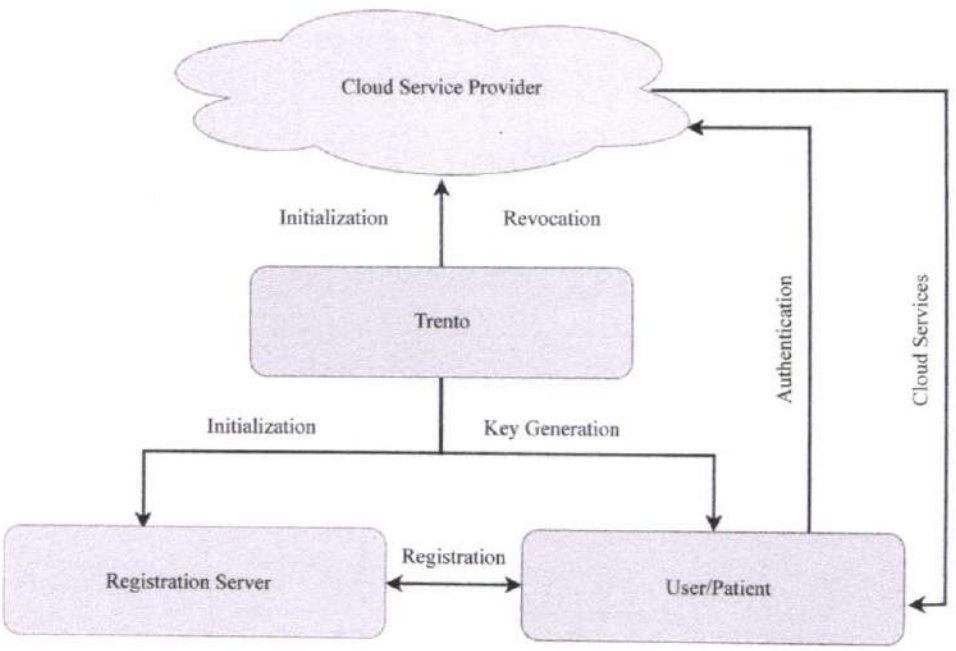


Figure 3. Proposed Design Architecture

3.2 *Proposed design architecture*

Anonymous Authentication scheme includes 5 phases [19]:

1. Initialization
2. Key Generation

3. Registration
4. Authentication
5. Revocation

Initialization: Trent creates a private-public key pair and gives public half to CSP and RS. With a scope of pairings clients should utilize concurred pairings. When Trent sets up the framework, reinstatement is finished.

Key Generation: Trent produces bunch key that substantial for quite a while, ace gathering key and from that infers public gathering key which is somewhat arbitrary and some degree got from bunch chief key. Trent produces a marked endorsement containing data. Trent encodes and sends that endorsement to CSP and RS by utilizing its public key. CSP and RS unscramble and confirm that the authentication is really from Trent with the assistance half open key given past. Trent needs to refresh bunch keys each season of the same key age measure.

Registration: RS presently does the enrollment interaction of the client to start framework entrance. It trades data to Trent and CSP according to mentioned.

Authentication: A user wishes to demand assistance from CSP and starts the verification interaction. The client associates with CSP over an unknown organization and sends the gathering key to verify. CSP checks the gathering key matches a put-away authentication sent by Trent and ought not to be terminated. CSP produces an irregular number and sends it to the client. Client and CSP play out a zero information convention. The client produces a signature and sends it and solicitation to CSP. CSP proceeds to the subsequent stage if the balance remains constant/substantial mark in any case ends the association. CSP additionally makes sure that the client didn't play out the convention with the renounced key. CSP encodes and plays out the mentioned administration with an encryption key and saves it in the review log so that lone Trent might understand.

Revocation: When Trent tracked down that a client has been manhandling the administrations, he disavows the client's vital. Key disavowal fundamentally permits untrusted CSP who keeps a decoded log to interface the entirety of clients' associations and ought not to be utilized essential not by ending a customer's administration. Trent demands the enrollment log and review log from RS and CSP separately and decodes it to get demands. Trent utilizes bunch signature ace key and the rundown of record of interaction to separate which bunch part held marking key to mark the message and burned-through which administration. Trent tests for each record in enrollment log, if a match is discovered, Trent figures the relating boundary and adds it to renouncement log. Trent shares the following data for clients with CSP to disavow client's participation key. To permit CSP to get confirmations of participation made by client and deny offering administrations to him. RS eliminates clients from the rundown of adequate customers when Trent sends the client's character to it.

3.3 *Proposed algorithm*

3.3.1 *Key generation*

Public key and private key generated.
The public key generation equation: $Q = d \times P$
Where k and d is random number selected within the range of (1 to n − 1),
P is the point on the curve and Q public key and d is the private key.

3.3.2 *Encryption*

Input
1. String = message M (plain text)
2. Public key = key Literal types as Plain text, encrypted text Output
1. START
2. Init = (ENCRYPT MODE, key)
3. Plaintext = Input message
4. Encrypted Text-do Final (plaintext)
5. Encrypted String = cipher text cipher text 1 = $k \times P$ cipher text 2 = $M + k \times Q$
6. Return encrypted String.

3.3.3 *Decryption*

Input
1. String = cipher text
2. PrivateKey = key Literal types as Ciphertext, decrypted text Output
1. START
2. Init-(DECRYPT MODE, key)
3. Ciphertext-cipher text
4. Decrypted Text-do Final (cipher text)
5. Decrypted String-message (plain text) M = cipher text 2 d × ciphertext1
6. Return decrypted String (Figure 4)

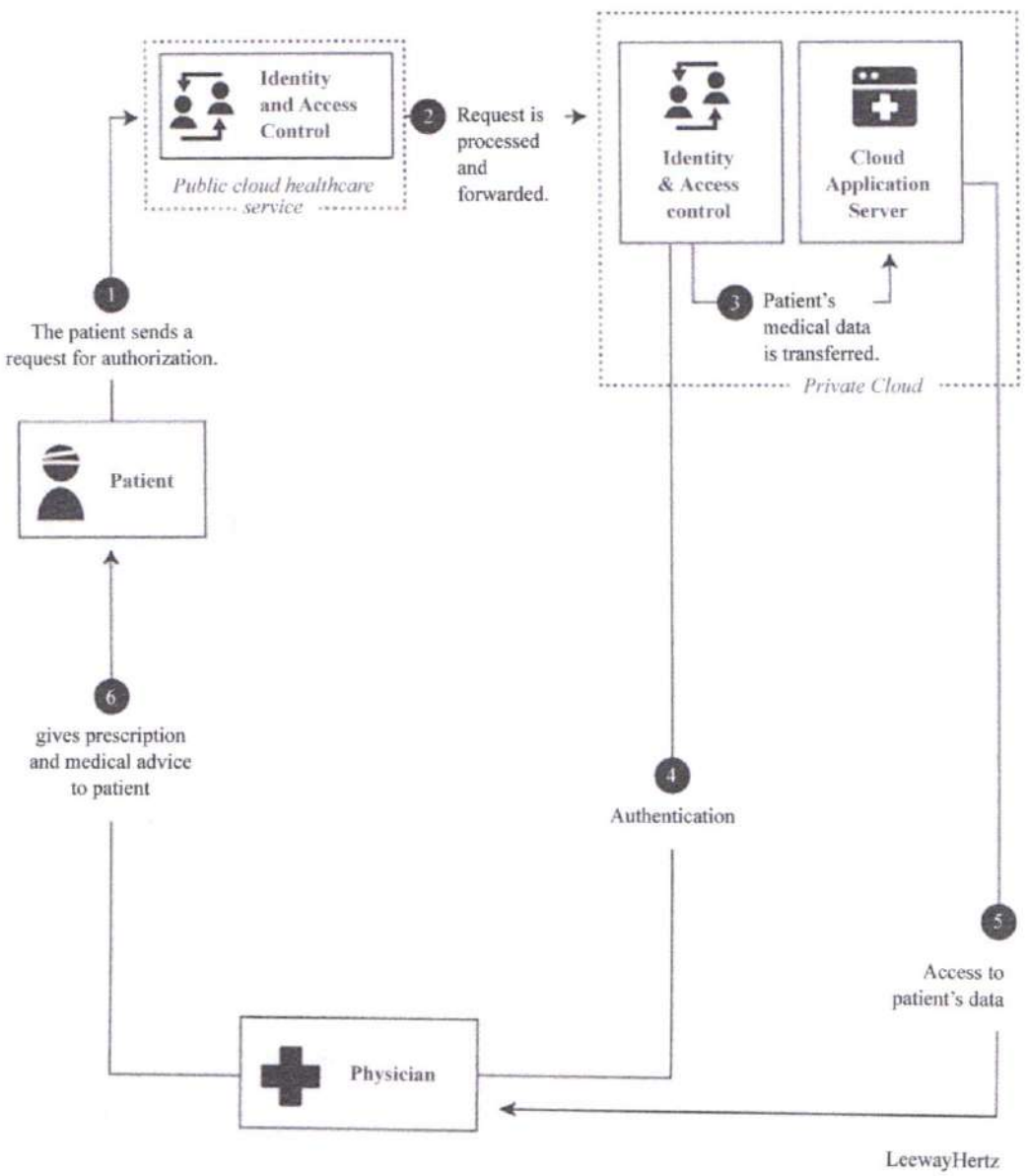


Figure 4. Architecture of private and public cloud communication scenarios [20]

3.4 *Requirement specification*

1. Software Requirements Microsoft Windows 7 and Above Net Beans IDE 8.
2 Java Development Kit (JDK) 1. 7 MySQL 5.5 onwards Application server, Tomcat 5.0
The following steps of cloud-based architecture gives a complete idea of the overall workflow process.

3.4.1 *Stage 1: Patient requests authorization*

Public cloud administrations are tended to exclusively by other clients like patients and outsiders like insurance agencies, drug stores, research medical services organizations, and drug producers. A patient is additionally expected to be an outside client. Thus, the signs on utilizing (username and secret word) addressing public personality and access control cloud administrations to put a solicitation for approval [20].

3.4.2 *Stage 2: Request is prepared at public cloud and sent to private cloud organization*

In light of the solicitation type for capacity, access, or preparing wellbeing information, it is handled at the public cloud level and is sent to the character and access control administration from the private cloud.

3.4.3 *Stage 3: Request is either acknowledged or dismissed*

On the off chance that a private cloud worker acknowledges the solicitation, it is sent to a medical care private cloud application worker. Unexpectedly, if the solicitation is dismissed, an advising message is sent indicating the solicitation's dismissal.

3.4.4 *Stage 4: Physician demands approval*

The doctor is viewed as an inner client. In this way, he signs on to the private cloud benefits and sends an approval demand containing the client and secret phrase to personality and access control.

3.4.5 *The doctor's solicitation is prepared to get the information from the cloud application worker*

When the confirmation is effective, private cloud administrations measure the solicitation, and doctors can get the information from the public cloud application worker.

3.4.6 *A clinical exhortation is straightforwardly shipped off the patient*

A doctor can straightforwardly send criticism as far as clinical counselor medicine to the patient.

Growing such kinds of cloud-based medical care answers for provincial wellbeing and in case of debacles is significant. Also, caregiving organizations and clinical experts should start utilizing cloud-based clinical records and clinical picture chronicling administrations. This sort of arrangement's principal objective is to lessen the difficult undertaking of the specialists and clinical staff worked on clinical frameworks and successful patient consideration [21].

4. Results and discussion

This section discusses the performance evaluation of the implementation of proposed work and compared various algorithms with different features and parameters. In a hospital setting, all of the patient's health information will be gathered. We have created a patient health information form which should be filled out by a nurse or doctor in our suggested job. A table named the health status record will have a complete collection of data (PHR). The PHR is consolidated in the cloud architecture to offer the necessary health data for detection alerts and therapies based on medical professional analysis. IoT is used to integrate networking elements, displays, actuators, sensors, and other healthcare devices and equipment in a multidimensional system. This contributes to the primary trends on the Internet of Things-based medical industry, which focuses on wearable gadgets, robotic surgery, and other cutting-

edge technologies. Experimental results presented in the machine learning field frequently utilize statistical tests of significance to compare learning algorithms. These tests provide a sound response to the issue of whether one machine learning algorithm is superior than another at a given learning task. However, in machine learning contexts, determining the significance statistically is not always simple. Precision is a common metric in many software toolkits for general data analysis and machine learning. Utilizing qualified doctors, pathologists, or radiologists to review medical imaging and identify the underlying causes of clinical diseases is the current clinical standard.

Table 2. Comparison of Features

Features	KG [22]	ECA [23]	H [24]	E_M [25]	Proposed
Anonymity	√	√	√	√	√
Mutual Authentication	√	×	√	√	√
Forward Unlink ability	√	√	×	√	√
Traceability	√	√	√	√	√
Revocation	×	×	√	√	√
Efficient Credential Update	√	√	√	×	√
Communication, Integrity	√	×	√	√	√
Resistance to Modification Attacks	√	×	√	√	√
Resistance to MitM Attacks	√	×	√	√	√
Resistance to Replay Attacks	√	×	√	√	√

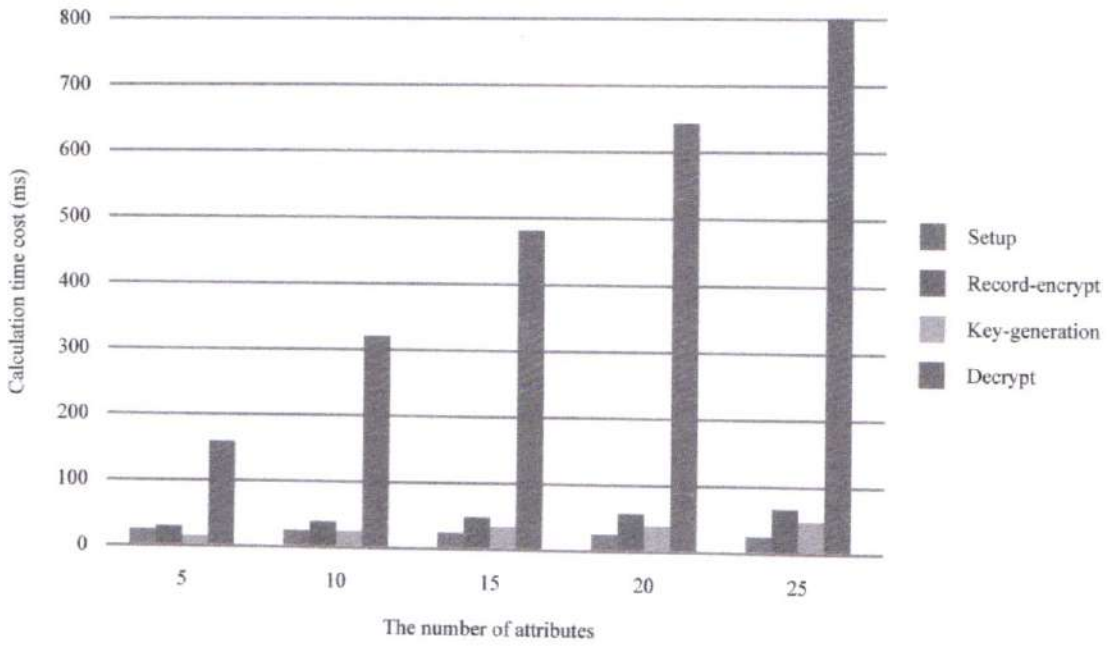


Figure 5. Higher efficiency of all attributes graph for health care system

- KG- Generate public/private key pair
- ECA- Elliptic Curve Addition
- H- Hash Operation
- E_M- Modular Exponentiation

As shown in Table 2, our calculation gives the entirety of the ideal provisions and insurances against assaults. The calculation that comes nearest is that of which needs forward-unlink capacity. It very well may be found in that the pseudo personality created in enlistment is given as a piece of each validation bundle utilized, making the exchanges inconsequentially linkable. Additionally, for a few of the calculations recorded, the issue of accreditation renouncement isn't expressly tended to; nonetheless, in the event that it seems conceivable that the convention could give qualification repudiation, the plan is given to acknowledge for giving denial also. The Figure 5 shows a graphical representation of comparison of a number of attributes with time costs, for the effectiveness of higher efficiency of all attributes of the health care system.

Table 3. Comparison of Execution Time

Cryptographic Operations	Execution Time in ms
KG [22]	625
ECA [23]	496
H [24]	326
E_M [25]	126
Proposed	30

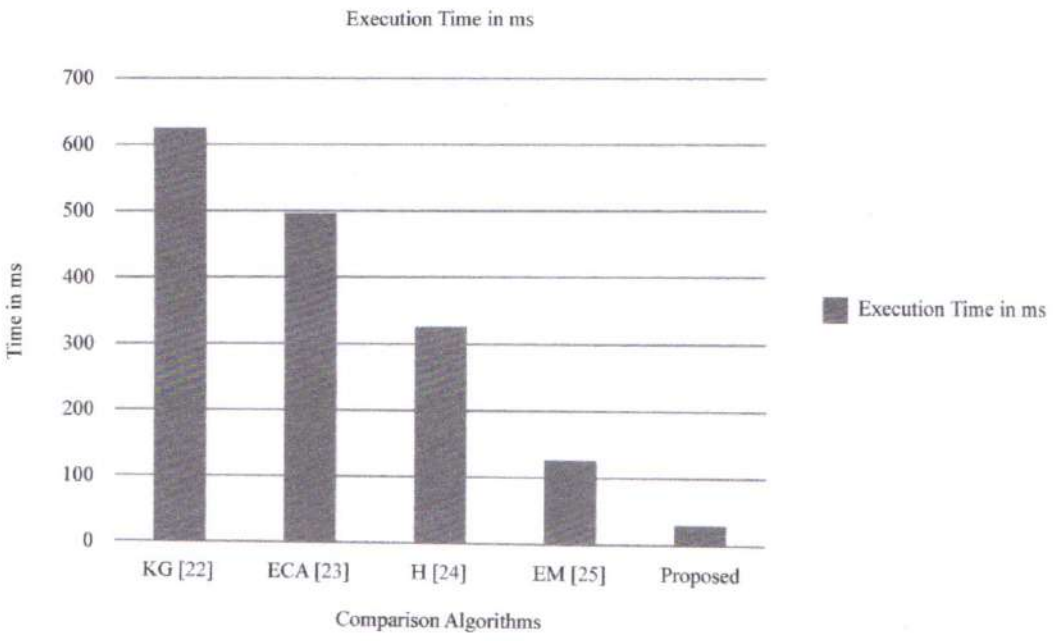


Figure 6. Comparison of Execution Time

Table 3 provides the execution times for each method, which can be used to evaluate the relative complexities.

In the start up and authentication phases, it can be seen that our approach is considerably faster than other algorithms, which is the only other algorithm that has the ability to unlink. In the revocation phase, however, it is slower. The Figure 6 shows a graphical representation of different algorithms execution time's from the reference [22] to [25] compared with proposed algorithm. The Figure 6 shows the effectiveness of proposed algorithm execution time has less than the previous algorithms.

Table 4. Communication overhead for Each Algorithm

Algorithms	Initialization (bits)	Registration (bits)	Authentication (bits)	Revocation (bits)
KG [22]	0	2592	7045	N/A
ECA [23]	544	1952	6914	N/A
H [24]	376	864	1856	N/A
E_M [25]	368	768	1056	N/A
Proposed	1480	576	2368	1024

Then we compare (see Table 4 and Table 5) the algorithms we've looked at based on how many one-way communications are required for each step of the protocol. Table 4 displays the results. The number of patient records to be packaged in a single transmission from the database of physicians is denoted by the integer t in Lin's scheme. For the sake of initialization, it is assumed that each message publication necessitates a single transfer. The Figure 7 shows a graphical representation of different algorithms, communication overhead from the reference [22] to [25] compared with proposed algorithm. The Figure 7 shows the effectiveness of proposed algorithm communication overhead has higher than the previous algorithms.

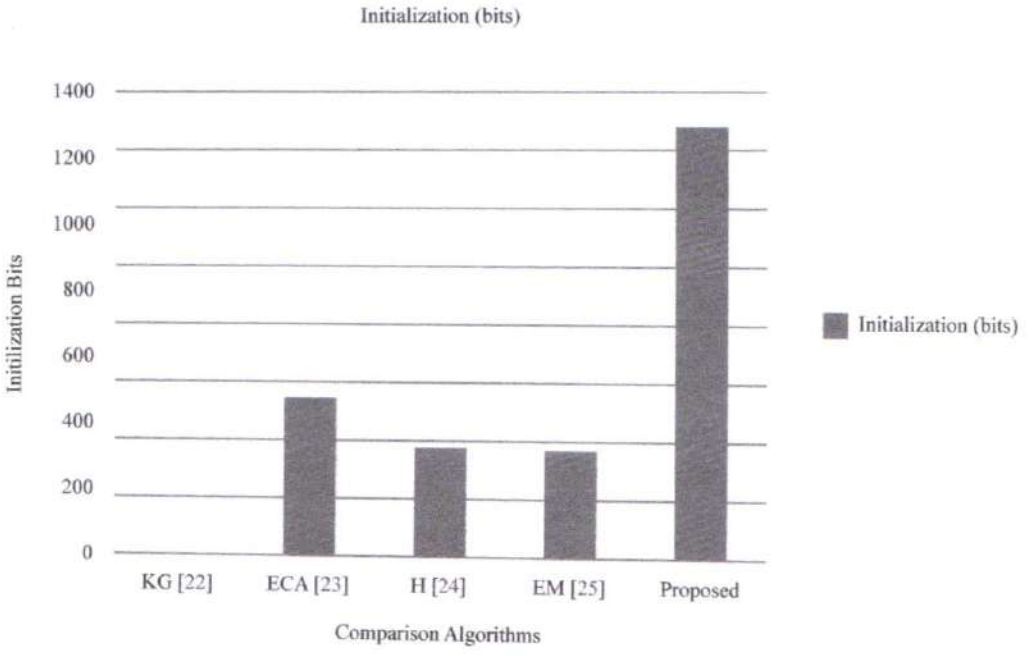


Figure 7. Communication overhead for Each Algorithm

Table 5. Performance validation of proposed with existing algorithm

Parameters	DES [26]	BLOWFISH [27]	AES [28]	Proposed
Network lifetime	150 s	155 s	168 s	195 s
Latency	0.622 ms	0.56 ms	0.5 ms	0.46 ms
Scalability	0.59 ms	0.89 ms	0.73 ms	0.92 ms
Security	87%	82%	95%	97%
Encryption Time	52 ms	43 ms	39 ms	38 ms
Decryption Time	85 ms	82 ms	78 ms	77 ms

Because of the more modest key sizes utilized in Camel, the security of the framework can be effortlessly increased by expanding the critical size without influencing the computational intricacy. The plan adds an additional layer of security against traffic investigation assaults by a snoop by giving secrecy at the organization layer by utilizing TOR. The plan shields patients' delicate information from a snoop and untrusted cloud workers. One notable element of our plan is that the clinical application or specialist organizations can't uncover the character of the patient consequently securing the protection. In this paper, we have planned a viable framework that is secure and proficient. The proposed verification plot guarantees that the patients can devour administrations without uncovering their personality at the hour of utilization or reflectively.

5. Conclusion

The success of smart cloud-based healthcare applications hinges on the protection of patients' privacy. We present an anonymous authentication mechanism for a smart cloud-based healthcare application in this work. Patients' privacy is protected under the proposed approach when they use Cloud services. The proposed work employs a rotating board signature pattern based on a camel. The system fails due to the camel's small key sizes without affecting the computational complexity. This application adds an extra layer of security against a deaf person's traffic analysis attacks by hiring a camel to provide anonymity in the network layer. This application safeguards critical patient information from a deaf person and unstable cloud services. One of the most important aspects of our program is that medical use or service providers are prohibited from disclosing patient identities, ensuring patient privacy. We have devised a realistic, safe, and effective method in this paper. Patients can access the services at the time of consumption or without revealing their identity under the suggested certification process.

Conflicts of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] Sowjanya K, Disrupt M, Ray S. An elliptic curve cryptography based enhanced anonymous authentication protocol for wearable health monitoring systems. *International Journal of Information Security*. 2020; 19: 129-146.

[2] Jain S, Gui Z, Ji S, Shen J, Tan H, Tang Y. Cloud-aided lightweight certificateless authentication protocol with anonymity for wireless body area networks. *Network and Computer Applications*. 2018; 106: 117-123.

[3] Wei F, Vijayakumar P, Shen J, Zhang R, Li L. A provably secure password-based anonymous authentication

scheme for wireless body area networks. *Computers & Electrical Engineering*. 2018; 65: 322-331.
[4] Shim K. Universal forgery attacks on remote authentication schemes for wireless body area networks based on Internet of Thing. *Internet of Things*. 2019; 6(5): 9211-9212.
[5] Hussain SJ, Irfan M, Jhanjhi NZ, Hussain K, Humayun M. Performance enhancement in wireless body area networks with secure communication. *Wireless Personal Communications*. 2021; 116: 1-22.
[6] Rahmani AM, NguyenGia T, Negash B, Anzanpour A, Azimi I, Jiang M, et al. Exploiting smart e-health gateways at the edge of healthcare internet-of-things: A fog computing approach. *Future Generation Computer Systems*. 2018; 78: 641-658.
[7] Kuzhalvaimozhi S, Rao GR. An efficient scheme for anonymous authentication using identity based group signature. *Fourth International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom2012)*. The Institution of Engineering and Technology; 2012.
[8] Lin X, Lu R, Shen X, Nemoto Y, Kato N. Sage: A strong privacy-preserving scheme against global eavesdropping for ehealth systems. *Selected Areas in Commun*. 2009; 27(4): 365-378.
[9] Djellalbia A, Badache N, Benmeziane S, Bensimessaoud S. *2016 Conference on Internetinal Technology and Secured Transactions (IJITST)*. Anonymous authentication scheme in ehealth cloud environment. Barcelona, Spain: IEEE; 2016. p. 47-52.
[10] Li T, Zheng Y, Zhou T. Efficient anonymous authenticated key agreement scheme for wireless body area networks. *Security and Commun Networks*. 2017; 2017(1): 1-8. Available from: https://doi.org/10.1155/2017/4167549.
[11] Liu J, Zhang Z, Chen X, Kwak KS. Certificateless remote anonymous authentication schemes for wireless body area networks. *Parallel and Distributed Syst*. 2014; 25(2): 332-342.
[12] Sudarsono A, Al Rasyid MUH. *2016 Seminar on Intelligent Technology and Its Applications*. An anonymous authentication system in wireless networks using verifier local revocation group signature scheme. Lombok, Indonesia: IEEE; 2016. p. 49-54.
[13] Zhu J, Ma J. A new authentication scheme with anonymity for wireless environments. *Consumer Electron*. 2004; 50(1): 231-235.
[14] Horn G, Preneel B. Authentication and payment in future mobile systems. *Comput Security ESORICS*. 1998; 98: 277-293.
[15] Yang C, Ma W, Wang X. Novel remote user authentication scheme using bilinear pairings. *Lecture Notes in Computer Science*. 2007; 4610: 306-312.
[16] Abi-Char PE, Mhamed A, Bachar E-H. A fast and secure elliptic curve based authenticated key agreement protocol for low power mobile communications. *The 2007 International Conference on Next Generation Mobile Applications, Services and Technologies (NGMAST 2007)*. IEEE ; 2007. p. 235-240.
[17] Zhang L, Tang S, Luo H. Elliptic curve cryptography-based authentication with identity protection for smart grids. *PLoS ONE*. 2016; 11(3): e0151253. Available from: https://doi.org/10.1371/journal.pone.0151253.
[18] Gebreyohanes MG, Asse AM. Adaptation mechanisms of camels (camelus dromedarius) for desert environment: A review. *Journal of Veterinary Science & Technology*. 2017; 8(6): 486. Available from: https://doi.org/10.4172/2157-7579.1000486.
[19] Sudarsono A, Al Rasyid MUH. *2016 International Seminar on Intelligent Technology and Its Applications*. An anonymous authentication system in wireless networks using verifier-local revocation group signature scheme. Lombok, Indonesia: IEEE; 2016. p. 49-54.
[20] Joshi A, Mohapatra AK. Authentication protocols for wireless body area network with key management approach. *Discrete Mathematical Sciences and Cryptography*. 2019; 22(2): 219-240.
[21] Tang J, Liu A, Zhao M, Wang T. An aggregate signature-based trust routing for data gathering in sensor networks. *Security and Communication Networks*. 2018; 2018: 1-30. Available from: https://doi.org/10.1155/2018/6328504.
[22] Mehmood A, Natgunanathan I, Xiang Y, Poston H, Zhang Y. *2014 IEEE International Advance Computing Conference (IACC)*. Anonymous authentication scheme for smart cloud based healthcare applications. IEEE Access; 2018. p. 33552-33567.
[23] Sun W, Cai Z, Liu F. *2017 International conference on e-health networking application and services*. A survey of data mining technology on electronic medical records. IEEE; 2017. p. 1-6. Available from: https://doi.org/10.1109/Healthcom40869.2017.
[24] Takyar A. *How does cloud computing impact healthcare industry*? LeewayHertz. Available from: https://www.leewayhertz.com/cloud-computing-in-healthcare/ [Accessed 20th March 2022].
[25] Red Hat Fuse. *Apache Camel Security*. Red Hat Customer Portal. Available from: https://access.redhat.com/documentation/enus/red_hat_jboss_fuse/6.2/html/security_guide/arch-architecture-camel
[26] Hossain MS, Muhammad G, Guizani N. Explainable ai and mass surveillance system-based healthcare framework

to combat covid-i9 like pandemics. *IEEE Network*. 2020; 34(4): 126-132.
[27] Yang G, Jan MA, Menon VG, Shynu PG, Aimal MM, Alshehri MD. A centralized cluster-based hierarchical approach for green communication in a smart healthcare system. *IEEE Access*. 2020; 8: 101464-101475.
[28] Raj J, Shobana S, Pustokhina I, Pustokhin D, Gupta D, Shankar K. Optimal feature selection-based medical image classification using deep learning model in internet of medical things. *IEEE Access*. 2020; 3: 58006-58017. Available from: https://doi.org/10.1109/ACCESS.2020.2981337.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

An Advanced VLSI Architecture For A Three-Operand Binary Adder For Both High-Speed And Area-Efficient

SINGAM SAI KIRAN
M.Tech student ECE , VLSI system design, Avanthi institute of Engg & Tech.
Dr.S. Kishore Reddy
Associate professor, HOD ECE, VLSI design Avanthi institute of Engg & Tech.
E mail : kishorereddy416@gmail.com
P.V.RAJU
Assistant professor, ECE Department, Avanthi institute of Engg & Tech.
E Mali: vijnatharaju@gmail.com

ABSTRACT

The utilization of a three-operand binary adder is employed for executing modular arithmetic in various cryptography and pseudorandom bit generator (PRBG) methodologies. The carry save adder (CS3A) is widely employed as the primary approach for performing three-operandaddition. The ripple-carrying stage (n) of the CS3A introduces a propagation delay of O. The critical route time can be reduced by employing a parallel prefix two-operand adder, such as the Han-Carlson (HCA) method, for three-operand addition. The process of three-operand binary addition is executed by employing an innovative adder design that is both high-speed and area-efficient. This design incorporates pre-compute bitwise addition, followed by carry prefix calculation logic, resulting in a significant reduction in adder latency to O(log2 n). The proposed architecture has been subjected to functional validation on an FPGA device and has been generated utilising a 32nm CMOS technology library that is readily available. In the caseof 32-, 64-, and 128-bit architectures, the recommended adder exhibited a performanceimprovement of 3.12, 5.31, and 9.28 times respectively compared to the CS3A after post- synthesis. The HC3B demonstrates superior performance in high-speed data processing due toits reduced spatial requirements, lower power consumption, and diminished delay when compared to the adder. Furthermore, it should be noted that the proposed adder exhibits loweraverage delay power (ADP) and peak delay power (PDP) compared to the existing three- operand adder techniques.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023
Keywords: ***carry save adder, FPGA, CMOS***

1. Introduction

Hardware multipliers rely heavily on multi-operand adders in order to calculate partial products. The use of multi-operand adders becomes important when performing multiplication operations that need the addition of numerous partial products. Due of the high powerconsumption in the multipliers and other arithmetic blocks, low-power electronics with low switching noise are required.

Due to the ability of inspecting operands for addition that might be either single bits or multiplebits, the adder's input and output can be in multiple bits [3]. To more directly depict a multi- operand adder, where partial sums are compressed and carry is less widely propagated, compressor trees may be used. In this work, many different kinds of multi-threaded arithmetic(MTA) are used. These include the Array tree adder, Wallace adder, Balanced delay tree adder,and Overturned-stairs adder. Despite its high power consumption and processing lag, adders are crucial in arithmetic-functioning machines. Adders are also used in multipliers, another component of resource-intensive arithmetic circuits.

Quick adders, sometimes known as other adders, are faster than the ripple carry adder (RCA) in terms of latency. However, they often have a bigger surface area and greater energy needs. The RCA, on the other hand, has a smaller footprint and lower power requirements, but it also has a longer latency. It is important to remember, however, that systems with a high number ofoperands often have resource constraints.

2. Existing Work

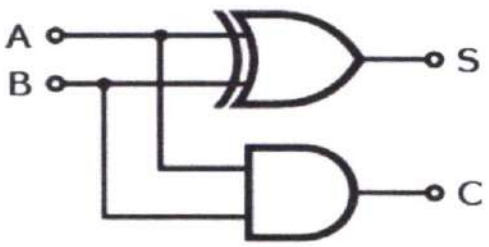
No significant effort towards delay refinement of RCA-BTA has been documented in the existing literature. Therefore, the critical route delay analysis is provided [5] to investigate thepotential for delay minimization of the RCA-BTA structure. Most

of the suggested work in theliterature is geared at bettering the design metrics of fast adders, which in turn improves the performance of the WTA architecture.

2.1 Adder Types

2.1.1 Half Adder

The half adder is used to perform the addition of A and B. These results are S and C (the valuethat will theoretically be carried over to the next addition), both of which are produced by the method. The sum is 2C plus S at the end. The right half-adder arrangement uses an XOR gateand an AND gate to process S. By connecting the carry outputs of two half adders with an ORgate, a full adder may be created.



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 1: Half Adder

2.1.2 Full Adder

A full-adder may multiply a binary number by 8, 16, 32, or even more digits. The usual notation for the circuit's two-bit sum at the output is Cout or S. The following is the truth tablefor a complete adder with one bit.

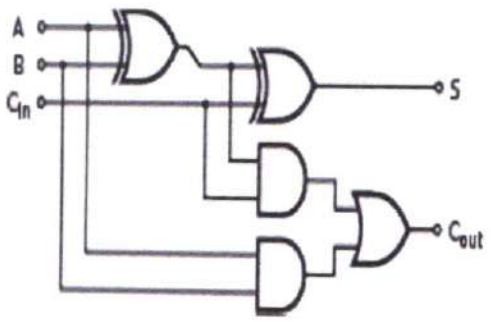


Figure 2 : Implimentation Of full adder

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

2.1.3 Ripple Carry Adders (Rca)

Ripple carry adder of N bits is created by concatenating N complete adders. The result of one full adder is sent into the input carry of the next full adder in this implementation. The followingequations are used in the computation of sum and carry. By bouncing from one full adder to the next, carry takes the longest critical route and experiences the most severe delay. Si = Ai *Bi * Ci

Ai + Bi + (Ai + Bi) Ci + 1. Where i is an integer between zero and n minus one

Although it takes the longest amount of time to add (O (n) time), RCA takes up the least amountof space (O (n) area). The delay of a ripple carry adder with N full adders chained together is 2N gate delays from Cin to Cout. The adder's latency grows proportionally as the number of bits rises. Figure shows an RCA block diagram.

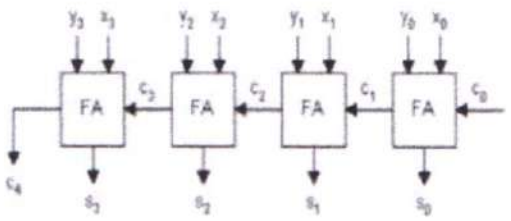


Figure 3: Block diagram of RCA

2.1.4 Carry Save Adder

In computer microarchitecture, a carry-save adder is used to compute the sum of three or morebinary data of n bits.

It's elementary school maths: "8+1=0, carry 1," "7+2+1=0, carry 1," "6+3+1=0, carry 1," and so on. By carrying the carry from one digit to the next during the calculation, we may have a better idea of the initial digit of the result. Adding two numbers of the same length will take time proportional to n if the computer can do several calculations simultaneously. In electrical

terms, using bits (binary digits), a carry must propagate from one end of a number

to the other,taking time proportional to n if we have n one-bit adders. We won't rest until this is resolved, Fifth, we have no idea what the ultimate verdict will be.

6) We can't say if the sum is more than or less than a certain value (or even whether it's positiveor negative).A carry look-ahead adder has the potential to decrease the delay. However, the propagation delays increase as n increases because the distances signals must travel on the device expand in proportion to convey look-ahead. This is no longer the true, however, for really large numbers. Carry look ahead is mostly useless for public key cryptography, which needs integersizes between 512 and 2048 bits.

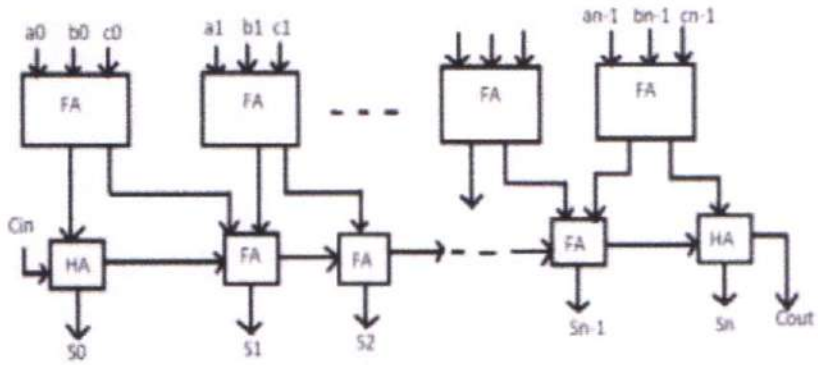


Figure 4: Carry Save Aadder

It is common custom to use either one three-operand adder or two two-operand adders when carrying out a binary addition with three operands. However, it is also possible to utilise a single two-operand adder. [2] The carry-save adder is a tool that is ideal for mathematical computations because of its small size and portability. The three-operand binary addition is a variation of the regular arithmetic that is used in cryptographic algorithms and PRBG approaches. On IoT-based hardware devices, the performance of MDCLCG and other alternative encryption algorithms is negatively impacted because CSA has a longer ripple-carrystage carry propagation delay. It is possible to use the Carry Save Adder to add together valuesof any size, ranging from 3 bits all the way up to n bits. The CSA and the Full Adder are equivalent to one another. Instead of the other adder, the partial product terms for each clusterwill be added using CSA. When compared to the CSA approach, using

an alternate adder takesmuch more time. More than two numbers will need to be added together in a lot of different situations. The addition of the first two numbers, each of which has n bits, is the quickest and easiest technique to merge m numbers. And so on, until each of the three is in equilibrium. If

the gate delay is O (m log n), then an adder tree that has O (log m * log n) additions will needto be constructed. Using carry-saving augmentation might potentially lower the amount of timeneeded to complete the job in half.

It is possible to use a parallel prefixed two-operand adder like the Han-Carlson (HCA)[3] in order to cut down on the essential route time required for performing three-operand binary addition. We may be able to reduce the critical route latency by O(log2 n) if we increase the area by O(log2 n), and the same is true in the other direction. Therefore, a potent very large scale integration (VLSI) architecture is necessary in order to do the rapid binary addition whileemploying relatively simple hardware. This study introduces a novel high-speed area-efficientadder approach that employs pre-computed bitwise addition followed by carry-prefix calculation logic to accomplish the three operand addition. In contrast, the HCA-based three operand adder (HC3A) consumes less gate area and minimises propagation latency. This technique was developed to conduct the addition of three operands. The suggested Verilog HDL adder design is synthesised using a 32nm CMOS technology library that is available forpurchase commercially. The one-of-a-kind adder technique is put to the test, after which it is contrasted with the tried-and-true CS3A and HC3A approaches to adding three operands. In order to shorten the time required for the crucial route, it is possible to make use of a parallel prefix two-operand adder that has two stages. According to the findings of the study, the methods that are the most efficient for adding two operands together are logarithmic prefix adders and parallel prefix adders. There are a total of six unique topologies for these adder techniques, and they are referred to as the Brent-Kung, Sklansky, Knowles, Ladner-Fischer, Stone (KS), and HanCarlson (HC) topologies, respectively. When n is more than 16, Hanlon and Carlson emerge as the most efficient of the three methods.

Using the Han-Carlson adder, it is possible to carry out a three-operand addition in

two separatestages, as seen in Figure. (HCA).

The blueprint for the three-operand version of the HC3A (HC3A) is quite detailed. The numberof black-grey cell stages that represent the length of the PG logic chain that the Han-Carlson adder makes use of.

3. Proposed Method

Integrated circuits are in danger of losing their field dependability as a result of increases in integration density and process shrinkage. It is essential for mission-critical systems such as server-class computers and embedded devices to have error detection that runsin parallel. Due to the fact that adding is the initial step in any computation, many adders finda home in extremely large size integrated circuits. Any erroneous output may be recognisedby a comparison of two internal values included inside the carry select adders. It has been proposed in the past that concurrent error detecting adders may be used; these adders are able to recognise wrong outcomes from a single mistake. On the other hand, it is not always easy to identify a flawed product that is the consequence of a confluence of problems. If a second faultoccurs before the first fault is discovered as a result of the detection of an erroneous output, then the capacity to identify concurrent errors may be compromised or lost entirely. Finding the first flaw before the second one is necessary in order to have error-free adding machines. Because of this, the simplicity with which a failure in a concurrent error detecting adder may be recognised during maintenance, a reboot, or even during operation is of the utmostimportance.

3.1 Multiple Block Selection Adder, Size

In Figure 5, you can see a straightforward structure for an n-bit multi-block carry select adder.Its outputs are the carry output cn and the sum S: [sn1.. s0], while its inputs are the agehend X:[xn1.. x0] and the addend Y: [yn1.. y0]. It is composed of several little b bits. Block 0 is the name given to the first part of the series. Let's assume the kth block, which we'll refer to as blockk, has a bit width of nk. Every nk has the potential to be different from the others. Carryinformation is included in both the input cink and the output coutk of blockk. A row of full adders that executes a ripple carry addition on n bits makes up block0. An incrementer (INC) and a half adder (HA) are included in the construction of each full adder seen in the figure. A

binary value consisting of just two bits plus a carry bit is input to an INC, and the resulting sumis output as a binary number consisting of only two bits. Each of the remaining blocks consistsof a row of 2:1 multiplexers (MUXs), a row of HAs, two rows of INCs (INC0 and INC1), anda row of INCs (INC0 and INC1). The gatelevel designs for the HA, INC, and MUX gates maybe seen in Fig. 5(b). INC0 and INC1 in each block, with the exception of block0, calculate two alternative sum results. One of these outcomes is based on the assumption that the carry inputcink is 0, and the other is based on the assumption that cink is 1. The row of MUXs selects the correct one. In this abbreviated form, a signal name that has two subscripts specifies, respectively, the block index and the position inside the block. The xk,j and yk,j representationsof the input bits at position j in blockk are written as (0 j nk). Where l = j + Pk1 m=0 nm, xk,j
= xl. The column of INCs to which a signal belongs is indicated by the superscript that is placedafter the name of the signal. It might also be expressed as s 0 k,j (0 j nk), where j represents theresult of running INC0 at position k in blockk. The carry signals for bit j 1 are indicated by thenotation c 0 k,j and c 1 k,j, respectively. These signals are referred to as INC0 k and INC1 k. The ranges [xk,nk1.. xk,0] and [yk,nk1.. yk,0] serve as Blockk's inputs, while the range [sk,nk1.. sk,0] serves as Blockk's output range.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

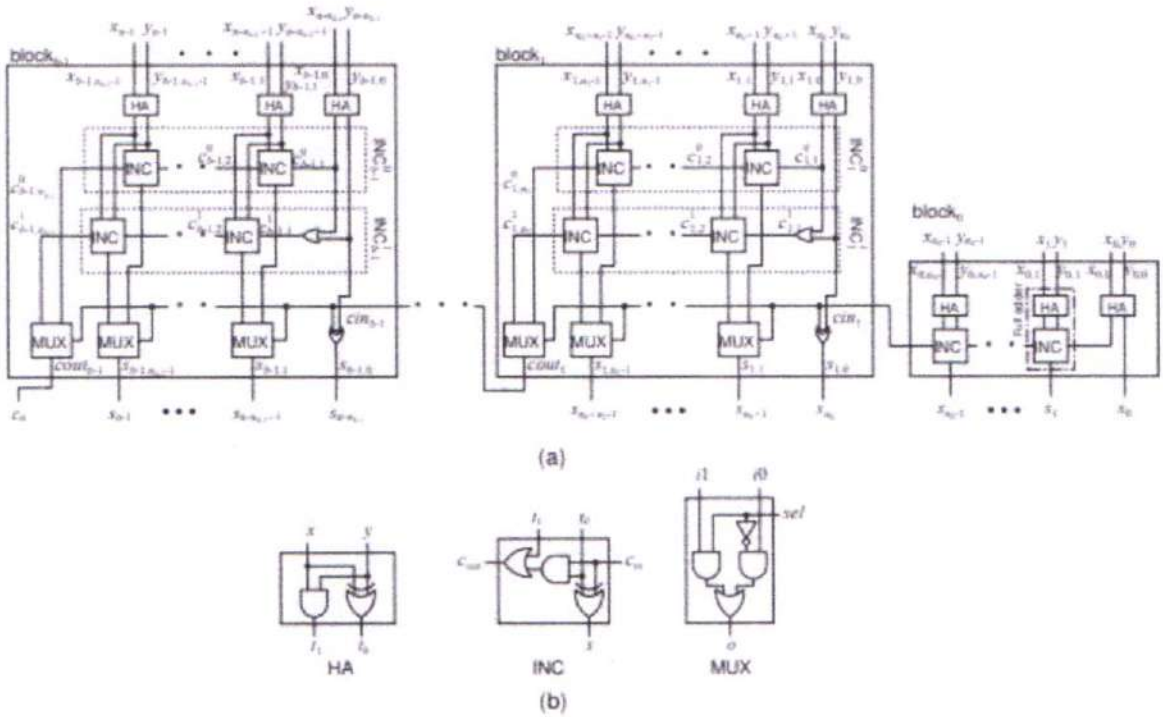


Figure 5: Multi-block carry select adder (a), and the gate-level designs of HA, INC and MUX (b).

3.2 Capability to Identify Problems in Parallel Operations

One stuck-at fault in an INC' or its ascendant HA' never affects both the total output and one of the two carry signals at the same time, as stated in Section 3.1. Since only a single stuck-at fault may exist inside an INC' or its parent HA', this is the situation. This means that (1) the sum signal of the INC', (2) one of the carries of the INC', or (3) all three signals (the two carriesand the total) will be affected by a fault in the INC' or its ascendant HA'. By comparing the expected parity pS with the actual parity S and the values of cn and c ′ n, we may assess whether

or not an error was caused by a fault. The first case involves using one of INC's two carry signals for the addition operation and the other for parity prediction. Errors in the parity prediction carry signal only affect one bit of the parity prediction carry bits, hence the final tally is unaffected. Incorrect results caused by the flaw may then be identified and corrected. Let ck,j represent the carry that is affected by the fault that occurred at an INC' when the carrysignal for addition is erroneous. A defect at an INC' has an effect on the carry, denoted by ck,j.If the problem affecting ck,j does not propagate to other nodes, it will be uncovered when it causes a second error in

the total signal, sk,j. The reason for this is because the faulty carry signal is not being used for parity prediction. However, errors will be introduced into the q sumsignals sk,j+1, sk,j+q if the incorrect value of ck,j is passed on at q consecutive carry signals. This happens because ck,j is being incorrectly propagated. So, the wrong answer is the sum signals sk,j, sk,j+1, , sk,j+q. Here, the q carry signals c ′ k,j+1, , c ′ k,j+q are also incorrect because the logic used to generate them is the same as that used to generate the ck,j+1, , ck,j+q,and both use the same carry inputs (ck,j, ck,j+1, , ck,j+q1). Signals for q+1 sum sk,j, sk,j+1, and sk,j+q, as well as q carry c′ k,j+1, and c′ k,j+q, will be off as a result. Therefore, we will use q incorrect signals to determine the expected parity (pX pY) (pCb1 pC0), and q+1 incorrectsignals to determine the overall signal parity. Each of these two parities will be different fromthe other due to the one variation in the total amount of erroneous signals used in each computation, allowing the error to be pinpointed. In the second case, the total result is not the same as the right one since a bit of the sum result was flipped. However, the calculated parity is correct since all of the carry bits used to make the prediction were correct. The impact of a mistake may be determined by comparing the predicted and actual parities of the final outcome.In the third instance, the INC'-derived total bit and all of the carry bits would be incorrect. Theacquired sum bits and carry bits used for parity prediction in the upper locations do not conflictwith one another, with the exception of the position of the flawed INC'. This is because it has been shown that both carry bits are incorrect. Even if the parity prediction carry bits are correct, the total bit from the INC' will be inverted because of the lower bits. Consequently, the expected and actual levels of equality are not the same. The adder has two carry inputs, cink and cin' k, one for each adder block. If the cink is wrong, then the sk,0 will be wrong as well. The error on cink may also lead to problems with subsequent sum outputs (say, q additional sum outputs). It will also lead to errors at the q carry signals c ′ k,i, much as the explanation provided in scenario 1. As a result, there will be q + 1 incorrect sum outputs and q incorrect carry signals c ′ k,i, both of which will be identified for the same reasons as in instance (1). When performing an XOR or MUX' operation, only one of the sum bits, the carry bit, or the projected parity is altered. Therefore, the effect of an error in them may be determined by comparing the projected parity with the parity and by comparing the two carry outputs of the

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

adder. Keep in mind that if one of the input operands does not match its parity input, the projected parity may be off. This occurs because the parity input is used to make parity predictions. As a result, it is possible to find contradiction between X and pX or between Y andpY even if the adder is error-free. This is so because it is possible to verify these discrepanciesseparately. As can be seen in Figure 3, the proposed adder is well-suited for usage in systems that conduct parity-based error detection. Real-world designs like [21] and [22] make use of arithmetic circuits with parity-based error detection. The adder's expected parity is utilised forthe result's parity bit, while the parities of the operands (pX and pY) are read from memory ora register file and used to perform the addition. By monitoring the system's parity checker and comparing the adder's cn and c ′ n carry outputs, one may ascertain whether or not the adder has generated a faulty result.

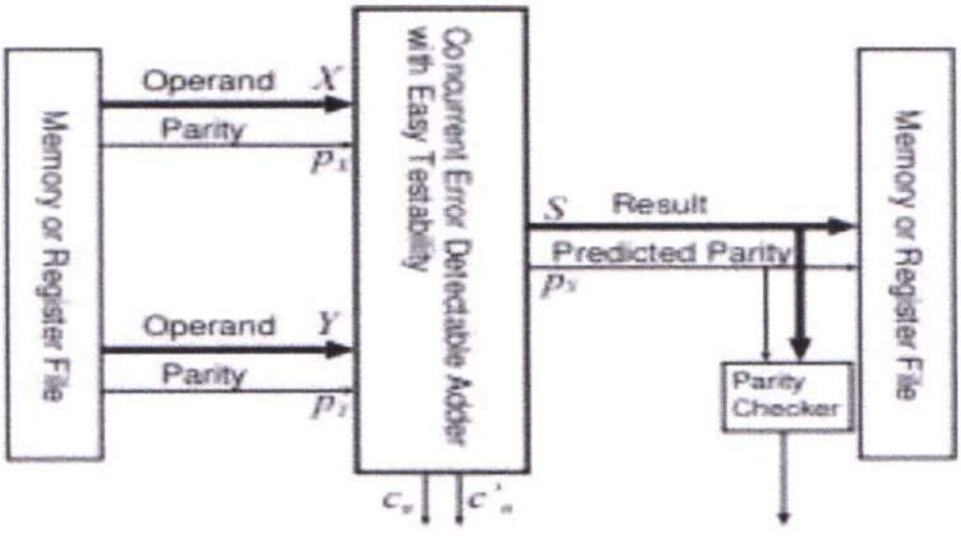


Figure 6: Example of a datapath circuit with the proposed adder in a system using parity- based error detection

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

TABLE 1
Input test patterns for block$_0$.

Pattern	$x_{0,j}y_{0,j}$	
	$j \geq 1$	$j = 0$
t_0	01	11
t_1	11	11
t_2	10	10
t_3	00	11
t_4	11	01
t_5	01	11
t_6	11	00
t_7	00	11
t_8	00	11
t_9	00	00

TABLE 2
Input test patterns for block$_k$ ($k \geq 1$) shown in Fig. 2(b).

Pattern	$x_{k,j}y_{k,j}$		cin_k
	$j \geq 1$	$j = 0$	cin'_k
t_0	01	11	0
t_1	11	11	0
t_2	10	10	0
t_3	00	11	0
t_4	11	01	0
t_5	01	01	1
t_6	11	11	1
t_7	10	00	1
t_8	00	01	1
t_9	00	00	1

4. Hardware Requirements

"Very Large Scale Integration" is the abbreviation for VLSI. This is the area of study concerned with cramming ever more logic devices into ever smaller spaces. With very large scale integration (VLSI), circuits that formerly required many boards are now able to fit into an area only a few millimetres wide. There is now a great chance to accomplish goals that werepreviously impossible. Everyday items like computers, cars, smartphones, and even cutting- edge digital cameras all use VLSI circuits. We'll examine how extensive knowledge in severalsubfields of the same topic is required for all this in the next chapters. While very large scale integration (VLSI) has been around for some time, developments in computing have led to a huge increase in the number of tools available for designing VLSI circuits. Additionally, IC capabilities has risen dramatically over time in terms of computing power, utilisation of available space, and yield in accordance with Moore's law. Thanks to the confluence of these two developments, novel ICs with a wide range of capabilities are now within reach. The proliferation of tiny computer devices, such as those found in embedded systems and ubiquitous computing, means that

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

even the shoes you wear may one day do valuable tasks, such as monitoring your heartbeats.

There are three types:

1. Analog:

2. Amplifiers, Data converters, Filters, Hase Locked, Sensors, etc., that need a high degree ofaccuracy yet have a low transistor count.

2. Application-oriented integrated circuits (ASICS)

Improvements in IC manufacturing have allowed us to pack more and more powerful circuits into ever-tinier packages. Because of this, we can fit a greater amount of functionality into thesame footprint. The primary use of this skill is in the creation of ASICs. These integrated circuits (ICs) are purpose-built, meaning they are designed to do a single task very well. Digitalsignal processing (signal filters, picture compression, etc.) is where you'll most often see this used. To put it simply, a digital wristwatch typically consists of a single IC doing all the time-keeping tasks, in addition to other functions like games, calendars, etc.

3. Systems-on-a-chip (SOC):

These mixed signal circuits (digital and analogue on the same chip) are quite sophisticated. Anexample of a system on a chip is a network processor or a wireless radio chip.

4.1 VLSI's Benefits

While our focus in this book will be on ICs, it is important to note that the capabilities and limitations of ICs heavily influence the design of the larger system. There are several essentialways in which integrated circuits enhance system features. When compared to digital circuits made of discrete components, ICs provide three main benefits:

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

• Size. In contrast to discrete components, which may be as large as millimetres or centimetresin size, integrated circuits include transistors and wires that are just micrometres in size. Since smaller components have less parasitic resistances, capacitances, and inductances, they are faster and use less power than their larger counterparts.

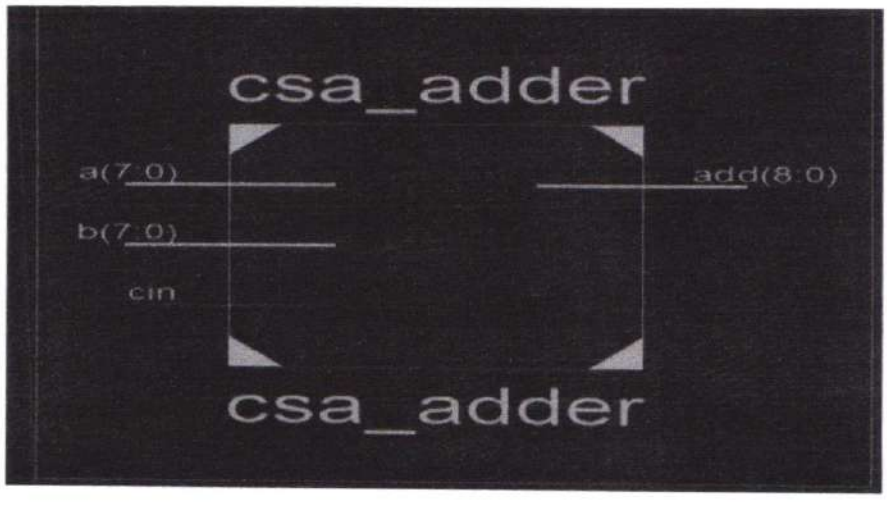
• Speed. Within a chip, it is significantly faster to flip a signal from logic 0 to logic 1 than it isto do so across chips. Internal chip communication may be several orders of magnitude quicker

than inter-chip communication on a PCB. Smaller components and connections mean less parasitic capacitance to slow down the signal, which is why circuits on a chip can operate at such fast speeds.

The use of energy. Within a semiconductor, logic activities use far less energy. Again, smallercircuit sizes on the chip are mostly responsible for the reduced power consumption; circuits with smaller sizes have fewer parasitic capacitances and resistances, respectively.

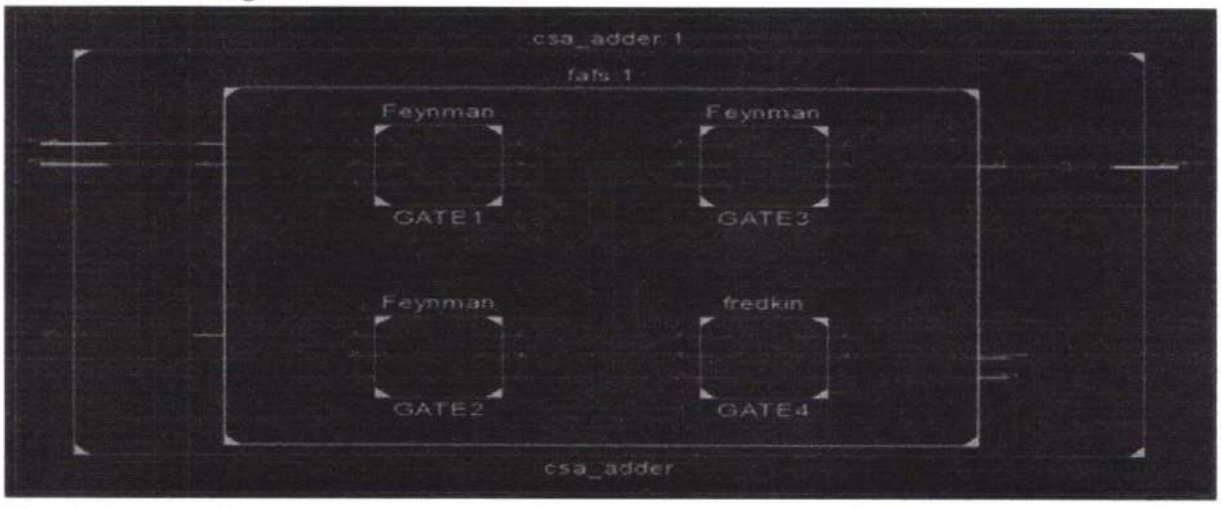
5. Simulation Result

RTL:

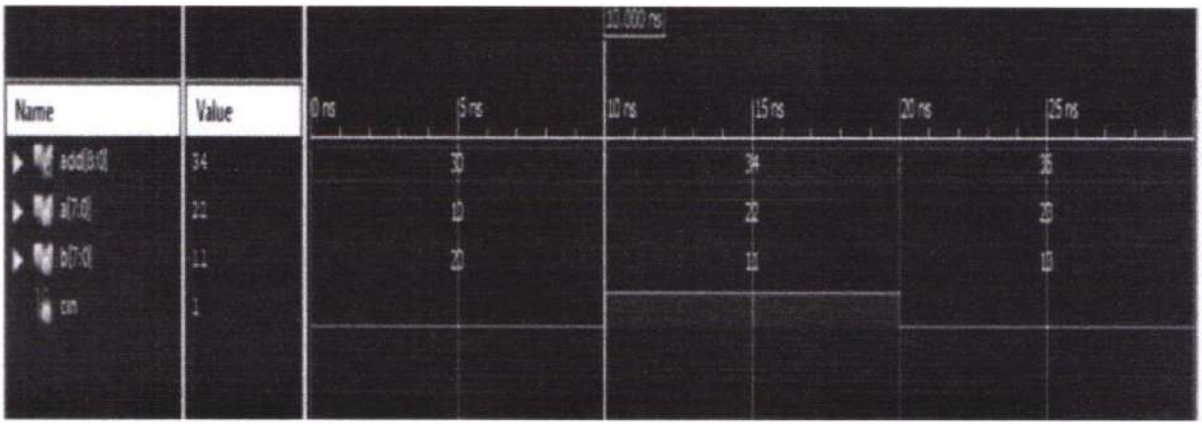


Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

Internal Block Diagram



Simulation Results:



Conclusion

This research presents a high-speed, area-efficient adder strategy and related VLSI architecture for computing modular arithmetic for use in cryptography and PRBG applications. In this method, the addition of three input operands is computed concurrently using a four-stage prefix adder. The suggested architecture is smaller overall due to the elimination of unnecessary prefix calculation steps in both PG logic and bit-addition logic. The idea of the hybrid Han-Carlson two-operand adder (HHC2A) is expanded upon in the hybrid Han-Carlson three-operand adder (HHC3A) design. Similar to the suggested adder design, the Kogge Stone hybrid Han-Carlson three-operand adder is written in Verilog HDL. All of these devices' core area and delay timing are synthesised using the Spartan 3 technology library. For better area and latency performance, we implemented our adder in the FIR filter's adder section. By considering both area and delay, we determined that our adder was the best option.

References

[1] M. M. Islam, M. S. Hossain, M. K. Hasan, M. Shahjalal, and Y. M. Jang, " FPGA implementation of high-speed area-effificient processor for elliptic curve point multiplication over prime fifield," *IEEE Access*, vol. 7, pp. 178811–178826, 2019.

[2]Z. Liu, J. GroBschadl, Z. Hu, K. Jarvinen, H. Wang, and I. Verbauwhede, "El liptic curve cryptography with effificiently computable endomorphisms and its hardw are implementations for the Internet of Things," *IEEE Trans. Comput.*, vol. 66, no. 5, pp. 773–785, May 2017.

[3] Z. Liu, D. Liu, and X. Zou, "An effificient and flflexible hardware implementation of the dual-fifield elliptic curve cryptographic processor," *IEEE Trans. Ind. Electron.*, vol. 64,no. 3, pp. 2353–2362, Mar. 2017.

[4] B. Parhami, *Computer Arithmetic: Algorithms and Hardware Design*. New York,NY, USA: Oxford Univ. Press, 2000.

[5] P. L. Montgomery, "Modular multiplication without trial division," *Math. Comput.*, vol. 44, no. 170, pp. 519–521, Apr. 1985.

[6] S.-R. Kuang, K.-Y. Wu, and R.-Y. Lu, "Low-cost high-performance VLSI architecture for montgomery modular multiplication," *IEEE Trans.Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 2, pp. 434–443, Feb. 2016.

[7] S.-R. Kuang, J.-P. Wang, K.-C. Chang, and H.-W. Hsu, "Energy-effificient high-throughput montgomery modular multipliers for RSA cryptosystems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 11, pp. 1999–2009, Nov. 2013.

Applying Hidden Markow Models to Ontology Based IRS for Coherence

[1] Dr Shahebaz Ahmed Khan, [2]Y DurgaJhansi

[1]Avanthi Institute of Engineering and Technology, Hyderabad,
[2]Narayana College, Hyderabad
[1]sakklkyr@gmail.com

Abstract

Abstract: *An Information retrieval model occupies a vital position in information extraction platforms. Information retrieval helps the users to retrieve and extract the information from unstructured data sets. It has a set of fast algorithms capable of facilitating the relevance of the documents displayed for the queries searched. To efficiently acquire the documents, the domain based ontology works as more suitable option. Ontology based information retrieval systems can form the information index and also the index of information inference. Ontology based IRS is found with many function in comparison to keyword based retrieval models as these systems neglect the semantic information. Ontology based information retrieval systems sometimes suffer the problems of inaccurate index term frequency. This paper suggests the application of Hidden Markow Models (HMM) to ontology based IRS which can probably provide the ways to form the efficient index with coherence between the terms of the documents for the search query. Hidden Markow Models can help in better conceptualization of the documents for relevancy.*

Keywords: *HMM, ontology, semantic information, index terms, information inference.*

1. Introduction

An Information Retrieval System (IRS) is highly potential software for information retrieval. Information retrieval is a process of extracting the relevant data or documents from the large sets of unstructured data. Information Retrieval Systems can store, organize, evaluate and retrieve the documents from the unstructured data repositories. These systems are particularly meant for extraction of the information from the textual data bases. IRS selects and retrieves the suitable documents for the user queries by applying a matching function with some retrieval status value in return for each document in the collection. Based on type of the data it uses various models, user interaction language, and search methods for the display of the relevant information. There have been probabilistic models, Boolean models, VSMs, binary and non binary independence models to retrieve and represent the relevant information for the user query [1]. These models do not consider the internal relations between keywords and documents but will retrieve the results based on probabilistic estimations.

Due to the data accumulation and acquisition, here is a demand for high quality retrieval of documents to improve and match relevancy. The traditional methods of information retrieval are not suitable options and cannot meet the needs of task relevant high quality results. So, to improve the efficiency and accuracy of the results, ontology based information retrieval can be used. Ontology has a mark in promoting and representing the knowledge and information. Ontology based information retrieval systems can be found with more options of functions than classical keyword based information systems which can be helpful to provide the resultant documents to the query passed by the users. The concept in domain ontology considers a relation to other concepts simultaneously [2]. The use of ontology in information retrieval can conceptualize the information based on the semantic order which can be a need of user's personalized queries. Ontology based models of information retrieval can process the useful information from the unstructured textual information by establishing the mapping between the document terms and the domain concepts.

Hidden Markov Models are types of Markov Chains which constitute a finite state automaton with edges between any pair of states that are tagged and labeled with transition probabilities. Hidden Markow Models can evaluate, decode and can classify the most likelihood of data. These can explain and derive the probabilistic events of random process of document query search evaluation. The HMM can be combined with ontology based strategies to further improve the efficiency and accuracy of the search results in document retrieval. The application of HMM can boost the term distributions for the document search. Our work is a proposal to experiment the ontology based retrieval by applying the Hidden Markow Models so as to generate the information sequences of complex probability distributions. This application of Hidden Markow Models on ontological information can conclude the quality of the knowledge source by deriving well defined and more semantically related document terms for a document query. This proposed approach can be experimented with domain experts using the HMM.

2. Ontological IRS

Ontology based Information Retrieval System is a non classical IR model. It is a theory that concerns kinds of abstract entities which are to be admitted in any language system. Ontology can be an informal conceptual system and it is a philosophical discipline which takes the shape of formal semantic account. Ontology is a representation of some conceptual system using the logical theories. There can be different forms of ontologies. The classification of ontologies is based on two constraints, the first is by the type of the information they capture and by the internal structure richness. There can be

a) Top Level Ontologies/ Upper Level Ontologies

b) Domain Ontologies

c) Task Ontologies

d) Domain Task Ontologies

e) Method Ontologies

f) Application Ontologies

There are also linguistic ontologies whose origin is natural languages and these describe semantic constructs rather than modeling a specific domain. The linguistic ontologies use the words as grammatical units and can be used for natural language processing and generation. Ontologies conceptualize the information by representing the information in the form of knowledge via reasoning and logical relations which further allows finding the new knowledge from the existing one. It has consistency checks to validate the obtained knowledge. The process of developing ontology requires knowledge acquisition from any relevant sources [3]. There are several possible sources of knowledge: domain experts or unstructured, semi-structured, and structured sources.

2.1 Ontology in Information Retrieval

Implementation and design of the information retrieval system constitutes two parts; the first is document processor and the second is document retrieval. In ontology based information retrieval model, an ontology server is added to tags and it forms the indexes to the retrieval sources based on ontology; later the query conversion module implements semantic processing in users' need and expands the initial query on its synonym, hyponym, and its senses. The retrieval agent module uses the conversion of queries for retrieving the information source. One way of introducing the external knowledge into information retrieval is by using fixed vocabularies in controlled indexing [4], for example we can use the instance of keywords which can reflect the knowledge about the domain. The concept in domain ontology has a relation to other concepts simultaneously. Ontology theory is applied as the base of semantic representation to represent user need and document semantics. Domain ontology is the detailed description of domain conceptualization which expresses the abstract objects, relation, and class in one vocabulary set. The figure no 1 gives the ontology with ISA relationship.

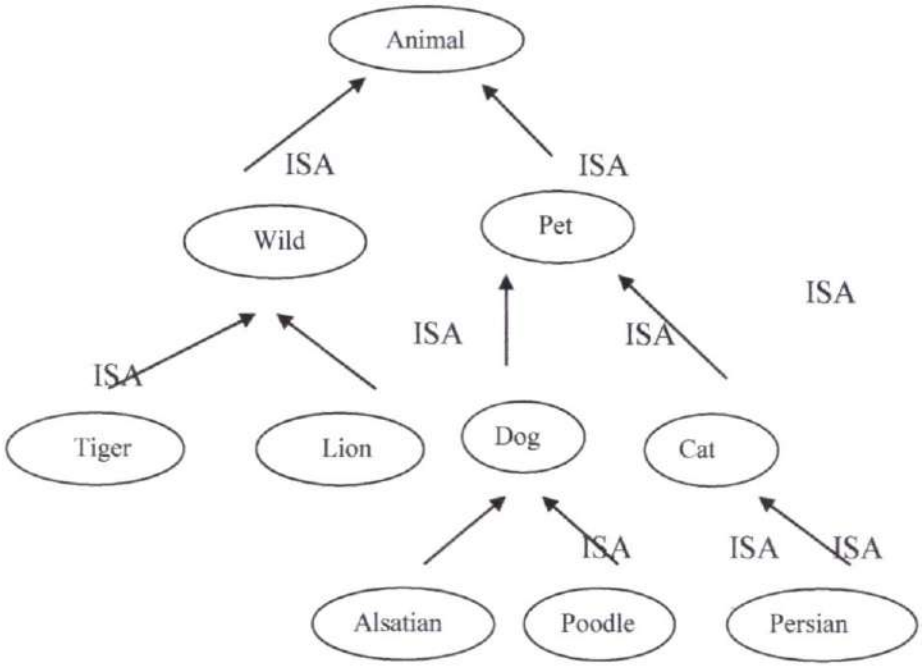


Figure No1: Ontology with ISA relation

In ontological IRS, the concept inclusion relation can be mapped based on the two factors namely generalization and specialization [5]. To match and find the similarities, distance is measured by assigning some weights to the nodes. Distance can be measured from the path length to express similarity. The recall ratio and precision ratio of ontology based Information Retrieval Systems are higher than that of the information retrieval models based on keyword at a certain extent. A semantic retrieval system based on the domain ontology, aims to achieve higher efficiency than keyword based search engines.

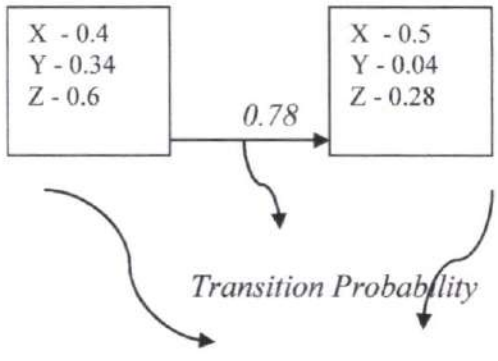
3. Hidden Markow Model (HMM)

Markow Models are based on markow chains. A markow chain is a random process which has some finite set of states, where the current state goes to the next state. Markow chain models are the simplest methods which can model the sequential data.These are useful in data base search and retrieval. Markow chains tell about the sequences that appear in random variables of states. A Markow chain gives the probability of occurrences of states in discrete states [6]. Markow models predict the future states based on the observations on the past. This means whether a state 'S' can be state 'S_n' in future depends on the known facts and states of the past like (S_n, S_{n-1}, S_{n-2}, S_{n-3}..... S_{n-n}).

To estimate the probability 'P' of these states i.e, $P(S_n|S_{n-1}, S_{n-2}, S_{n-3}..... S_{n-n-1})$ the Markow model considers the past states for simplifying the assumptions [7]. The

Markow models calculate the transition probability (the probability which is the change in one state to another state takes place).

Hidden Markow Models are statistical models where the systems which are to be modeled are assumed to be Markow process [8]. A Markow process is a memory less process with hidden states where its future and past states are independent. In Hidden Markow Models, non observed factors influence the transitions/probabilities. HMM considers the non observed factors or states into account. Here, there can be two or more than two chains. One chain can be obvious chain of 'observed states' and another chain can be a chain(s) of 'non observed states'. The Hidden Markow Models take not only the transition probability but also emission probability (it is the probability value associated with each symbol in each state. There are different Markow Models like Hidden Markow Models, Non-Homogeneous HMM, Mixture HMM and Non-Homogeneous Mixture HMM. The HMM are used in the situations where the data is infinite. Viterbi algorithm is an example for HMM.



4. Framework and Methodology

Ontology based Information Retrieval Systems can extract knowledge from knowledge sources by considering symbolic, statistics and multi strategies. To improve the working efficiency of ontological IRS, we have proposed a framework based on Hidden Markow Models. In this work, the idea is to deploy the concept of Hidden Markow Models on the existing ontological retrieval systems so as to conceptualize the terms of the documents which are more relevant to the user defined query. In this model, the user query whenever it is submitted, then the following procedure falls in execution.

The search words or phrase input from the user is accepted by the user interface; the system prunes the function words of the input phrase and generates the stop list by reserving the nouns and verbs. From this, the semantically conceptual phrases and words are determined by term extraction implementation. The query transition module accepts the input as progressed and sends the consequent result to the ontology server so as to determine the semantically related conceptualized meanings such as synonyms, hyponyms, hypernyms etc. Later the query transition module searches and forms the

semantic judgments to match the concepts in domain ontology data base. Before the information is extracted, this model implements the semantic analysis of words of the user query and checks whether the words found with the user request belongs to the ontology knowledge base or not. Further semantic reasoning and logical evaluation is performed by the evaluation engine to obtain the suitable documents of request. Whenever the suitable words for the query are not available, then the user query is adjusted by sending a return statement to the users for better results [9]. Due to this there is no certainty of obtaining at least the 'far distance relevant results'. In such cases of user adjustment of the query, there can be burden on the search process and so here we can deploy and apply the Hidden Markow Models on the conceptualization of the terms of the ontology database.

After semantic analysis on the user request, the Markow Models can predict the probable words which can suit the query of request. In this theme of retrieval, the goal is to find the sequence of hidden states (words those whose meaning is not found in ontology data base but match the user query and are similar in meaning and fall with long distance in semantic analysis). The word relationships are transformed into states and these states have the greater probability to produce the observation sequence that is searched. The string or the term that matches and which is relevant to the user query can be translated as most probable term sequence for the query words. The ontology is defined in such a way that the words are lexicon specific and trained with some model for the Hidden Markow probability estimation. The proposed framework is shown in figure no 2

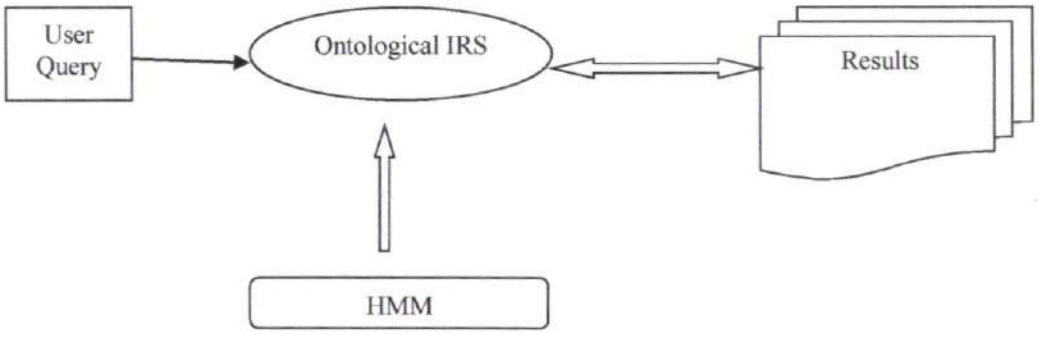


Figure No 2: HMM Based OIRS

4.1. Discussion

We denote and calculate the paths 'P' to the number of specializations s(P) and number of generalizations g(P). The similarity is considered by transforming the ontology into a directional weighted graph with downward weights and upward weights. After transforming the ontology into weighted directional graph, the immediate specialization and generalization similarity values are taken into count. The weighted

shorted path is measured to find the similar concepts those which match the user query request. To avoid the zero probabilities to the terms which do not occur in the training data, the Hidden Markow Model is applied on the ontology to detect the unobserved terms for the documents.

The statistical evaluation of HMM reflects and corresponds to the terms which are hidden and do not occur in relationship of coherence in the ontology database. The HMM can perform the smoothing of the words to close the distance gaps, later these models filter the conceptualized words by analyzing new observation sequence and then predict the most closely matching and less least distanced words for the relevant document retrieval. This can improve the precision and recall ratio due to which the relevancy retrieval is obtained. After applying HMM on the ontological database, the framed relationship probabilities are as follows in figure no 3.

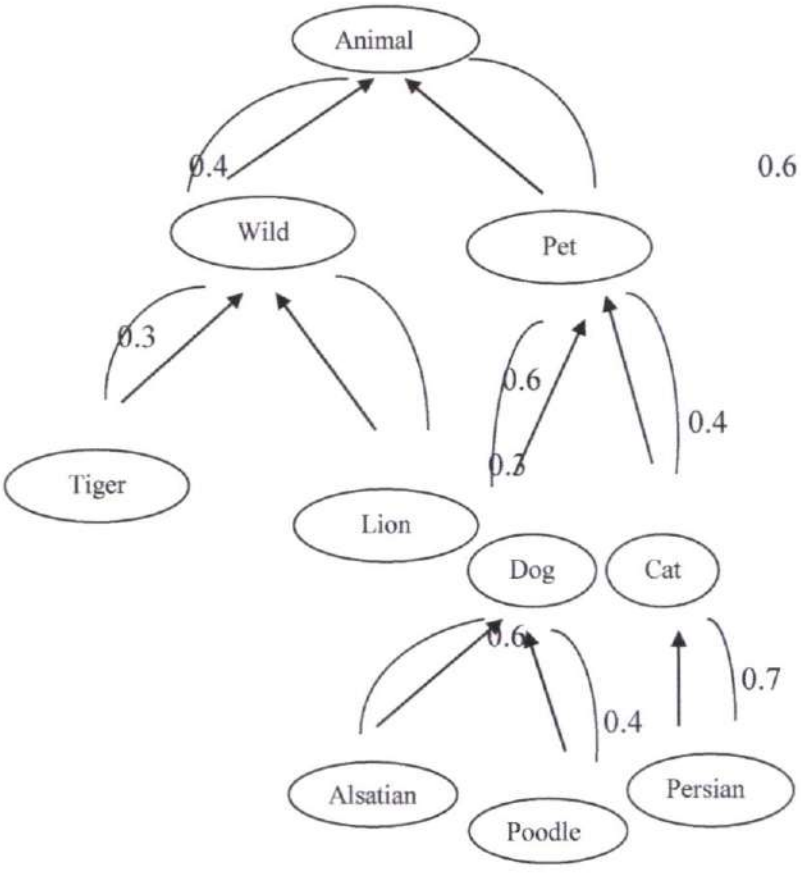


Figure No 3: HMM Probabilities to OIRS

In order to operate the query results effectively, the ranking can be scored based on the probabilities obtained by HMM through the sequence of non observed word semantics. The probabilities will show the degree of match between the search terms and the semantic type of information resource. This ontological model when applied HMM can obtain the more relevant and related information because it includes not only the

relationship matching but also, the estimated probabilities which can show the maximum similarity for the words in the documents.

5. Conclusion

In this paper, we have proposed a framework which can integrate Hidden Markow Models with ontology based Information Retrieval Systems. Using this approach, to satisfy the user needs of search criterion, we have made an attempt to optimize the performance and improve the efficiency of results in ontology based Information Retrieval Systems. Hidden Marow Models can improve the efficiency of the information search in the context of ontology preference. The comprehensibility of HMM can form the systematic and consistent logical connections between the terms of the ontology database which can further progress the user search with less fraction of irrelevant document retrieval.

References

[1] *I.Ruthven, M.Lalmas, C.J. van Rijsbergen, Incorporating user search behaviour into relevance feedback, in Journal of the American Society for Information Science and Technology, Volume 54, Number 6, pp. 528-548, 2003.*

[2] *Christophides, V., Karvounarakis, G., Plexousakis, D., Scholl, M. and Tourtounis, S.: Optimizing taxonomic semantic web queries using labeling schemes. Journal of Web Sematics 1, Issue 2, Elsevier (2003) 207-228.*

[3] *Hazman M., El-Beltagy S.R., Rafea A., A Survey of Ontology Learning Approaches, International Journal of Computer Applications, 2011, 22(8), 36–43*

[4] *He, Lina & Ming, Xinguo & Ni, Yanrong & Li, Miao & Zheng, Maokuan & xu, Zhitao. (2015). Ontology-based information integration and sharing for collaborative part and tooling development. Concurrent Engineering. 23. 10.1177/1063293X15580857.*

[5] *Dellschaft K., Staab S., Strategies for the Evaluation of Ontology Learning, In Proceedings of the 2008 Conference on Ontology Learning and Population: Bridging the Gap Between Text and Knowledge, IOS Press, Amsterdam, The Netherlands, The Netherlands, 2008, 253–272.*

[6] *Pietrzykowski, Marcin & Sałabun, Wojciech. (2014). Applications of Hidden Markov Model: state-of-the-art.*

[7] *K.P. Murphy, Machine Learning: A Probabilistic Perspective, Cambridge, MA: MIT Press, 2012.*

[8] *Kouemou G.L., History and Theoretical Basics of Hidden Markov Models, Hidden Markov Models, Theory and Applications, 2011, 10.5772/15205*

[9] *Azanzi Jiomekong et al, Extracting ontological knowledge from Java source code using Hidden Markov Models, Open Computer Science, Open Access 2019; 9:181–199*

Bidirectional Power Control Strategy for Super Capacitor Energy Storage System Based on MMC DC-DC Converter

SAJJANAPU RAJANI[1] | M.SHANKAR[2]

[1]PG SCHOLAR, Dept of EPS, AVANTHI INSTITUE OF ENGINEERING AND TECHNOLOGY, HYD, TS, INDIA.

[2] ASSISTANT PROFESSOR, Dept of EEE, AVANTHI INSTITUE OF ENGINEERING AND TECHNOLOGY, HYD, TS, INDIA.

ABSTRACT: The vessel integrated power system (IPS) displays a rising interest for high-voltage and huge limit energy capacity frameworks to prepare extra high-energy beat loads and upgrade power supply dependability. This examination centers around a super capacitor energy capacity framework in view of a flowed DC converter comprised of a secluded staggered converter (MMC) and double dynamic scaffolds considering the background (Spot). The truncation for the flowed converter is MMC-Spot. Top to bottom examinations of the framework's geography and tweak plot are given in this work. This exploration recommends a control technique that uses the Spot module of each branch to freely change the voltage of the sub-module capacitor while considering the downsides of the ordinary bidirectional power control methodology. The customary and recommended control systems' numerical models are laid out. Investigating and differentiating the two control strategies' security. The viability of the proposed control procedure was then affirmed by simulation on a MW-level of the MMC-Spot energy capacity framework that was built in MATLAB.

KEYWORDS: MMC, SUB MODULE, vessel integrated power system, DC CONVERTER.

I.INTRODUCTION: The vessel-facilitated electricity structure has a wide concept inside the fields of boating using pressure, delivery information, and DC energy dispersal. Later on, IPS will be one of the inescapable, unique courses for supportable electricity ships [1] and [3]. Lately, with the growing interest in higher boat strength, unflinching quality, and stuff like beat hundreds and new high-energy weapons, electricity restriction systems have become an important piece of the second-generation IPS [4], [5]. As wishes be, the strength-storing converter associated with the IPS medium voltage DC (MVDC) corporation needs to be portrayed by high voltage and large cutoff, voltage change, electric separation, and bidirectional change. To healthy the MVDC power machine, the converter can take on series-equal improvement, among which the information series yield equal (ISOP) structure is the maximum always used shape, which could chip away at the voltage and modern level of the converter [6]. In [7], a strength electronic transformer containing H-stages streamed by using Spots is proposed to additionally foster the electricity degree of

the train traction machine. Recorded as a tough replica [8], [9], one-of-a kind standardised DC converters are participated in in the collection and look like they cope with the identification and redecorate the voltage and cutting-edge stage of the converter. In any case, most of the above geologies take on midway series-associated capacitors and have an appalling weak spot and undeniable monotony potential, so they may now not be suitable for events with high requirements on power supply steadfastness and lucidity.

MMC is by and large used in excessive-voltage and big power programmes considering its planned improvement and version of non-fundamental unhappiness [10]. For excessive-voltage rail journey motors, the manipulation techniques of awesome capacitor energy restrict structure considering MMC are packed in [11], [12]. These papers understand the truthful decoupling management of the power of notable capaci-pinnacles and put forward the searching at exertion the board frameworks. In [13], the manage approach of the expected staggered power limit device under operating situations of move section voltage uniformity and unevenness is thought of, which deals with the issue of fee country concord of electricity accumulating elements. In [14], a weakness assurance system thinking about the combination of clear tools, recognisable proof circuits, and Field Programmable Doorway Display (FPGA) cease estimation for MMC amazing capacitor energy limit shape is proposed to cope with the prosperity and trustworthiness of the system. Yet the electricity is amassing shape, considering MMC can deal with the issues of MVDC pass segment access and transformation to non-basic unhappiness; it cannot realise the electrical separation between MVDC shipping and low-voltage DC (LVDC) transport; and it has excessive requirements for the association of energy management frameworks.

To comprehend the electrical segregation and voltage exchange, a limited bidirectional DC converter should be used between the MVDC enterprise and the LVDC lattice. Spot is a bidirectional DC converter with an electric separation restriction and a unique even plan. It has attracted expansive notions in the fields of electric motors, DC microgrids, and electricity limit systems [15] and [17]. In [18], [19], a solid kingdom transformer is proposed, which embraces the streamed plan of the half-range sub-module, Contact as the department topography, and ISOP as the general development. This geology is sensible for the MV scattering association in view of the fact that it is beneficial for the confirmation of the anticipated plan and the transformation to non-primary sadness. In [20], a 3-port DC converter made from MMC, spot, and copy chopper circuits for IPS is proposed, which comprehends the versatile strength required to manage the various MVDC shapes, LVDC enterprises, and conveyed power restriction units.

Nevertheless, the above abstract works consciousness on the application condition of interacting resistive weight at the LVDC transport of MMC-Spot. Their manipulation technique is that MMC controls the voltage of sub-module capacitors and Spot controls

the voltage of the LVDC transport. In the event that this system is contacted by a utility with an electricity restriction unit associated with the LVDC aspect, the Spot module generally controls the port current of the strength amassing unit. To all of the more likely control the port present day of the strength amassing unit, the channel inductor has to be associated between the spot converter and the strength accumulating unit. Regardless, this may affect the extent and weight of the device, and the robustness of the Touch Control gadget is near nothing. Especially even as turning in the terrific capacitor, the channel inductor, and the channel capacitor on the later duration of Spot structure a LC channel with big outcome impedance, which is simple to purpose streamed security issues [21].

The schematic of the proposed bipolar bidirectional DC converter is displayed in Fig. 1.1. It consists of three modules, and each module incorporates switches, an inductor, and a capacitor as essential circuits. Helper switches and thunderous circuits accommodate inductors and capacitors. The first module comprises fundamental switches (S1, S2), inductor L1 and capacitor C1, and two helper switches (SA1, SA2), inductor LR1 and capacitor CR1, which go about as an L-C reverberation circuit. Comparably, the other two modules, too, have similar parts. The ongoing through the inductors L1, L2, and L3 are addressed by i1, i2, and i3 in my view. A high move-ahead benefit in help mode or a high step-down gain in dollar mode can be accomplished by thinking about both high-quality and terrible circuits as a unique bidirectional DC converter. The transmission of the force stream and inborn voltage stability occur by making use of the L-C reverberation circuit. In every module, the assistant cell uses the L-C reverberation circuit to perform sensitive replacements in the switches and diodes. Working in spasmodic conduction mode makes the switches activate typically beneath ZCS situations, and a helper mobile is embedded into the fundamental energy channel to bring down the modern to not anything, bringing approximately a zero cutting-edge progress transfer off circumstance. At the factor of the fine circuit competencies as the lift mode and the terrible circuit talents as the buck mode, the direction of pressure flow can be from the low voltage side to the excessive voltage aspect. At the point when the superb circuit talents as greenback mode and the poor circuit capabilities because the elevate mode, then, at that factor, the heading of pressure move is from high voltage facet to low voltage aspect. The itemised interest of a bipolar secluded bidirectional DC converter is talked about in the resulting phase.

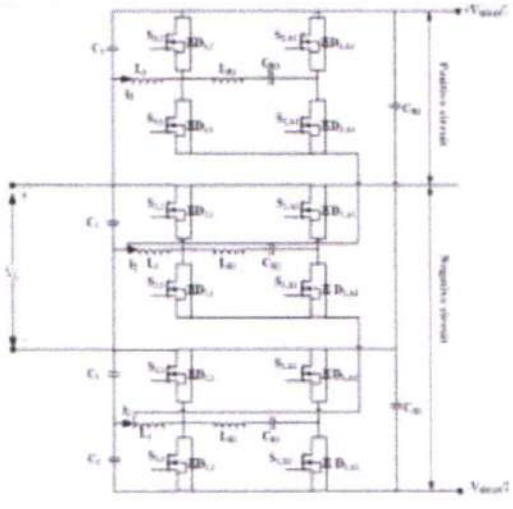


Fig. 1.1 Schematic of bipolar bidirectional DC-DC converter

The main innovations of this paper are as follows: (1) the bidirectional power conversion of a super capacitor energy storage system based on MMC-DAB is studied and a control strategy based on independent control of sub-module capacitor voltage is proposed. (2) A 1MW engineering prototype of MMC-DAB energy storage system is designed and manufactured to validate the proposed control strategy.

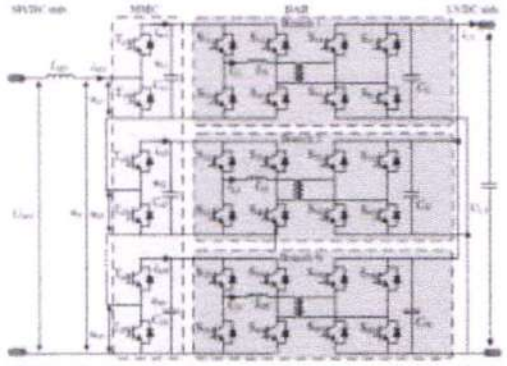


FIGURE 1. Topology of super capacitor energy storage system based on MMC-DAB.

II. PROPOSED SYSTEM: The topology of the super capacitor energy storage system based on the MMC-DAB, which is composed of N branches, is presented in Fig. 1. MMC structure with N half bridge sub- modules in series is adopted at the MVDC side to improve the power system capacity, voltage level and fault-tolerant operation ability.DAB is adopted at the LVDC side to provide electrical isolation. The super capacitor energy storage unit is connected to the LVDC bus to realize bidirectional power conversion with the MVDC bus. MMC-DAB is characterized by bidirectional power con- version, high degree of modularity and fault tolerance, which can meet the needs of integration of high-voltage large- capacity energy storage unit and improvement power supply reliability. In Fig. 1, UMV and iMV are the voltage and current of the MVDC bus, respectively. ULV and iLV are the voltage and current of the LVDC bus, respectively. Csi and usi are the capacitance and voltage of the i-th sub-module of MMC, respectively. LMV is the inductance on the MVDC side. Cfi is the lter capacitor of each branch on the LVDC side. Lsi and iLi are the leakage inductance and leakage inductance current of the transformer of each branch.

MMC is composed by series-connected half bridge sub- modules. When the branch fails, it can quickly cut off the whole branch through bypassing the sub module to sup- port the continuous operation of the energy storage system. To reduce the current ripple on the MVDC side, MMC adopts carrier phase-shift modulation. The driving pulse signals of the upper and lower switches of the same half bridge sub-modules are complementary. The phase-shift angle of the driving pulse signals of the corresponding switches of adjacent sub-modules is 2/N, and N is the number of sub- modules. Considering the relationship between the duty cycle of the upper switch and the carrier phase-shift angle, a switching cycle Tm is divided into N parts. Within each part, the total cascaded input voltage of the MMC uat has only two levels, and the difference between the two voltage levels is Usi. It is assumed that the capacitor voltage and the power of the sub-module of each branch of MMC is balanced, which means the duty cycle of each sub-module is consistent. According to KVL, the state equation of

inductance on the MVDC side is listed as (1).

As shown in Fig. 2, the topology of DAB is composed of two H-bridges and high-frequency transformers. In Fig. 2, us is the DAB high-voltage side port voltage. uLV is the DAB low-voltage side port voltage. nT is the transformation ratio of the high-frequency transformer. Cf is the low-voltage side lter capacitor. Csci and Resr are the capacitance and resistance of the equivalent supercapacitor of each branch. When operating within the rated voltage range of the energy storage unit, through the implementation of voltage matching control, the DAB can match the sub-module voltage on the high-voltage side with the voltage of the energy storage unit on the LVDC side, which is conducive to optimizing the high-frequency circulation characteristics and current stress of the DAB, which improves the efficiency of the system. Therefore, the single-phase shift (SPS) modulation is used in this paper.

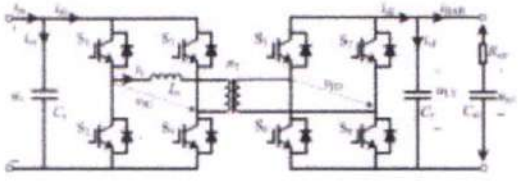


FIGURE 2. Topology structure of DAB module.

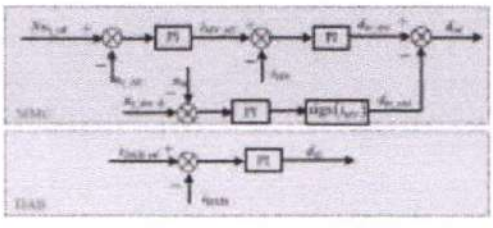


FIGURE 3. Block diagram of traditional control strategy of MMC-DAB.

As shown in Fig. 3, under the traditional control strategy, the control strategy of MMC is a dual closed-loop control with the sub-module capacitor voltage and the current of the MVDC bus as the control objectives, and the control strategy of DAB converters is a closed-loop control with the LVDC side current of each branch as the control objective. The reference value of the current of the MVDC bus is generated by the outer voltage loop of the controller of MMC, and the shared duty cycle dm_ave of sub-modules is generated through the PI regulator of the inner loop. Considering the difference of branches, the compensation duty cycle dm_exti is generated by the sub-module voltage balancing regulator to equalize the capacitance voltage of the sub-module. In Fig. 3, Nus_ref and us_All are respectively the sum of the reference value and the actual value of the capacitance voltage of all sub-modules. usi and us_ave are respectively the actual value and average value of the capacitance voltage of each sub-module. iMV_ref and iMV are the reference value and actual value of the current of the MVDC bus respectively. When the DAB converter is connected with energy storage units such as super capacitor, the charging or discharging cur- rent is difcult to control. Therefore, a filter inductor needs to be set between the DAB and the super capacitor. At this time, the DAB adopts single-loop current control. Since the voltage at the high voltage side of DAB is controlled by MMC under the traditional control strategy, the capacitance voltage of sub-module can be equivalent to voltage source when analyzing the mathematical model of DAB.

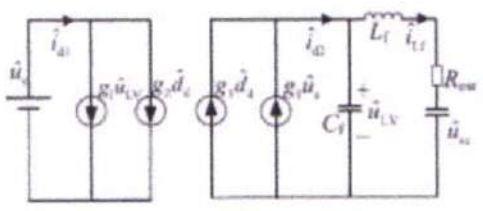


FIGURE 4. Small signal model of DAB module under traditional control strategy.

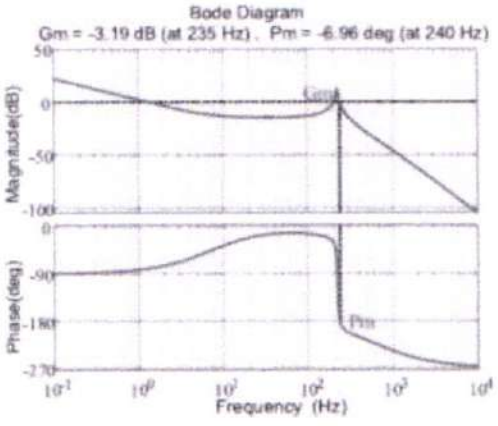


FIGURE 5. Open-loop frequency characteristic curve of DAB converter under traditional control strategy.

In Fig. 5, the frequency characteristic curve of open-loop transfer function under traditional control strategy is drawn by MATLAB. Among them, Gm is the amplitude margin of the open-loop transfer function of the closed-loop system, and Pm is the phase margin of the open-loop transfer function of the closed-loop system, which are used to measure the relative stability of the closed-loop system. According to the control theory, the stability of the closed-loop control system can be rejected by judging whether the amplitude margin Gm>0dB and the phase margin Pm>0 are satisfied. As shown in Fig. 5, the amplitude margin Gm is □3.19 dB, and the phase margin Pm is □6.96, which indicates that the DAB control system is unstable under the traditional control strategy.

The frequency of 240Hz in Fig. 5 is actually the cutoff frequency of the open-loop transfer function. In the above traditional control strategy, there are multiple PI regulators including the current control of MVDC bus, sub-module capacitor voltage balancing control of MMC and current control of DAB. There are many control variables, different regulators affect each other, and PI parameters are difficult to adjust. At the same time, when the DAB converter controls the current of the energy storage port, the system damping is small, which is difficult to realize the rapid charging and discharging of the super capacitor, and it may be also a problem of system instability.

When DAB is connected with energy storage units such as super capacitor, the charging or discharging current is dif- cult to control, so it is necessary to set lter inductance or interface converter at the input port of super capacitor, but this will increase the structural complexity and volume weight of the system. In order to control the charging and discharging current of super capacitor more conveniently, the DAB converter in each branch independently controls each sub-module capacitor voltage without controlling the charging or discharging current, which can simplify the converter structure and reduce the volume and weight of the system. The control strategy proposed in this paper will be further described in detail below. As shown in Fig. 6, under the control strategy proposed in this paper, MMC adopts double closed-loop control. The inner loop takes the inductance current on the MVDC side as the

control objective, and the control objective of the outer loop is decided according to the operating mode. In different modes, the control objective of DAB converter of each branch is always the voltage of sub-module capacitor, which is controlled by N independent voltage regulators. The port on MVDC side has two operating modes: (1) Mode 1 is that a bidirectional power source is connected to the MVDC bus to realize the bidirectional energy flow between the MVDC bus and super capacitor. In Mode 1, the control objective of the outer loop of MMC is the DAB output current, which indicates the total power of MMC-DAB. (2) Mode 2 is to connect the resistive load at the MVDC side, and the super capacitor supplies power to the resistive load. In order to maintain the continuity of the ship's power supply, in Mode 2, the control objective of the MMC outer loop is MVDC bus voltage.

From Fig. 6, iDAB_ref and iDAB_mean are respectively the reference value and the average of actual value of charging or discharging current of super capacitor. iMV_ref and iMV are respectively the reference value and actual value of the current of the MVDC bus. us_ref and us1 usi are the reference value and actual value of the voltage of each sub-module capacitor respectively. dd1 ddN are the outer phase-shift ratio of the DAB converter of each branch generated by the voltage loop.

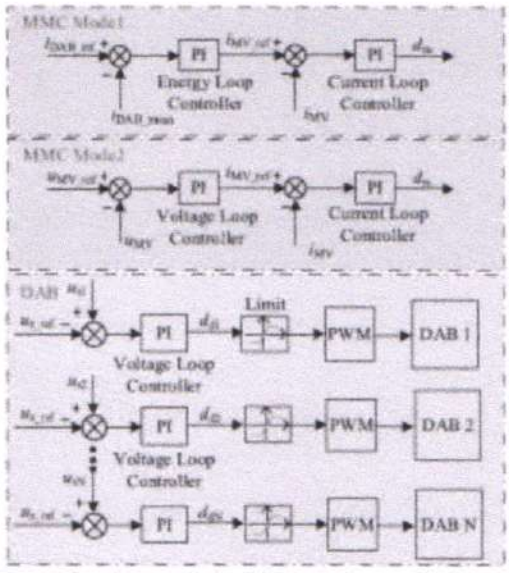
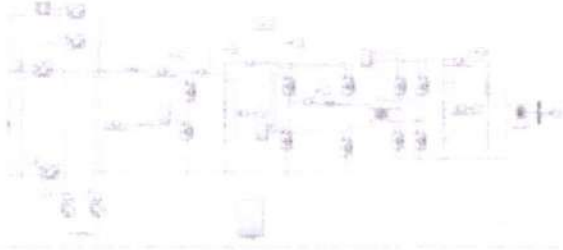


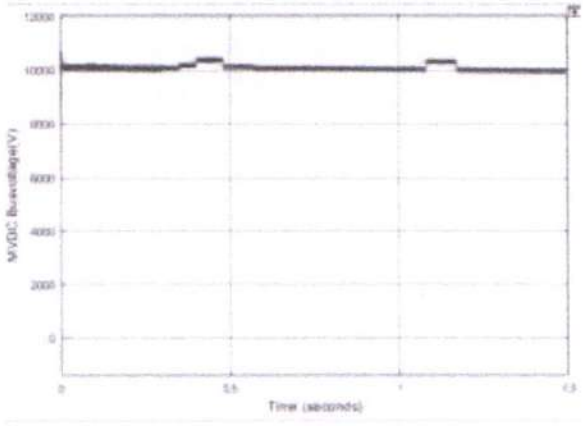
FIGURE 6. Block diagram of independent control strategy of sub-module capacitor voltage for MMC-DAB.

III.SIMULATION RESULTS

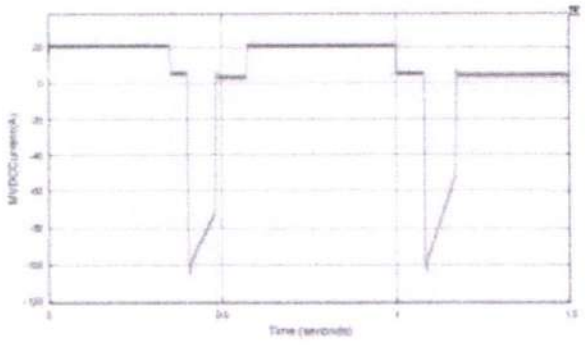
MODE_1



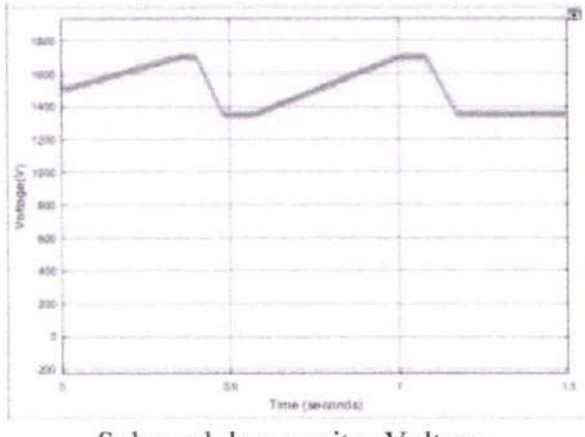
SIMULATION BLOCK DIAGRAM OF MODE_1



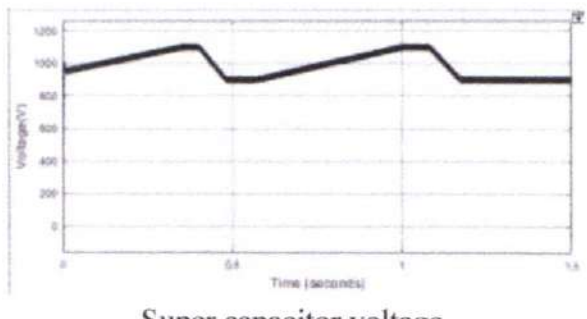
Voltage (V)



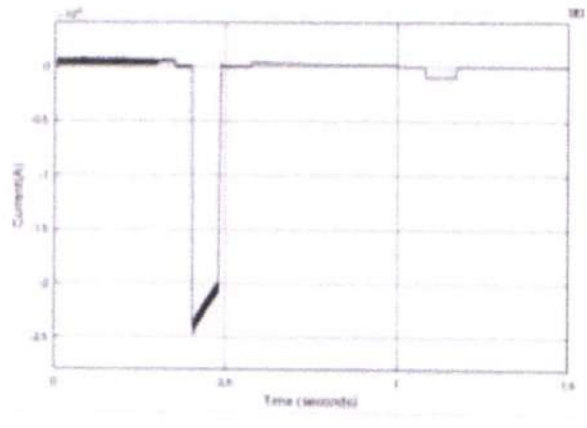
Bus current of MVDC



Sub module capacitor Voltage

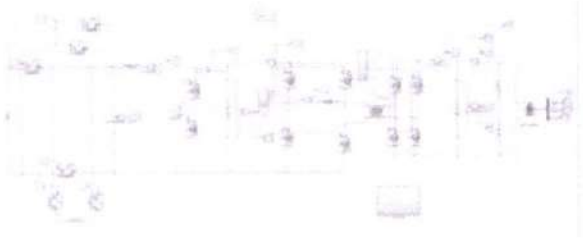


Super capacitor voltage

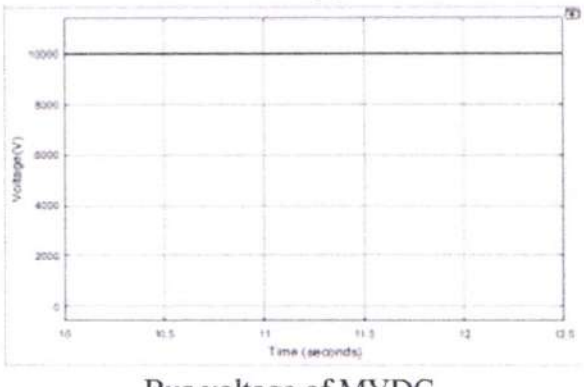


Bus current of LVDC

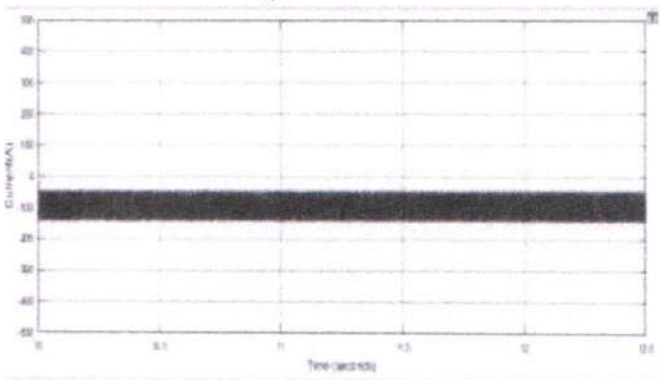
MODE_2



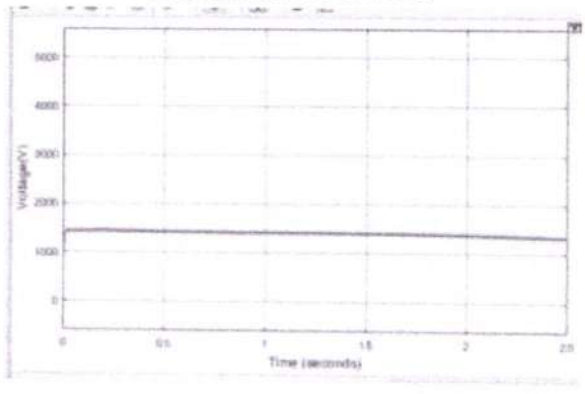
SIMULATION BLOCK DIAGRAM OF MODE_2



Bus voltage of MVDC

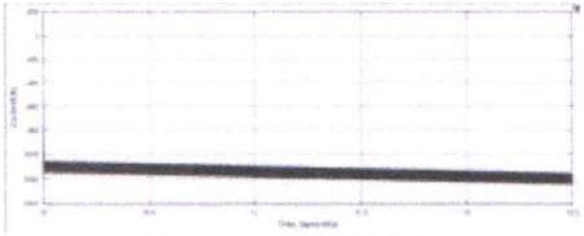


Bus current of MVDC

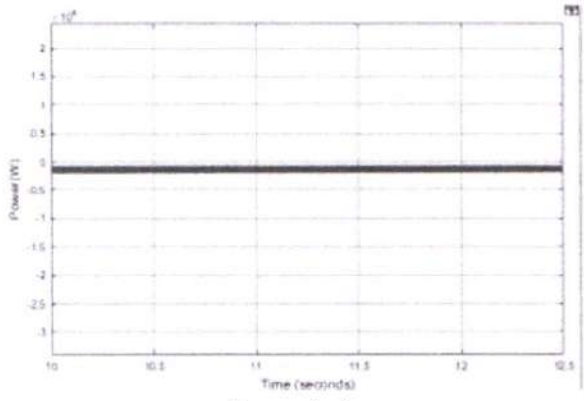


PRINCIPAL
Avanthi Institute of Engg. & Tech.
Guntihapally (V), Abdullapurmet (Mdl.), R.R. [illegible]

Sub module capacitor voltage



Bus current of LVDC



Power(w)

CONCLUSION

A cascaded super capacitor energy storage system based on MMC-DAB for vessel integrated power system is studied in this paper. The super capacitor energy storage unit is connected to LVDC bus, which is conducive to enhance the flexibility and reliability of the energy regulation of shipboard DC grid, and also provides power source for pulse loads on board. The traditional control strategy and the proposed independent control strategy of sub-module capacitor voltage are compared and analyzed. The mathematical models of DAB converters under the two control strategies are established, and the stability characteristics of them are compared. Under the proposed control strategy, the amplitude margin of DAB is infinite and the phase stability margin is 72.7, while under the traditional control strategy, the system presents an unstable state. Therefore, the system has better stability under the proposed control strategy. Finally, a modular and standardized engineering prototype of 1MW is designed and manufactured, and the experimental results are analyzed to verify the correctness of the theoretical analysis and control strategy design. This paper provides an effective solution for the development of MW-class modular energy storage converter.

REFERENCES

[1] W. Ma, ``On comprehensive development of electrization and information- ization in naval ships," J. Nav. Univ. Eng., vol. 22, no. 5, pp. 14, Oct. 2010.

[2] M. Weiming, ``Development of vessel integrated power system," in Proc. Int. Conf. Electr. Mach. Syst., Beijing, China, Aug. 2011, pp. 112.

[3] W. Ma, ``Development of vessel integrated power system," Ordnance Knowl., vol. 4, no. 3, pp. 3133, 2011.

[4] L. Fu, L. Liu, G. Wang, F. Ma, Z. Ye, F. Ji, and L. Liu, ``The research progress of the medium voltage DC integrated power system in China," Chin. J. Ship Res., vol. 11, no. 1, pp. 7299, Feb. 2016.

[5] S. Wan and Z. Meng, ``Current status and prospects of analysis technolo- gies of shipboard integrated power system," Chin. J. Ship Res., vol. 14, no. 2, pp. 107117, Apr. 2019.

[6] L. Qu, ``Study on key technique of input series combination converters control strategy," Ph.D. dissertation, Shenzhen Graduate School, Harbin Inst. Technol., Shenzhen, China, 2018.

[7] F. An, W. Song, and K. Yang, ``Model predictive control and power bal- ance scheme of dual-active-bridge DCDC converters in power electronic transformer," Proc. CSEE, vol. 38, no. 13, pp. 39213929, Jul. 2018.

[8] W. Chen, X. Ruan, and H. Yan, ``Control strategy for DC/DC multiple modules series-parallel combined systems," Trans. China Electrotech. Soc., vol. 24, no. 7, pp. 93102, Jul. 2009.

[9] L. Qu, D. Zhang, and Z. Bao, ``Output current-differential control scheme for input-seriesoutput-parallel-Connected modular DCDC converters," IEEE Trans. Power Electron., vol. 32, no. 7, pp. 56995711, Jul. 2017.

[10] H. Zhang, W. Shao, X. Wei, and N. Li, ``Study on fault tolerant con- trol strategy for sub-modules of modular multilevel converter," in Proc. Asia Energy Electr. Eng. Symp. (AEEES), Chengdu, China, May 2020, pp. 416420.

International Journal of Early Childhood Special Education (INT-JECSE)
DOI: 10.48047/INTJECSE/V14I6.374 ISSN: 1308-5581 Vol 14, Issue 06 2022

COMPENSATION MANAGEMENT

Author1: Dr. Y Jayaprada
Research Scholar, DR. A P J ABDUL KALAM UNIVERSITY, INDORE
Assoc. Prof. at Avanthi Institute of Engineering & Technology, Hyderabad

Author2: Dr. Sushil Beliya
Prof. DR. A P J ABDUL KALAM UNIVERSITY, INDORE

Abstract:
Compensation is a systematic approach to providing monetary value to employees in exchange for work performed. Compensation may achieve several purposes assisting in recruitment, job performance, and job satisfaction. An ideal compensation management system will help you significantly boost the performance of your employees and create a more engaged workforce that's willing to go the extra mile for your organization. Such a system should be well-defined and uniform and should apply to all levels of the organization as a general system. Plus you'll enjoy clearer visibility into individual employee performance when it comes time to make critical compensation planning decisions. With effective compensation management you'll also enjoy clearer visibility into individual employee performance when it comes time to make critical compensation planning decisions. These performance appraisals assist in determining compensation and benefits, but they are also instrumental in identifying ways to help individuals improve their current positions and prepare for future opportunities. Human Resource is the most vital resource for any organization. It is responsible for each and every decision taken, each and every work done and each and every result. Employees should be managed properly and motivated by providing best remuneration and compensation as per the industry standards. The lucrative compensation will also serve the need for attracting and retaining the best employees.

KEYWORDS: Human resource, Compensation, Organization, Management, Compensation Policies.

Components of Compensation

Basic wages /salaries. These describe the monetary portion of the pay system that serves as the foundation for other forms of remuneration. It is typically a set sum that may shift in light of yearly sums or likely to repeating compensation raises. It is coordinated in light of an individual's status inside the association and changes from grades to grades.

Dearness allowance. Workers and employees are able to deal with price inflation or increases in the cost of the goods and services they use when a dearness stipend is provided. The rapid rise in prices has a significant impact on how the labour force lives. The remuneration is reduced by rising costs to zero, and Inflation is causing a decline in the value of money.

The dearness stipend, which may be a fixed percentage of the base salary, helps employees deal with the rising costs.

Bonus. There are various methods to receive the incentive. It can be a set amount of the yearly minimum salary or a ratio based on profitability. Furthermore, the government requires all workers and employees to receive at least the minimum legal incentive.

Additionally, there is an incentive programme that pays managers and staff according to the amount of sales or profit margin they accomplish. Bonus programmes may also be founded on component rates, but they are subject to labour output.

Commissions. Depending on the company's sales or earnings, managers and staff members may receive commission payments. Every goal has a predetermined percentage that has been achieved. For tax purposes, commission is once more a taxable component of compensation.

The payment of commission is frequently utilized as a component of commission in target-based sales. Depending on the outcomes, businesses may pay commissions on a daily or recurring basis

INTRDUCTION: "Compensation Management is a process of determining cost-effective pay structures, designed to attract and retain talent, offer rewards for putting in extra effort, and structured to ensure that pay levels are perceived as fair." (David A. Deconzo, Eileen B. Stewart, Robin Stuart-Kotze, and Stephen P. Robinson). The money incentive mechanisms that organizations use to pay people for the job they do for them are known as compensation systems. (Margret AnnNeale, Gregory B. Northcraft, and Linda K. Stroh). "Compensation Management" relates to payment frameworks that establish employee pay, benefits, and direct and indirect compensation.

Objectives of Compensation Management

Compensation management seeks to attain the following objectives:

1. To entice highly qualified and effective workers, whose efforts will boost organizational success.
2. To keep bright workers on board so that the organization can continue to perform well and reach better skill levels.
3. To boost employee enthusiasm and happiness in order to improve employee dedication to the organizations aims and objectives.
4. To keep market viability in order to limit or regulate the hiring of new employees, which can have an impact on how well an organization runs.
5. To recognize staff members for their profitable efforts to the bottom line of the company.
6. To enhance efficacy by integrating staff efforts with organizational performance management tools.
7. To develop company identity, which is important for creating a group of prospective employees.
8. To assist the employee in achieving his or her material, social, psychological, and fiscal wants and goals.
9. To motivate staff members to advance their knowledge and abilities by giving higher pay for better work performance.
10. To instill in workers the necessary and favored behaviors.
11. To adhere to labor and societal laws such as the Equal Remuneration Act of 1976, the Minimum Wages Act of 1948, and Section 529-A of the Companies Act of 1956.

1.1 Principles of Compensation Management

1. Ability to pay:

Employers should compensate staff members in accordance with their ability and competence to pay. A company may go insolvent if it makes payments that are in excess of its financial capacity. On the other hand, if an organization spends significantly less than it can afford to pay, it will be difficult for it to hire and keep capable workers, which will eventually hurt the organization's effectiveness.

2. Internal and external equity:

Employers are required to pay their staff members in accordance with their education, background, work duties, abilities, and success. The term for this is domestic equity. Employees' happiness, dedication, and ability will suffer if their pay is not commensurate with their training, efficiency, skills, knowledge, and performance.

Such organizations are likely to witness low employee productivity, poor quality, high turnover, poor corporate image, etc . Therefore, maintaining a proper and fair difference in employee's compensation levels in terms of their position, competence, knowledge and performance is necessary fur effective business performance.

3. Performance orientation:

Compensation should be based on both organizational and individual success. Employees who perform better should receive greater pay in order to keep their improved production or performance and to motivate them to strive for greatness. Linking performance to work ethic is crucial for developing a performance-driven workplace. Where every employee willingly assumes responsibility and works with ownership. This also helps in maintaining a sense of justice and faith in the organization's leadership.

4. Non- discriminatory:

Employers must compensate their staff without discriminating on the basis of color, faith, gender, country, or heritage. For example, often female employees In India are paid far less than their male Counterparts. This is due to misplaced belief that women cannot perform as better as men do. Such biases and prejudices often rooted in our social norms and values, act as deterrent to employee performance and commitment.

5. Legal compliance:

According to the applicable rules of the country, organizations must contribute. For instance, the Minimum Wages Act of 1948 in India mandates that employees in minimum wage positions in the untrained, semi-skilled, and expert categories must be paid. This is essential character of any welfare state committed towards the goals of social justice and securing the rights of the employees to at least minimum standard of living. Therefore, an organization that does not have the ability to pay even minimum wages to it's employees has no right to exist.

6. Simplicity and flexibility:

Designing, comprehending, and implementing compensation systems should be easy. Compensation plans and policies must be adaptable in order to easily take into account the shifting requirements of the workforce, organizational goals and objectives, and employment market circumstances. To put it another way, pay administration needs to be tactically oriented.

7. Fosters employee development :

Employees should be compensated in a way that encourages them to develop their skills and abilities in line with shifting organizational requirements, technological advancements, and technological advancements. Increased differentiation on account of gaps in employee's skills and competencies acts as a motivator.

Types of compensation

The amount of pay that workers receive can influence In the form of direct financial benefits and/or secondary financial benefits in the form of perquisites, rewards at the time of, or acts. Compensation is the sum of all benefits and perks provided to workers in exchange for their services. This includes pay. When remuneration is given and handled well, it increases organizational output.

1.2 Direct compensation

The term "direct compensation" describes financial advantages offered and given to workers in exchange for the services they render to the company.

1 Basic Salary

Salary is the money that workers receive in exchange for the job they perform for a set quantity of time, such as a day, a week, a month, etc. Compensation is the payment an employee receives from their manager in return for their work.

2 House Rent Allowance

Associations either give lodging to their laborers who come from another state or country or they give them cash to cover their lease. This is accomplished in order to give them social protection and encourage them to labour.

3 Conveyance

Organizations offer their workers access to taxi services. A select few businesses also give their workers car and fuel payments to encourage them.

4 Leave Travel allowances

Organizations offer their workers access to taxi services. A select few businesses also give their workers car and fuel payments to encourage them.

5 Medical reimbursement

The wellbeing of workers is another concern for businesses. Medical claims are given to the workers for both themselves and their family members. These medical claims cover compensation for medical expenses and health insurance.

6 Bonus

Employees receive bonuses during the holiday season to encourage them and provide for their social protection. The incentive typically equals one month's worth of an employee's pay.

7 Special Allowances

Employees are given special benefits like extra pay, mobile reimbursements, food, rewards, transport costs, insurance, loans with lower interest rates, club memberships, etc. to keep them motivated and provide them with social security, which increases organizational output.

1.2.1 Indirect Compensation

The term "indirect compensation" refers to non-monetary advantages given and delivered to workers in exchange for the services they have rendered to the organization.

1. Leave Policy. Employees have the opportunity to take an appropriate amount of time off while employed by the company. The companies offer compensated breaks like maternity leaves, medical leaves (ill leaves), and informal leaves, as well as mandatory compensation, among other benefits.

2. Over time Policy. If an employee works extra, it is important to provide them with the necessary benefits and amenities, such as transportation services, overtime compensation, etc.

3. Hospitalization. To get their routine checkups, say every year, the workers should be given compensation. Even their children should be qualified for the medical claims because this would give them mental and social support.

4. Insurance. Organizations also offer health insurance and unexpected insurance to workers. This gives them mental stability and makes them feel appreciated by the company.

5. Leave Travel. As an the purpose of taking a family vacation, the workers are given time off and trip reimbursements. There are some businesses that plan a trip for their staff. Most of the time, this is done to reduce tension for the staff.

6. Retirement Benefits. Employers give benefits programs and different advantages for their staff individuals, which are beneficial to them once they reach the required retirement age.

7. Holiday Homes. Organizations offer their workers guest houses and vacation residences in various places. The majority of these vacation houses are found in hill towns and other popular vacation locations. The businesses ensure that the staff members have a trouble-free stay while they are staying at the hotel.

8. flexible Timings . Companies give workers variable scheduling options if they are unable to report to work during regular hours for legitimate personal or professional reasons.

CONCLUSION:

The motivation of the employee to improve organizational output depends on the quality of the pay plan. No one will come work for the company unless remuneration is offered. Therefore, remuneration aids in the efficient management of an organization and the achievement of its objectives. The pay system includes more than just salaries; workers also have other psychological and self-actualization requirements to meet. Therefore, payment accomplishes the goal. The finest talent will be attracted and retained by the organization with the aid of the most attractive pay. The salary should be in line with business norms.

References

1. Bob, N. (2011). Making employees suggestions Count, Journal of personnel management 17; 20 -41. 2. Bob, N. (2011). Making employees suggestions Count, Journal of personnel management 17; 20 -41. 3. Anyebe, A. (2003). The Nigerian Civil Service; Issues in structure and operation, journal of professional administration, 5; 11-17.

4. Armstrong, M (2005). A Handbook of Human Resources management practices. UK: Kogan page, 986

5. Ejiofor P. (2010). Management in Nigeria: Theories and issues. Onitsha: Africana- Feb publishers limited, 295.

6. Armstrong, M. and Brown, D. (2005). Relating Competences to pay: The UK Experience, Compensation and Benefit Review, 18(2); 2905-310.

7. Brown, A. (2003). Reward strategies, Journal of personnel management, 1; 17-29.

8. Dyer, and Schwab, P. (1991) Developing Job Evaluation, Journal of management, 5, 10- 14.

9. Fein, B. (2001). Compensation Management Strategies, Journal of personnel Administration, 18; 13-27.
10. Harrison, D.A and Liska, N. (2010). Promoting Regular Exercise in Occupational Fitness Programme, Journal of Personal Psychology, 5(5); 27-45.
11. Hewitt A.(2005). Managing performance with incentive pay, Journal of personnel Management, 7(1): 20-31
12. Nweke, A.(2009). Three years of Visionary leadership in Anambra State, Journal of Anambra State, Civil Service, 8(1), 7-12.
13. Pearce, L.(2010). Managerial compensation based on organization performance, Journal of industrial Relation, 52:3-28.
14. Redling, A. (2005). Effects of merit pay on performance, Journal of Management, 31:12- 19.
15. Luminita, B. (2001). The assessment center, a new "fashion" in personnel selection. Annals of the University of Oradea, Economic Science Series, 18 (4), 439-441.
16. Muchinsky, B. M. (2003). Psychology applied to work: Anintroduction to industrial and organizational psychology (7th ed.). Belmont, CA: Wadsworth/Thomson Learning.
17. Piotrowski, A. (2003). Current recruitment and selection practices: A national survey of Fortune 1000 firms. North American Journal of Psychology, 8 (3), 489-496.
18. Thornton L. (2008). Selection versus development assessment centers: An international survey of design, execution, and evaluation. International Journal of Human Resource Management, 20 (2), 478-498.
19. B. (2003). The use of person-organization fit in employment decision making: An assessment of its criterion-related validity. Journal of Applied Psychology, 91 (4), 786- 801.
20. Delmestri, G. & Walgenbach, P. (2009). Interference among conflicting institutions and technical-economic conditions: The adoption of the assessment center in French, German, Italian, UK, and U.S. multinational firms. International Journal of Human Resource Management, 20 (4), 885- 911.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Deign Of Multi Data Functional Based Fipflop For High-Speed Data Communication System

Vemuganti Laxmi Prasanna
MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: prasannavemuganti@gmail.com

Dr.S. Kishore Reddy
Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

D Suryaprakesh
Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

***Abstract*—To increase system composability and facilitate timing closure, fully synchronous clocking is replaced by more relaxed clocking schemes, such as mesochromous clocking. Under this regime, the modules at the two ends of a monochromous interface receive the same clock signal, thus operating under the same clock frequency, but the edges of the arriving clock signals may exhibit an unknown phase relationship. In such cases, clock synchronization is needed when sending data across modules. In this brief, we present a novel mesochromous dual-clock first-input– first-output (FIFO) buffer that can handle both clock synchronization and temporary data storage, by synchronizing data implicitly through the explicit synchronization of only the flow-control signals. The proposed design can operate correctly even when the transmitter and the receiver are separated by a long link whose delay cannot fit within the target operating frequency. In such scenarios, the proposed mesochromous FIFO can be extended to support multicycle link delays in a modular manner and with minimal modifications to the baseline architecture. When compared with the other state-of-the-art dual-clock mesochromous FIFO designs, the new architecture is demonstrated to yield a substantially lower cost implementation**

***Key Words*- synchronization, FIFO, clock signals, mesochromous**

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

I. INTRODUCTION

Ever shrinking transistor sizes have enabled the integration of a greater number of components onto a single chip—thus making systems-on-a-chip (SoCs) with many complex modules a common design solution. Unfortunately, global interconnect scaling has not been able to maintain the same performance increases [1], causing the timing of high-speed global clock signals to become a major concern in system design. This has resulted in clock distribution circuits requiring increasing circuit resources and design time. Nearly all existing digital systems utilize synchronous design techniques which normally require an accurate and highly synchronized global clock reference to be supplied to all areas of the circuit. One solution for coping with the clock distribution problem is to utilize self-timed or asynchronous circuits, which do not have a global timing reference signal. However, the lack of mature design tools and the reluctance of industry to incur the cost and risk of moving away from successful synchronous design flows have limited the acceptance of these design styles [2]. An alternative approach is to create systems that mix asynchronous and synchronous design techniques using a globally asynchronous locally synchronous (GALS) [3] design approach. In this paradigm, blocks are built using traditional synchronous design techniques, but these synchronous blocks do not share global timing

information and are asynchronous with respect to each other. While it is often convenient to divide a system into multiple subcomponents, it is unlikely that these components will operate autonomously. Accordingly, data transfer is required between local synchronous blocks. Accomplishing this task reliably and efficiently are key challenges in GALS designs

II. LITERATURE SURVEY

Dally and Poulton [4] and Balch [5] present high-level views of dual-clock FIFO structures, but details of dual-clock FIFO designs are lacking in the literature. Fully asynchronous FIFOs often appear in the literature [6], [7], but these designs do not utilize clocks, and therefore, are difficult to apply in cases of synchronizing da ta between clock domains. Table I lists several dual-clock FIFO designs. In the work presented by Greenstreet [8], the clocks are derived from the same base frequency, but may have an arbitrary phase difference—which is slightly more general than strict mesochronous The FIFO designed by Chakraborty et al. requires time to develop a frequency difference estimate before transferring data, as well as usage of different circuits depending on which clock domain has the higher rate [9]. Siezovic [10] presents a linear FIFO architecture for data synchronization, which has the limitations presented in Section II-A. An alternative FIFO architecture for use in some dual-clock applications is presented by Chelcea and Nowick [11]. The design uses independent registers as storage elements, and each register has its own and signals. This scheme reduces the latency when the FIFO size is small, but is less suitable when the FIFO size is large. This work uses a dual-port SRAM as the storage element which increases memory density and improves FIFO size scalability [13]. Compared with the most similar previous work [12], this design includes configurable logic to make it suitable for many environments, and also enables complete oscillator halting during idle times to achieve high energy efficiency. The proposed FIFO design has been fabricated in what we believe is the first VLSI implementation of a GALS array processor.

III.EXISTING SYSTEM

To best address dual-clock FIFO issues, we first consider the case of a single-clock synchronous FIFO. This section covers these fundamental FIFO principles.

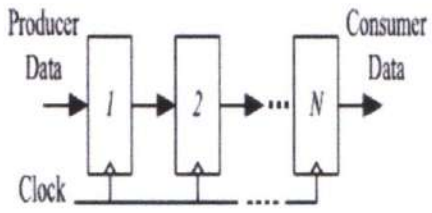


Figure 1. Linear shift-register FIFO block diagram.

A. *Linear FIFOs*

The simplest FIFO structure consists of a linear chain of latches or flip-flops connected serially as a shift register. Data is shifted into one end of the chain and propagates through every memory element until it reaches the end as shown in Fig. 1. This FIFO is synchronous since all movement of data requires a common clock. Alternatively, a linear elastic FIFO uses control signal handshakes to propagate data from location to location. Unlike the synchronous case, a datum can propagate through the FIFO without any new items entering. This results in the FIFO being at various degrees of fullness, hence, the name elastic. FIFOs of this nature work well with asynchronous designs and many examples of these can be found in the literature [15], [16]. A simple example of this type of FIFO is shown in Fig. 2.

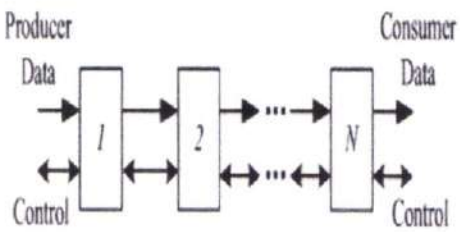


Figure 2. Linear elastic FIFO block diagram.

IV.PROPOSED SYSTEM

Modern systems-on-chip (SoC) implemented in deeply scaled technologies faces slow wires and process/voltage/temperature (PVT) variations. These challenges make the synchronous abstraction increasingly untenable over large chip areas, thereby requiring immense design effort to achieve timing closure [1], [2]. Partitioning the SoC into globally asynchronous, locally synchronous domains [3], [4] partially alleviate the problem, since synchronous operation and its associated timing constraints are confined inside each domain. However, in this case,

when crossing clock domains, the signals must be synchronized to the receiving clock domain, in order to avoid metastability [5], [6].

In addition to delivering synchronized signals across the clock domain interface, it is also important to ensure that any synchronized data that cannot be immediately consumed by the receiving domain are safely stored until it can be serviced. Since data must both be synchronized and (temporarily) stored, it is imperative that these two elemental and intertwined operations—synchronization and buffering—are combined in a cost-effective way that minimizes any latency and area overhead. In this brief, we focus on mesochromous clock domains, where clocks operate under the same frequency, but with a fixed, arbitrary phase difference. In such cases, using a generic asynchronous dual-clock first-input–first-output (FIFO) [7] for mesochromous clock domain, crossing is possible, but incurs unnecessary latency overhead [8]. Currently, there are two major approaches for efficient synchronization and buffering across mesochronic interfaces: 1) in a loosely coupled implementation [8], synchronization and buffering occur separately while 2) in a tightly coupled implementation [9]–[11], they are combined and fused into a single structure.

A. Proposed Mesochromous Fifo

The proposed mesochromous FIFO architecture combines the benefits of the loosely coupled [8] and tightly coupled approaches [9], [10], while avoiding their weaknesses. The new design couples synchronization and buffering in a cost-efficient implementation that fully supports multicycle link delays. A completely different operating approach is adopted, whereby the data are synchronized implicitly through the explicit synchronization of flow-control signals.

B. Architecture and Operation

Fig.1 shows the proposed mesochromous FIFO. Data that need to be synchronized are stored in a memory placed in the transmitter domain. Two monotonically increasing counters index the memory positions, where data are stored and accessed. The transmitter-synchronous tail pointer points to the write position in memory where a new data word is stored, while the receiver-synchronous head pointer points to the position from where a word will be read out. A pair of opposite-direction single-bit 4-flop synchronizers are used to sync enqueue (write) and dequeue (consume) events between the two sides. The 4-flop synchronizers are used to account for the worst case scenario that can occur with the asynchronous reset of the read and write pointers, as described in [8]. When the transmitter sends a data word that needs to be synchronized, it writes the data into the memory position pointed by the tail pointer. At the same time, the tail pointer is increased, and the push signal that is fed to the forward "tx2rx" mesochromous synchronizer [see Fig. 4(a)] is asserted. When the enqueue event is synchronized across the interface, the receiver can safely read out the data from the memory position pointed by the head pointer. This operation is shown in the short example of Fig. 4(b), which depicts the transfer of three data words ("A," "B," and "C") from TX to RX. Once the receiver actually consumes the data (e.g., reads it and sends it downstream), the pop signal is asserted, and the head pointer is incremented to point to the position where the next data word is found. Note that the receiver does not try to read data from the updated head pointer position, unless a new push event has been synchronized, indicating that new data exist and are safe to be read out.

In order to not lose track of multiple enqueue events, the receiver employs a "status" counter that counts the number of synchronized data items currently in the queue. Whenever a new data word is received, as indicated by an incoming enqueue signal from the "tx2rx" synchronizer in Fig. , the counter is increased; when a data word is consumed, the counter is decreased to reflect the change in the queue's state. In this way, two key objectives are achieved: 1) data are implicitly synchronized through the explicit synchronization of the enqueue events and 2) the FIFO order is preserved in the buffer. The next step is to synchronize the queue's state to the transmitter domain and guarantee that the queue does not overflow. To achieve this, the transmitter also uses a status counter, as shown in Fig. 4(a), to keep its own version of the number of items currently stored in the queue. The counter is incremented, or decremented, whenever an item is enqueued, or dequeued, from the queue, respectively. Since dequeue (pop) events are receiver-synchronous, they have to be synchronized to the transmitter domain through a separate backward synchronizer. On a dequeue, the receiver asserts the pop signal of the "rx2tx" synchronizer. Once the signal is synchronized, the transmitter decreases its status counter, effectively remaining in sync with the downstream buffer's state.

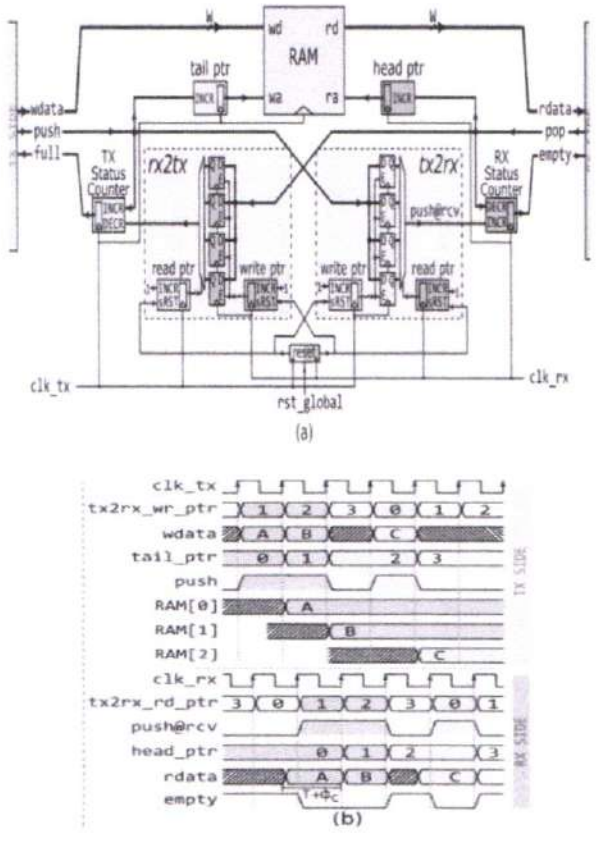


Figure 3. (a) Proposed mesochromous FIFO, which implicitly synchronizes data through the explicit synchronization of the flow-control push/pop signals. (b) Short cycle-by-cycle example of the operation of the proposed design.

Similar to [8], the forward latency of synchronizing and enqueuing a new data item is between one and three cycles, depending on he spread between the read and write pointers after reset. For safe operation under any phase difference, the initial spread between the read and write pointers at each synchronizer is two. When the reset of the read pointer of the push synchronizer is delayed (due to metastability), the forward latency is increased by one cycle. On the contrary, if the reset of the write pointer is delayed, the forward latency is decreased. In the case that the reset signal is not delayed, or delayed on both sides, the forward latency remains unchanged. The backward latency, i.e., the number of cycles needed to synchronize the pop events, is also between one and three cycles. However, worst case forward and backward latencies cannot occur simultaneously. The read pointer of the push synchronizer is driven by the same reset signal (the rx-side-synchronized version of the asynchronous reset) with the write pointer of the pop synchronizer. The same happens with the write and read pointers that are driven by the reset signal synchronized to the tx side. Therefore, once one side experiences a latency of three cycles (delayed reset of the read pointer), the other side will experience a latency of one cycle (delayed reset of the write pointer). Overall, the sum of the forward and backward latencies is constant at four cycles.

V.CONCLUSION

Irrespective of the physical proximity of the sender and the receiver in a mesochromous clock interface, the proposed low-cost dual-clock FIFO combines mesochromous clock synchronization and buffering in a scalable manner. Data are safely transferred on the receiver side of a mesochromous interface without being explicitly synchronized. Synchronization involves only the single-bit push/pop flow-control signals. This implicit synchronization of data saves considerable amount of area/power, especially in the case of multicycle links, without introducing additional latency, or reducing through.

References

[1]. Burchardt, A., Hekstra-Nowacka, E., and Chauhan, A.,"A Real-time Streaming Memory Controller", Design, Automation and Test in Europe 2005 Proceedings, 2005, vol.3, pp. 20-25.

[2]. Heithecker, S. and Ernst, R., "Traffic Shaping for An FPGA Based SDRAM Controller with Complex QoSRequirements", Design Automation Conference 2005, June 2005, pp. 575-578.

[3]. ANALOG DEVICES, AD9480 datasheet, Rev. A, 2004, 7.

[4]. ALTERA, DDR SDRAM Controller White Paper, Ver1.1, 2002, 8.

[5]. Guo Li, Zhang Ying, Li Ning, and Guo Yang, "The Feature of DDR SDRAM and the Implementation of DDR SDRAM Controllers via VHDL", The Journal of China Universities of Posts and Telecommunications, 2002, vol.9,no. 1, pp. 61-65.

[6]. Digital Systems Design Using VHDL by Charles H. Roth, Jr

[7]. CMOS Designing by Kanzg

[8]. Basic Digital Design by Morris Mano

[9].http://www.latticesemi.com/products/intellectualproperty/referencedesigns/ddrsdram controller.cfm

DESIGN AND SIMULATION OF MPC WITH FLC BASED HYBRID SYSTEM

T SAIKUMAR[1] | T.KRANTI KUMAR[2]

[1]PG SCHOLAR, Dept of EPS, AVANTHI INSTITUE OF ENGINEERING AND TECHNOLOGY, HYD, TS, INDIA.

[2] ASSISTANT PROFESSOR & HOD, Dept of EEE, AVANTHI INSTITUE OF ENGINEERING AND TECHNOLOGY, HYD, TS, INDIA.

ABSTRACT

In this task we propose fuzzy logic based hybrid energy framework took care of microgrid. By and large the vast majority of analysts are think about PI regulator for controlling the proposed framework however tuning the addition upsides of PI is troublesome due that getting more blunder and adding additional aloof components for remunerating recurrence variances. In this venture we propose FLC with a model prescient control (MPC) Controlling three-level bidirectional DC/DC converters for lattice associations with a HESS in a DC microgrid To start, a numerical model of a HESS with a battery and ultra capacitor (UC) is made, and the impartial point voltage irregularity of a three-level converter is tended to by looking at the converter's working modes. Second, a MPC approach for ascertaining consistent state reference values in the external layer and dynamic moving improvement in the inward layer is proposed for framework associated converter control. The external layer ensures voltage guideline and makes an ongoing prescient model, while the internal layer utilizes model prescient current control to cause the current to follow the anticipated worth, disposing of framework current wave. To understand the high-and low-recurrence power distribution for a HESS, this flowed design highlights two separate regulators and is without any trace of channels. Therefore, it empowers two sorts of energy stockpiling gadgets to independently manage voltage and acknowledges battery and UC power portion. At long last, reproduction results are planned in MATLAB/SIMULINK,ENVRIRORNMENTS. What's more, acquired results are demonstrated that proposed framework is superior to customary framework.

I.INTRODUCTION

Contrasted and the customary AC microgrid, the DC microgrid doesn't require complex AC/DC converters, and there is no adverse consequence brought about by responsive power. It diminishes power misfortunes and further develops matrix bandwidth and productivity [1], [2]. Thusly, research on the DC microgrid has gotten broad consideration. Sustainable power age is a significant piece of the DC microgrid framework. In any case, there are high-and low-recurrence power vacillations created by renewables [3]. The energy stockpiling framework (ESS) turns into a promising contender for tending to framework vulnerabilities and further developing framework functional efficiencies [4], [5]. The hybrid energy capacity framework (HESS) can make up for power vacillations in various recurrence groups by using remarkable attributes of different energy stockpiling gadgets, and in this way holds the qualities of each single energy stockpiling gadget. A commonplace illustration of a HESS is a blend of batteries with high energy thickness and ultra capacitors (UCs) with high power thickness. This blend can diminish battery charging/releasing cycles and draw out the help life, and has been broadly utilized in the

business. Be that as it may, the design and control issues related with the HESS should be broken. References [6], [7] show the resembled geography of battery and UC, which need low-pass channels to assign high- and low recurrence power changes and increment the control intricacy. By utilizing a flowing battery with UC through a power electronic gadget, for example, a bidirectional DC converter, the working methods of the battery can be improved [8], [9].

II.PROPOSED SYSTEM

In this paper, an MPC method is proposed for grid connected DC/DC converters of a HESS with a double layer control strategy to realize the voltage regulation and power allocation between battery and UC. Compared with the previous control methods, the main advantages of the MPC method proposed in this paper are as follows. 1) Compared with the previous work in [19], the proposed control method can achieve faster DC-link voltage restoration and desirable power allocation between the UC and the battery. 2) This control method of the HESS does not need filters to realize the high- and low-frequency power allocation. The proposed outer voltage control with a slope limiter can avoid a high charge/discharge rate of the battery. 3) Compared with the PI control method, the MPC method has a good dynamic response when the stable operating point of the system changes. Compared with other MPC methods with complex models, this method has lower computational complexity and running time.

A. Topology of the HESS

The topology of the hybrid storage grid-connected converter is shown in Fig. 1 [19]. The battery provides the UC with energy to regulate UC voltage and UC regulates the bus voltage by the three-level DC/DC converter. There are two types of input voltage values on the bus side, i.e., the full bus voltage Vdc or half of the bus voltage Vdc/2. The input voltage can be selected according to the actual situation. This topology can effectively reduce the inductor current ripples and the voltage stress of each switch, thereby suppressing the DC bus power fluctuations of the higher voltage levels.

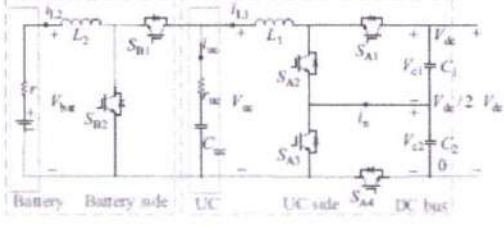


Fig. 1. The topology of a HESS.

In Fig. 1, Vbat and r are the battery terminal voltage and internal resistance, respectively; Vuc, ruc, and iuc are the UC voltage, resistance and current, respectively; Cuc is the UC capacitance; L1 and L2 are utilized for current regulation of the battery and UC; iL1 and iL2 are corresponding inductor currents; Vdc is the DC bus voltage; C1 and C2 are two identical capacitors; Vc1 and Vc2 are their voltages, respectively, and SAi (i is 1 to 4), SB1, SB2 are switches.

B. Mathematical Model of the Battery and UC

The battery model consists of a constant voltage source and a constant internal resistor in series. The output voltage is expressed as follows:

$$V_{\text{bat}} = E - i_{\text{bat}} r \qquad (1)$$

Where E is the constant voltage source potential and ibat is the battery current. UC has a large power density and can mitigate high frequency power fluctuations in the microgrid [20]. It can alleviate a high-power burden on the battery, and extend the lifetime of the battery [21], [22]. For DC microgrid systems, UC can be simply represented by an

ideal capacitor and equivalent series resistor r_{uc}. This simple model can accurately reflect the charging/discharging characteristics of UC [23]. The output voltage of UC can be depicted as follows:

$$V_{uc} = V_c + i_{uc} r_{uc} \quad (2)$$

C. Neutral Point Voltage Balance Method

Actually, the voltage values of the two capacitors on the DC bus side may vary and differ from each other significantly. It will result in the neutral point current in, known as the neutral point voltage (NPV) fluctuations, which will lead to an increase of the voltage stress of both the capacitor and switch. Therefore, switching on and off must be properly allocated to balance Vc1 and Vc2 [19]: When Vdc=2 < Vuc < Vdc, capacitors C1 and C2 are connected to the system, and the input voltage on the bus side is the full DC bus voltage Vdc, which will not produce a neutral point current in, when iL1 > 0, SA1 and SA4 operates in buck mode and when iL1 < 0, then SA2 and SA3 operate in boost mode. When Vuc < Vdc=2, only C1 or C2 is connected to the system, which will produce a neutral point current in. Thus, an NPV balancing scheme must be employed to effectively balance Vc1 and Vc2. At this time, the input voltage on the bus side is Vdc=2. The value of iL1 still determines whether the system operates in buck or boost mode and whether the capacitors are charged or discharged. The values of Vc1 and Vc2 determine whether C1 is connected to the system via SA1 and SA3 or C2 is connected to the system via SA2 and SA4.

III.MODEL PREDICTIVE CONTROL STRATEGY

In order to control the bus voltage of the DC microgrid and the voltage of UC, the control structure includes two parts: the battery provides the UC with energy and the UC provides the DC bus with energy. Each part includes two layers of control: outer voltage control and inner current control. The purpose of outer voltage control is to calculate the predictive value of the inductor current needed to stabilize the voltage. The function of the inner current control is to make the actual current follow the predictive value calculated from the outer control, so as to realize the function of the outer layer steady-state predictive value calculation and inner layer dynamic rolling optimization.

A. Outer Voltage Control Strategy

1) For Voltage Control on the Battery Side

When there is a deviation between the UC actual voltage Vuc and the rated reference voltage Vucref, the change of the UC voltage Vuc can directly result in the change of the current iuc. When the battery is discharged and the UC is charged, the converter on the battery side operates in boost mode and when the battery is charged and the UC is discharged, it operates in buck mode. In Fig. 2, according to Kirchhoff's current law (KCL), the input current of the converter is $i_{in} = i_{L1} - i_{uc}$. The reference current iL2ref can be obtained as follows:

$$i_{L2ref} = i_{in} \times \frac{V_{uc}}{V_{bat}} \quad (3)$$

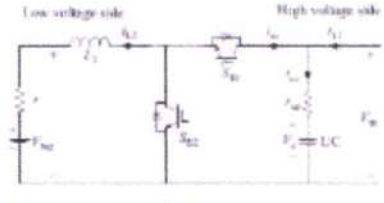


Fig. 2. The topology of the battery

The predictive current iL2(k +1) is calculated according to the sampling voltage and current. This current is the reference current iL2ref in the inner current control.

PRINCIPAL
Avanthi Institute of Engg. & Tech.
Guntlhapally (V), Abdullapurmet (Mdl.), R.R. Dist.

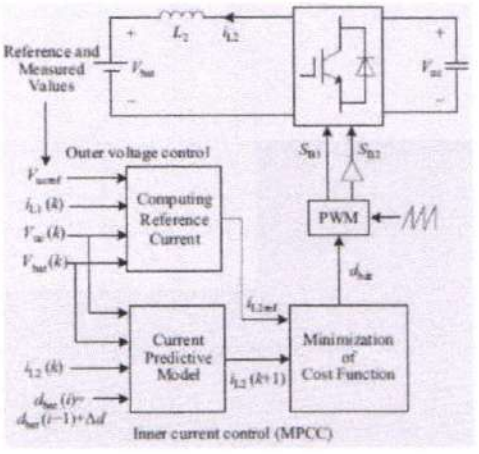


Fig. 4. The control block diagram for the battery

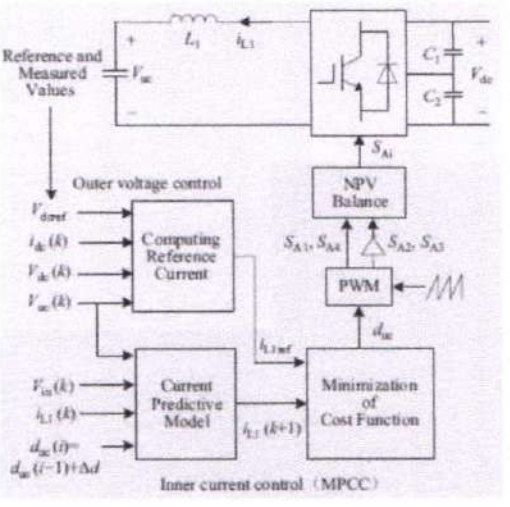


Fig. 5. The control block diagram for the UC.

2) Design a Slope Limiter for the Battery

Since the battery is not suitable for frequent charging/ discharging, the response of the battery current iL2 should be as slow as possible. In the outer voltage control, a battery current slope limiter is designed, that is, the change rate of the calculated reference current iL2ref can be made slower as follows. Within each sampling time Ts, the current reference value of the inductor L2 calculated at the kth instant is iL2ref(k), and the reference value calculated at the next instant is iL2ref(k+1).

3) For Voltage Control on the UC Side

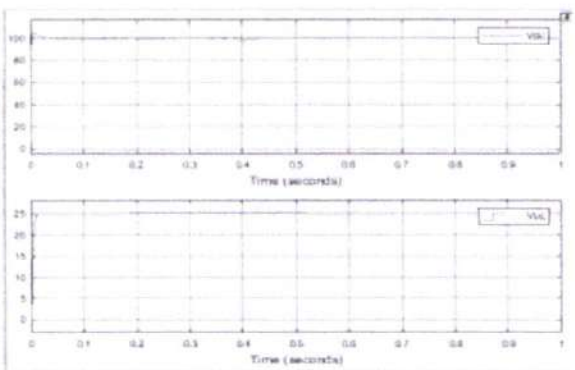
The rated reference bus voltage is Vdcref, and the actual voltage Vdc is regulated by the UC charging/discharging through the three-level DC/DC converter. duc is the duty cycle of the switches on the UC side, as shown in Fig. 5. The UC terminal voltage Vuc may be larger or smaller than Vdc=2 in the dynamic process of the system, which is according to the principle of NPV balance. The input voltage on the bus side may be Vdc or Vdc=2, which will be discussed in the following two cases.

The conventional controller approach may not be proficient to control the nonlinear systems. Over the years the concept of fuzzy logic regulator has been emerged and made itself one of the most dynamic regions of study. Because of its straightforwardness, fuzzy rationale control system ended up being commonly famous in this software. Fuzzy rationale is a sort of anticipation rationale or several-esteemed rationale; it accomplishes surmised thoughtful instead of fixed and careful. In contrast to conservative parallel groups, where factors take either obvious or bogus qualities, fuzzy rationale factors have a reality regard that ranges in degree some place in the scope of 1 and 0. Genuineness worth may range amongst totally obvious or completely bogus. Subsequently, Fuzzy rationale has been reached out to deal with the idea of fractional truth. Fuzzy rationale is a piece of computerized reasoning or AI is a piece of computerized reasoning or AI which deciphers a human's activities. PCs can decipher just evident or bogus qualities however a person can reason the level of truth or level of erroneousness. Fuzzy models decipher the human activities and are

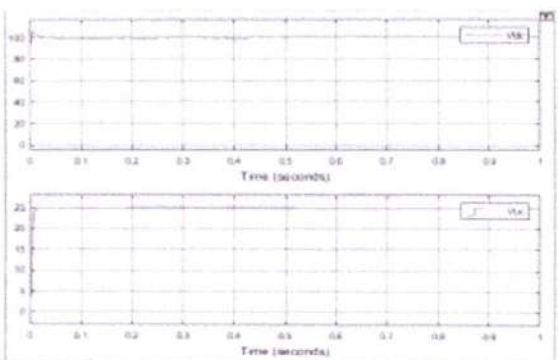
additionally called insightful framework. The crisp set is an advancement of a fuzzy set. fresh sets grant simply full enrolment or no participation in any way shape or form, while fuzzy sets fractional enrolment. In a fresh set, enrolment or no enrolment in segment x of group and is depicted by an incomplete participation, where and. Fuzzy set speculation widens this thought by describing fragmented enrolment.

IV.SIMULATION RESULTS

a. Step load changes



Simulation results using MPC method

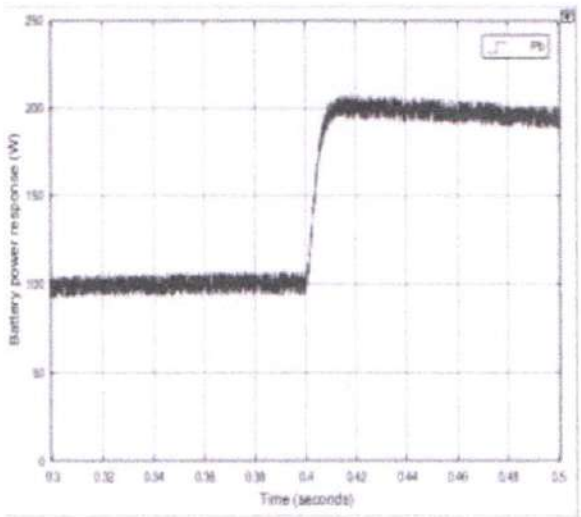


Simulation results using PI method

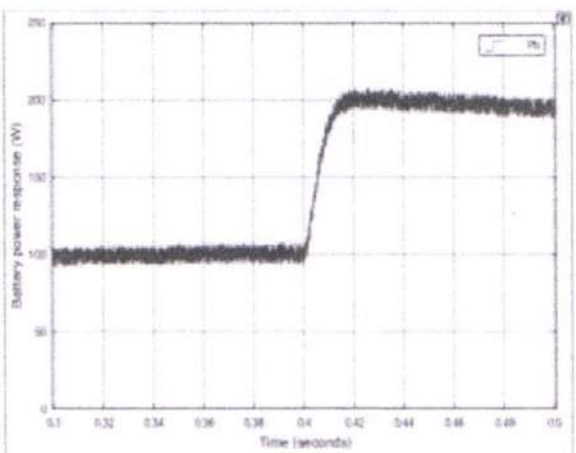
Comparison under the proposed MPC method with the PI control method.

b. Change controller parameters

At delta I = 0.05



At delta I =0.02



At delta I = 0.01

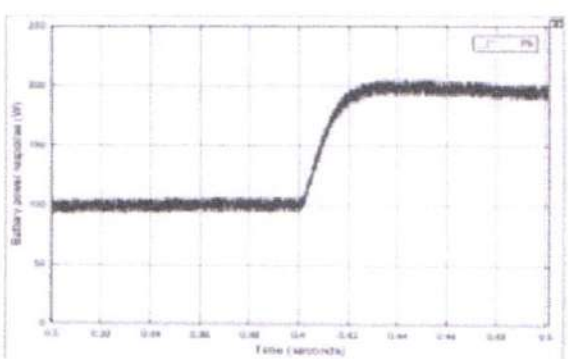
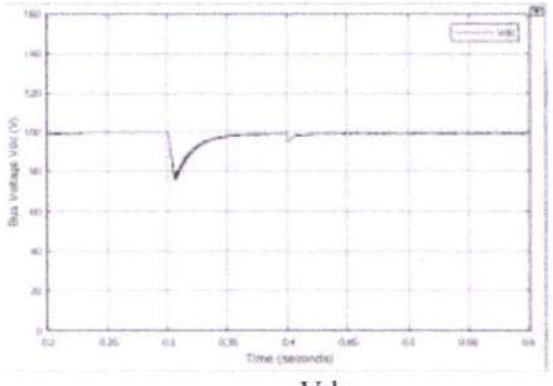
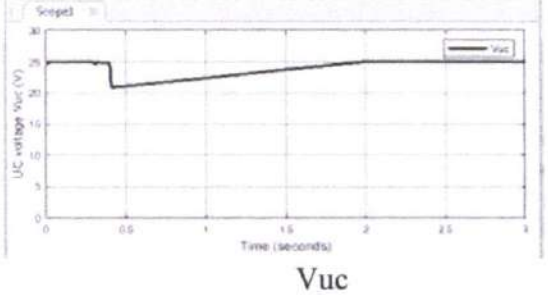


Fig. 2. The power response of the battery when the controller parameter δ_i is changed.

c. UC short circuit fault



Vdc



Vuc

Fig. 1. System voltage response in the case of short-circuiting of the UC

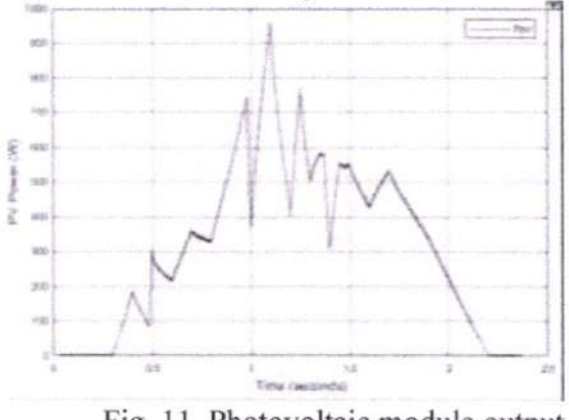
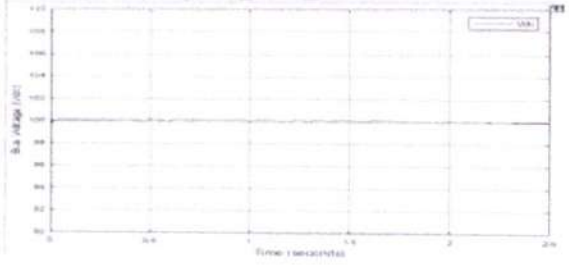
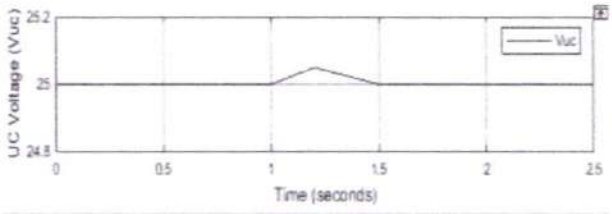
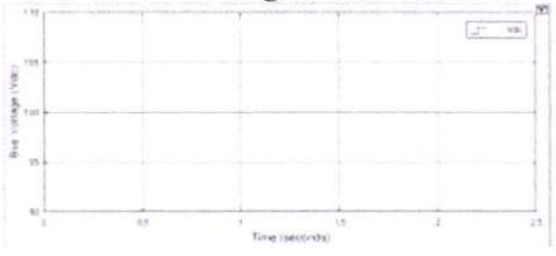


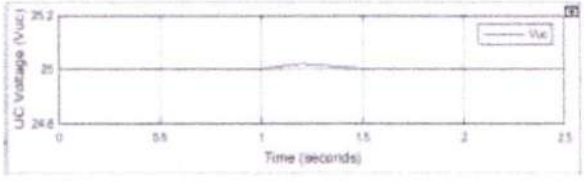
Fig. 11. Photovoltaic module output power.

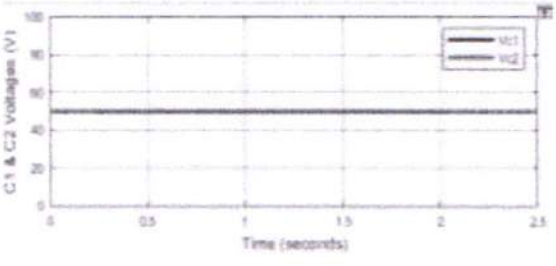




Using PI controller







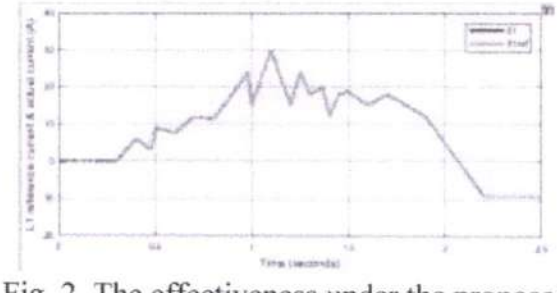
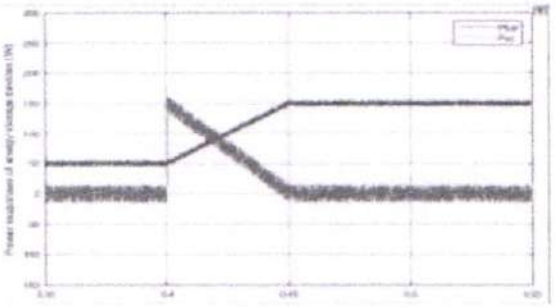
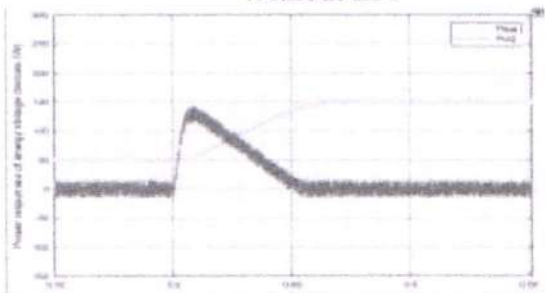


Fig. 2. The effectiveness under the proposed MPC method.

d. Comparison with LPF method
Step load change

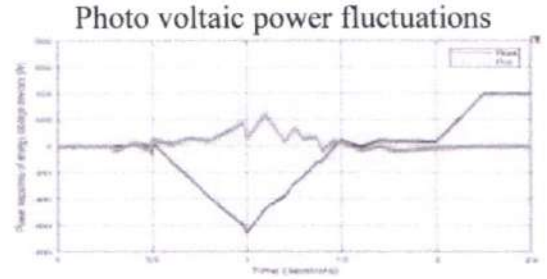


Without LPF

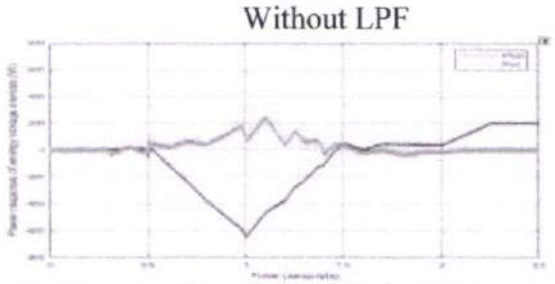


With LPF

Photo voltaic power fluctuations



Without LPF



With LPF

Fig. 3. Power allocation of the HESS.

A model Predictive controller with fuzzy

Fig 8a

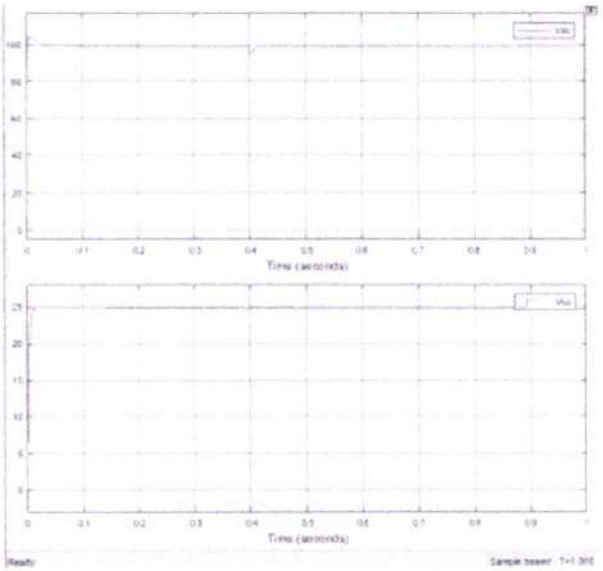


Fig 9a

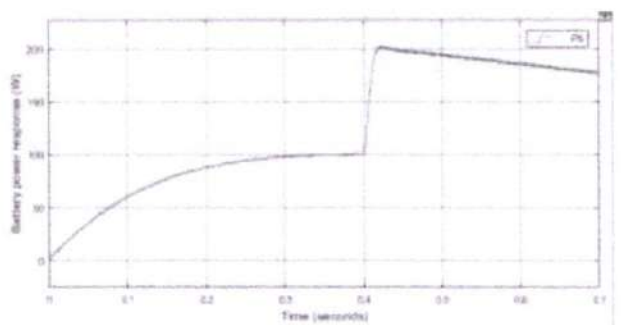
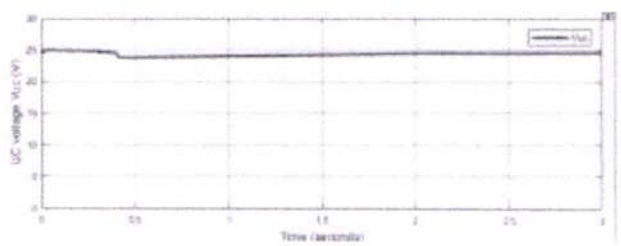
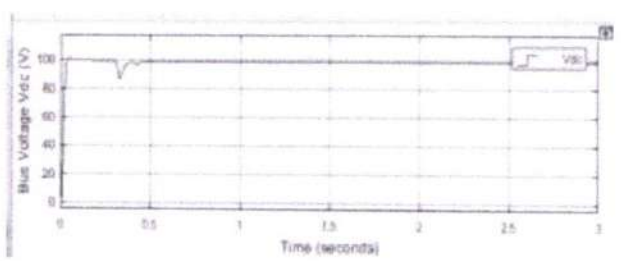


Fig 10





V.CONCLUSION

In this paper we propose FLC based hybrid energy framework took care of microgrid. By and large the vast majority of specialists are think about PI regulator for controlling the proposed framework however tuning the addition upsides of PI is troublesome due that getting more mistake and adding additional latent components for repaying recurrence vacillations. In this venture we propose FLC with a model prescient control (MPC) Controlling three-level bidirectional DC/DC converters in a DC microgrid for network associations with a HESS. After a two-stage helping development, the battery can smother higher voltage level changes at a similar framework voltage level. The MPC regulator, in contrast to the PI regulator, doesn't demand a tedious period of modifying boundaries, and many state factors are considered at each examining second. Moreover, the MPC calculation, which depends on a steady exchanging recurrence, accomplishes quick and exact voltage and current guideline with negligible waves. At long last, no filters are expected to disseminate power vacillations, and the control structure is enhanced while battery duration is broadened.

VI.REFERENCES

[1] D. Liang, C. Y. Qin, S. Y. Wang, and H. M. Guo, "Reliability evaluation of DC distribution power network," in Proceedings of 2018 China International Conference on Electricity Distribution, Tianjin, 2018, pp. 654–658.

[2] Z. Huang, J. Ma, J. Zeng et al., "Research status and prospect of control and protection technology for DC distribution network," in Proceedings of 2014 China International Conference on Electricity Distribution, Shenzhen, Sep. 2014, pp. 1488–1493.

[3] K. A. Joshi and N. M. Pindoriya, "Case-specificity and its implications in distribution network analysis with increasing penetration of photovoltaic generation," CSEE Journal of Power and Energy Systems, vol. 3, no. 1, pp. 101–113, Mar. 2017.

[4] Y. Xu, T. Y. Zhao, S. Q. Zhao, J. H. Zhang, and Y. Wang, "Multiobjective chance-constrained optimal day-ahead scheduling considering BESS degradation," CSEE Journal of Power and Energy Systems, vol. 4, no. 3, pp. 316–325, Sep. 2018.

[5] Y. Sun, Z. Zhao, M. Yang, D. Jia, W. Pei and B. Xu, "Overview of energy storage in renewable energy power fluctuation mitigation," CSEE Journal of Power and Energy Systems, vol. 6, no. 1, pp. 160–173, Mar. 2020.

[6] U. Manandhar, N. R. Tummuru, S. K. Kollimalla, A. Ukil, G. H. Beng, and K. Chaudhari, "Validation of faster joint control strategy for batteryand supercapacitor-based energy storage system," IEEE Transactions on Industrial Electronics, vol. 65, no. 4, pp. 3286–3295, Apr. 2018.

[7] H. J. Wang and J. C. Zhang, "Research on charging/discharging control strategy of battery-super capacitor hybrid energy storage system in photovoltaic system," in Proceedings of the 2016 IEEE 8th International Power Electronics and Motion

Control Conference, Hefei, 2016, pp. 2694–2698.
[8] U. Manandhar, B. F. Wang, X. N. Zhang, G. H. Beng, Y. T. Liu, and A. Ukil, "Joint control of three-level DC-DC converter interfaced hybrid energy storage system in DC microgrids," IEEE Transactions on Energy Conversion, vol. 34, no. 4, pp. 2248–2257, Dec. 2019.
[9] J. Cao and A. Emadi, "A new battery/ultracapacitor hybrid energy storage system for electric, hybrid, and plug-in hybrid electric vehicles," IEEE Transactions on Power Electronics, vol. 27, no. 1, pp. 122–132, Jan. 2012.
[10] Q. W. Xu, X. L. Hu, P. Wang, J. F. Xiao, P. F. Tu, C. Y. Wen, and M. Y. Lee, "A decentralized dynamic power-sharing strategy for hybrid energy storage system in autonomous DC microgrid," IEEE Transactions on Industrial Electronics, vol. 64, no. 7, pp. 5930–5941, Jul. 2017.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

Design Of Compression Tree Based Wallace Tree Multiplier For HighSpeed VLSI Application

GANGANAMONI ILAIAH
M.Tech student ECE, VLSI system design. Avanthi institute of Engg & Tech.
Dr.S. Kishore Reddy
Associate professor, HOD ECE, VLSI design Avanthi institute of Engg & Tech.
E mail : kishorereddy416@gmail.com
G.srinivas
Assistant professor, ECE Department, Avanthi institute of Engg & Tech.
E Mali: : sri414china@gmail.com

ABSTRACT

The concept of the estimated multiplier is a potential approach for many error-resilient systems to rising energy usage. We suggest an approximately 8 x 8 multiplier configuration with low power accuracy. in this phase. Two key aspects of the new architecture. The first is that various weights use various compressors to collect their component words depending on their value (in specific precision levels). It makes aminor mistake to reduce the power usage. Furthermore, we use rough-order (e.g. the 8:2 compressor) compressors to which the rationale of transport chains with small weights.To our knowledge, the proposed application is the first function in which approximate compressors in approximate multiplier architecture was effectively used. Experimental tests suggest that the estimated multiplier can achieve either low power and high precision relative to an actual multiplier (Dadda tree multiplier).

Key Words: ***multiplier, architecture, approximate compressors***

1. Introduction

One of the most important design requirements for any electronic device is the ability to save energy, and this is particularly true of mobile systems like smartphones, tablets, and other devices. Any such reduction at the cost of just a little time is highly sought

for. The most important parts of developing interactive software for such portable instruments are the DSP frames necessary for processing the signals. The functional core of these SPD structures is an arithmetic logic unit wherein multiplication plays a central role in all arithmetic operations. It is also important to improve multipliers' speed and power/energyconsumption qualities for greater CPU performance. Many of the DSP cores include built-in visual and video processing algorithms, with the resulting renderings suitable for either still images or moving ones.

Fast multipliers are crucial to optical signal systems. Since media processing has begun, the speed of multiply operations has been more important in both digital signal processing and general purpose processors. Historically, a series of addition, subtraction, and rearranging steps has been used. The term "multiplication" is often used to describe aseries of consecutive additions. To preserve information, the product is typically twice as lengthy as the operands if they are considered integrals. The numerical idea proposes a repeating kind of inclusion that is too slow to be nearly alwaysreplaced by a conditional layout method, and this is the case.

2. Literature Survey

In this section, we trace the lineage of our proposed approach in approximation computing back to some earlier work based on approximate multiplier architecture. Gupta et al. developed a proposal for an approximate adder that improves on the strength,range, and efficiency of a standard mirror adder by borrowing part of the rationale behindthe design. A bio-inspired approach proposed by Mahdiani et al. involves approximating the inputs' combined effects using OR windows. Estimated adders are presently the subject of new methods and indications for their modelling and estimation. Babic et al. proposed a piped log-based estimate to the form of a conventional Mitchell multiplier to achieve higher accuracy.

An error-tolerant multiplier is defined by dividing the multiplication into accurate (multiplication-based) and approximate (non-multiplication-based) halves. For partial component inclusion with tunable error recovery, Liu et al. proposed employing an estimated multiplier with a severely uncertain replacement. The method proposed by Kulkarny et al., in which an erroneous block is used to estimate a partial product, is

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

then applied to the final result. In this way, a faulty building block is used to produce widespread multipliers.

3. Existting Techniques

3.1 Basic Multiplication Schemes

In comparison to other arithmetic and logical, multiplication equipment also requires a lotof time and energy. A multiplier / MAC machine is used as a simple building block bythe digital signal processors, mostly with multi-intensive algorithms. Two steps may be preceded by a multiplication procedure:

1) Generate the partial products.

2) Accumulate (add) the partial products.

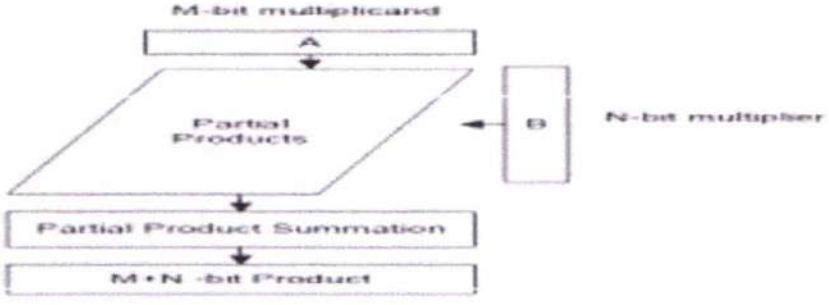


Fig. 3.1: Generic Multiplier Block Diagram

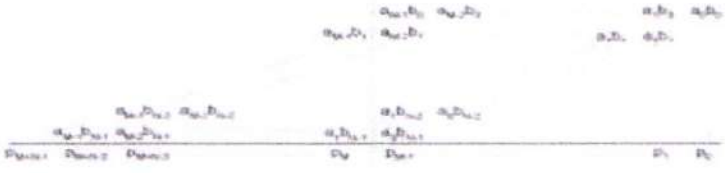


Fig. 3.2: Partial Product Array

3.2 Array Multiplier

The multiplier multiplies each and produces N partial products by something.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

That ofthese pieces is either moved by multiplicates or by 0. The partial output production consists of basic multiplier ANDing and multiplicanding.

3.3 Tree Multiplier

When introducing both of them concurrently, the tree multiplier decreases the period togenerate partial items. The multiplier sequence applies each partial platform in order.

CSAs are also used to collect partial goods in the tree multiplier.

3.4 Wallace Tree

Partial items were commonly identified as the Wallace Tree with complete adders as carrion-save adders, often called 3:2 counters. The definition of the 8 * 8-bit partial product trees reduction can be seen in Figure 3.3.

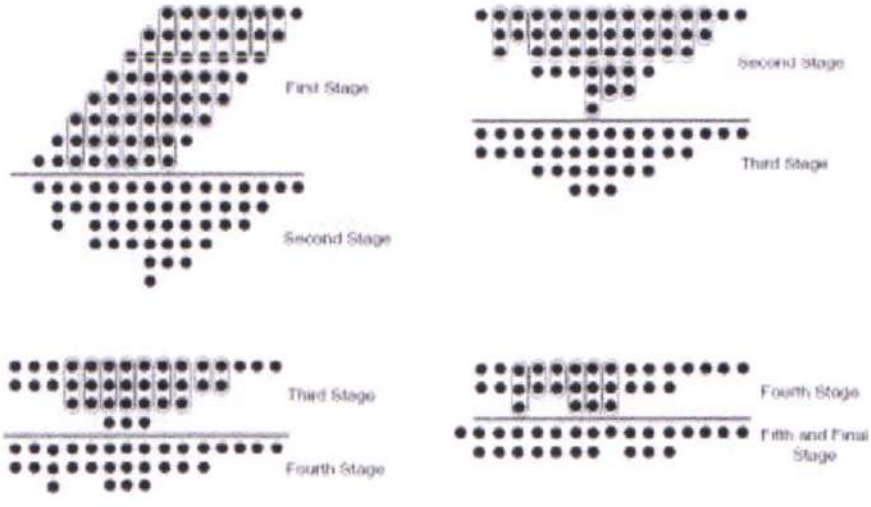


Fig. 3.3: Wallace Tree for an 8 * 8-bit partial product tree

4. Proposed Systems

4.1 Proposed Approximate Multiplier

The work plan of a multiplier is sometimes related to just the maximum height of PPM. So the PPM has to be compressed. A n:2 compressor is a multiplier slice that when

properly replicated reduces n (i.e. product terms) to two numbers. The n:2 compressor collects one or more bit of the bottom positions of n:2 in Slice I (e.g. i-1), generates two bits in the I and i+1 positions and one or more bits at the higher positions.

In the traditional design of the multiplier, 4:2 compressors are used[1,2]. The block diagram for an exact (i.e., exact) 4:2 compressor is shown in Figure 4.1(a). The input fourbits are X0, X1 , X2 and X3. The 2 output bits at positions I and i+1 are referred to respectively as Sum and Carry. The carrying bit is called Cin by the lower position, whilethe carrying bit is identified as Cout. The block diagram of an or thereabouts. 4:2 compressor is presented in Figure 4.1(b). The carrying pieces Cin and Cout are removed in order to save the sense of transporting strings. In addition, Sum and Carry logics (e.g., different of Sum and Carry logics in the accurate 4:2 compressor) is redesigned in [1,2] toreduce the error rate. Recent analysis [1,2] neglected to consider compression with high order (i.e., did not take n into account 5). High-order compression can reduce delay and power further. We present our high order design for compressors (that is to say n part 5) in this section.

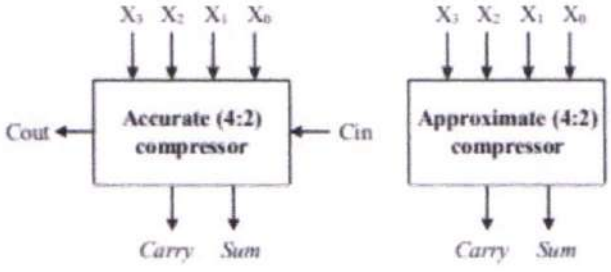


Fig. 4.1: (a) Accurate compressor (b) Approximate compressor

4.2 Proposed Approximate Multiplier Design

For addition, three pieces are a multiplier. For partial goods, AND gates are used in the first component. In the second section, a hold save adder tree lowers the max speed of PPM (partial component matrix). In the third component, the final product is a transportable propagation adder. The multiplier 's architecture sophistication is linked in particular to the PPM reduction circuitry (i.e. it needs to do with the PPM reduction circuitry in particular (i.e. second part). The Multiplier Technology Study[1-6] also concentrates on designing the circuitry for PPM elimination. We propose a configuration of approximately 8 x 8 multipliers in this segment. The configuration of

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

our PPMmitigation circuitry is shown in Figure 4.2.

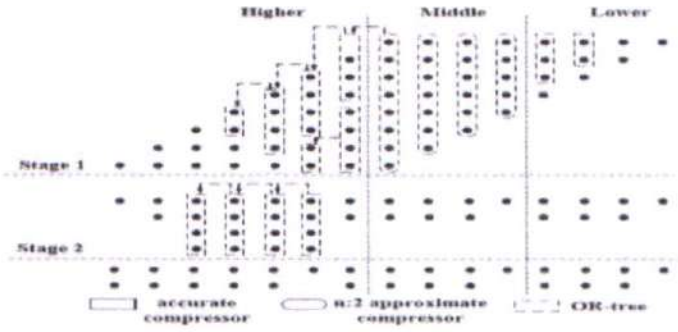


Fig.4.2:PPM Reduction In The Proposed Approximate Multiplier

The weights are categorized according to their definition under three categories: the higher weights, the medium weights and the lower weights. This is important to remember that the designers should specify the number of higher weights, the number of mean weights and the number of shorter intervals for the trade in power usage and numerical precision.

Our PPM reduction circuit utilizes the following sense guided logic compression technologies to minimize power usage with a minor factor: higher weights are using the actual (i.e., actual) of the 4:2 compressors, middle weights are using for our estimated high-order compressors (i.e. the estimated n:2 compressors) and unreliable compressors are using for the lower weights.

There are two phases to our PPM reduction chain. For both weights, the first stage is. Thesecond stage is for weights of greater value only. Increasing weight has a limit of two component terms until the second step is finished. The final result will then be achieved from a carry propagation adder. The specifics of the two phases are listed below.

4.3 Analysis Of Multiplier Using Approximate 4:2 Compressor

Approximate computing has drawn great attention as an attractive worldview for error tolerant applications that are able to accurately reduce energy consumption, delays and area. This article suggests the construction of a modern compressor of approximately 4–

2. A updated Dadda Multiplier design would be introduced to reduce the error on the performance for the effective usage of the proposed compressor.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

4.3.1 Exact And Approximate Compressor

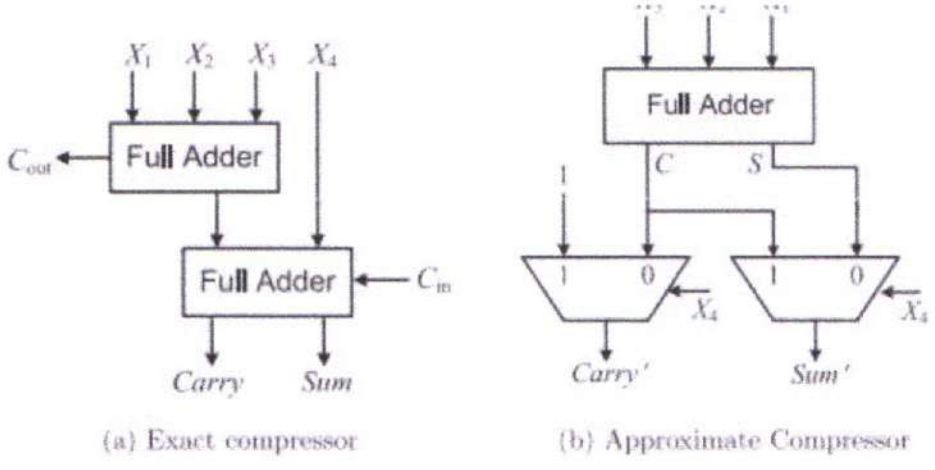
The function of the actual 4:2 compressor and the hypothetical compressor suggested is addressed in this section. Four compressors (X1; X2; X3; X4; Cin) and three (sum; carry;cout) are included in the 4:2 compressor. Both inputs are of the same binary weight and output value.

The compressor receives a binary bit less in value from the previous order block and generates Cut and Carry outputs one binary bit more in sense. The same 4:2 compressor circuit diagram is shown in the Fig. 4.6(a)(s). An integrated 4:2 compressor architecture proposed in [9] is used to evaluate estimated compressor output in this article.

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in} \tag{4.1}$$

$$C_{out} = (X_1 \oplus X_2)X_3 + \overline{(X_1 \oplus X_2)}X_1 \tag{4.2}$$

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4)C_{in} + \overline{(X_1 \oplus X_2 \oplus X_3 \oplus X_4)}X_4 \tag{4.3}$$



(a) Exact compressor (b) Approximate Compressor

Fig.4.3 :Sum Of 4:2 Compressor A)Exact B) Our Approximate

Around 4:2 is planned with the amount of output bits being decreased to two. Since this estimated compressor is used in the multiplier specification, the decrease of output bits

essentially decreases the amount of input bits in the multiplier layout for the succeeding compressors to four. The output bit Cut = 0 in the other 15 instances, with the exception of the input variation of "X4X3X2X1=1111'.' Cout is also not taken into consideration when constructing estimated compressors.

4.3.2Approximate Multiplier

In this section, design of an 8*8 approximate multiplier is presented. The multiplication operation can be divided into 3 steps as follows.

1. Generation of partial products by the multiplication of each bit of multiplicand with each bit of multiplier.
2. Accumulation of partial products into two rows.
3. The computation of final binary result generally using carry propagate adder.

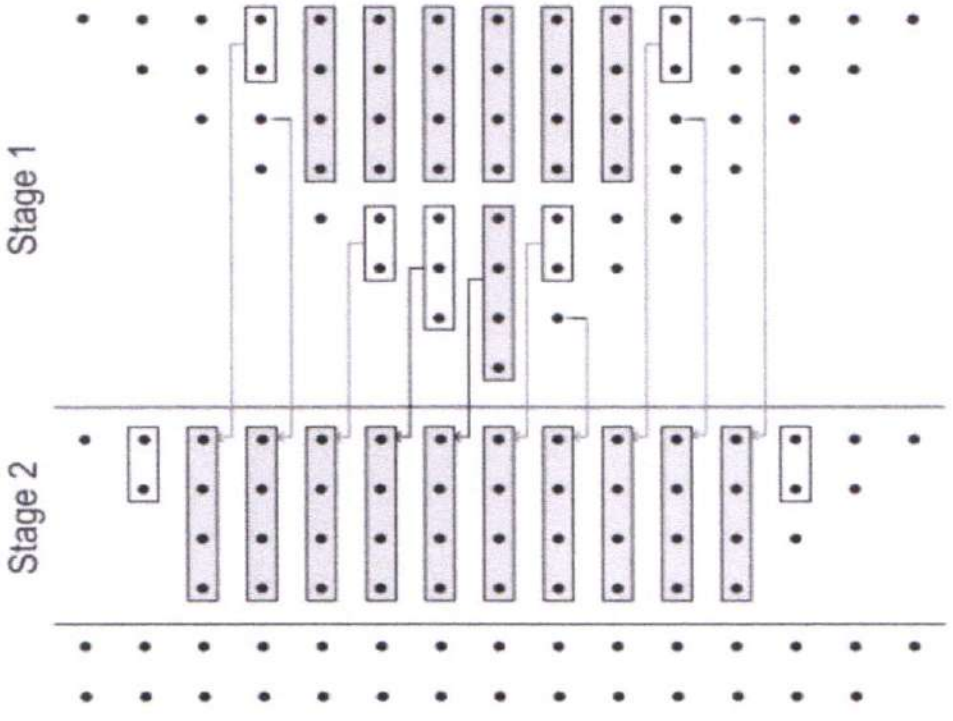


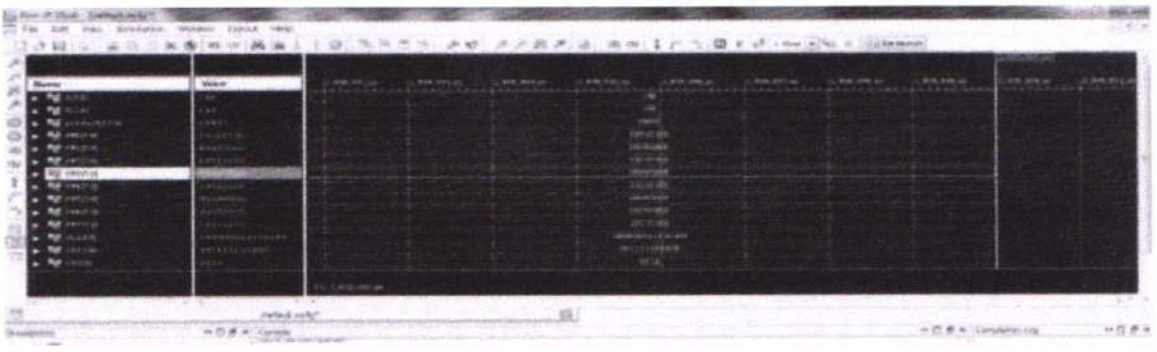
Fig.4.4 :8:8 Approximate Multiplier

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

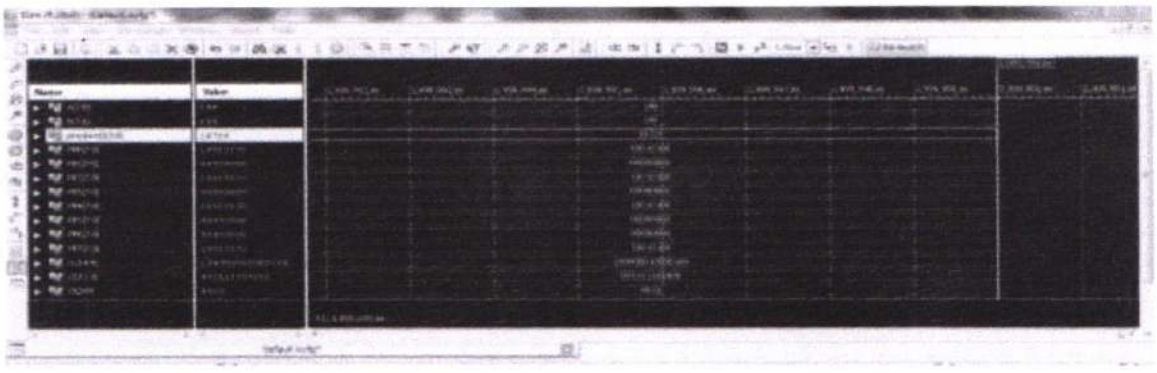
5. Result And Discussions

5.1 Simulation Result

Approximate Sum Approximate Carry



Exact_Sum_Approximate_Carry:



5.2 Synthesis Result

The programs that have been built are simulated and tested. The RTL analysis is carried out using the Xilinx ISE method after practical testing. The RTL pattern, which isassigned to a certain hardware repository, would be translated to the Gate level mesh set.

A number of different tools were included in the Xilinx ISE platform here in this Spartan 3E unit. For this synthesis, the computer called "XC3S500E" and the kit "FG320" have been selected with the pace of the system like "-5." This concept has

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

been synthesized and the effects analyzed:

5.3 Design Summary

Approximate Sum Approximate Carry

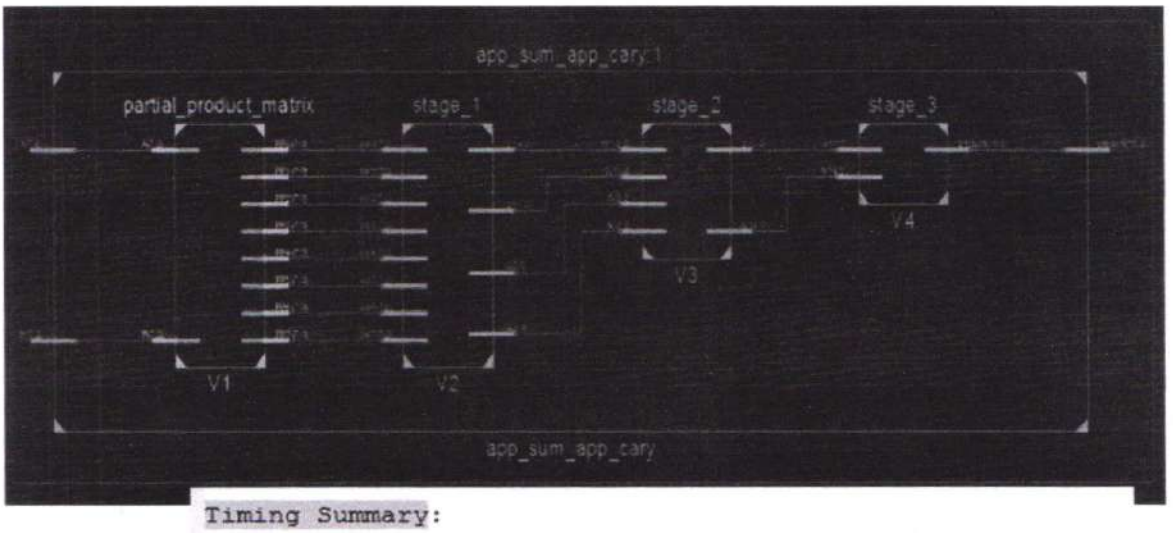
Device Utilization Summary (estimated values)				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	
Number of Slice LUTs	101	2400	4%	
Number of fully used LUT-FF pairs	0	101	0%	
Number of bonded IOBs	32	102	31%	

Approximate_Sum_Approximate_Carry:

Device Utilization Summary (estimated values)				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	
Number of Slice LUTs	101	2400	4%	
Number of fully used LUT-FF pairs	0	101	0%	
Number of bonded IOBs	32	102	31%	

5.4 RTL Schematic

Approximate Sum Approximate Carry



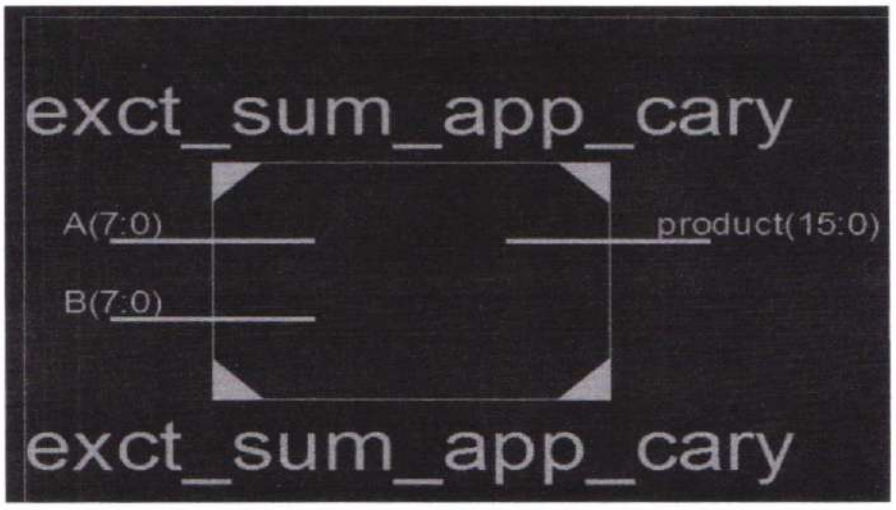

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 12.584ns
```

PRINCIPAL
Avanthi Institute of Engg. & Tech.
Guntihapally (V), Abdullapurmet (Mdl.), R.R. Dt.

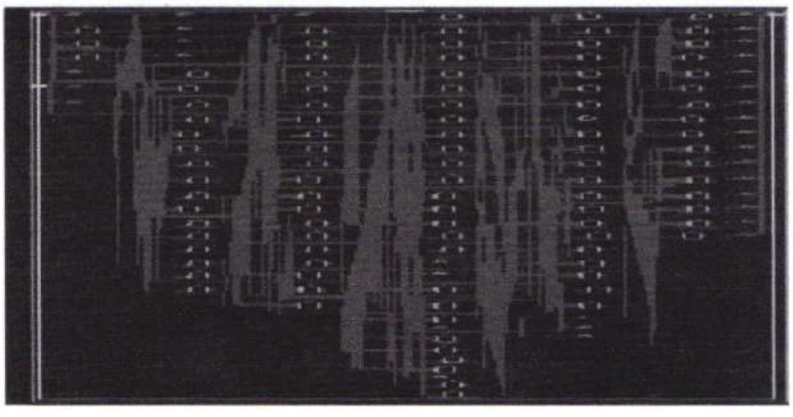
Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

Exact_Sum_Approximate_Carry:



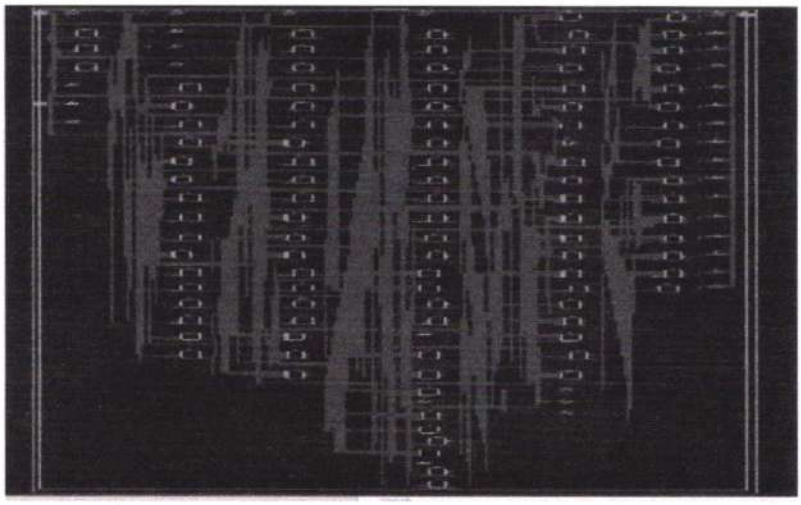
5.5 Technological Schematic

Approximate Sum Approximate Carry



Exact_Sum_Approximate_Carry:

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023



Conclusion

In this post, we have proposed a rough multiplier named RoBA multiplier, which is high-speed but energy efficient. The suggested multiplier was focused upon rounding the inputs in 2n format, which was highly effective. The calculally sensitive portion of the multiplication was therefore skipped for the sake of a small error to increase efficiency and energy usage. The solution suggested extended to both signed and unsigned addition and multiplication. Three device solutions were addressed, including one for the unsignedoperations and two for the subscribing operations. The efficiencies of the recommended multipliers were tested using various architecture criteria in contrast with those of other reliable and rough multipliers. In most (all) instances, the RoBA multiplier architectures surpassed the corresponding (exact) multipliers. In two image processing applications for sharpening and smoothing, the efficacy of the suggested approximate multiplicationmethod was tested. The picture output was similar to that of same algorithms in the contrast.

References:

[1] M. Alioto, –Ultra-low power VLSI circuit design demystified and explained: A tutorial,IIEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012.

[2] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, -Low-power digital signal processing using approximate adders,I IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.

[3] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, -Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications,IIEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 850–862, Apr. 2010.

[4] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, -MACACO: Modeling and analysis of circuits for approximate computing,I inProc. Int. Conf. Comput.-Aided Design, Nov. 2011, pp. 667–673.

[5] F. Farshchi, M. S. Abrishami, and S. M. Fakhraie, -New approximate multiplier for low power digital signal processing,I inProc. 17th Int. Symp. Comput. Archit. Digit.Syst. (CADS), Oct. 2013, pp. 25–30.

[6] P. Kulkarni, P. Gupta, and M. Ercegovac, -Trading accuracy for power with an underdesigned multiplier architecture,I inProc. 24th Int. Conf. VLSI Design, Jan. 2011, pp. 346–351.

[7] D. R. Kelly, B. J. Phillips, and S. Al-Sarawi, -Approximate signed binaryinteger multipliers for arithmetic data value speculation,I in Proc. Conf. Design Archit. Signal Image Process., 2009, pp. 97–104.

[8] K. Y. Kyaw, W. L. Goh, and K. S. Yeo, -Low-power high-speed multiplier for error- tolerant application,I in Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits(EDSSC), Dec. 2010, pp. 1–4.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Design Of High Order Compression Multiplier For High-Speed DSP Applications

B Bhavani
MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: Bhaskarabhavani20@gmail.com

Dr.S. Kishore Reddy
Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

Mr. E Nagesh
Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: nagesherugu@gmail.com

Abstract- **Redundant Binary Partial Product Generator technique are used to reduce by one row the maximum height of the partial product array generated by a radix16 Modified Booth Encoded multiplier, without any raise in the delay of the partial product creation Block. In this paper, we describe an optimization for binary radix-16 (modified) Booth recoded multipliers to reduce the maximum height of the partial product columns to [n/4] for n = 64-bit unsigned operands. This is in contrast to the conventional maximum height of [(n + 1)/4]. Therefore, a reduction of one unit in the maximum height is achieved. These Arithmetic multipliers increase the performance of ALU and Processors. We evaluate the proposed approach by comparison with Normal Booth Multiplier. Logic synthesis showed its efficiency in terms of delay and power consumption when the word length of each operand in the multiplier is 64bits.**

Key words **- multiplier, binary radix-16, reduction, Booth Multiplier**

I. INTRODUCTION

BINARY multipliers are a widely used building block element in the design of microprocessors and embedded systems, and therefore, they are an important target for implementation optimization.

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

A. *radix-16 partial products generation*

However, the advantage of the high radix is that the number of partial products is further reduced. For instance, for radix-16 and n-bit operands, about n/4 partial products are generated. Although less popular than radix-4, there exist industrial instances of radix-8. and radix-16 multiplier in microprocessors implementations. The choice of these radices is related to area/delay/power optimization of pipelined multipliers (or fused multiplier adder as in the case of a Intel Itanium microprocessor), for balancing delay between stages and/or reduce the number of pipelining flip-flops.

A further consideration is that carry-propagate adders are today highly energy-delay optimized, while partial product reductions trees suffer the increasingly serious problems related to a complex wiring and glitching due to unbalanced signal paths. It is recognized in the literature that a radix-8 recoding leads to lower power multipliers compared to radix-4 recoding at the cost of higher latency (as a combinational block, without considering pipelining). Moreover, although the radix-16 multiplier requires the generation of more odd multiples and has a more complex wiring for the generation of partial products, a recent microprocessor design considered it to be the best

choice for low power (under the specific constraints for this microprocessor).

In some optimizations for radix-4 two's complement multipliers were introduced. Although for n-bit operands, a total of n/2 partial products are generated, the resulting maximum height of the partial product array is n/2 + 1 elements to be added (in just one of the columns). This extra height by a single-bit row is due to the +1 introduced in the bit array to make the two's complement of the most significant partial product (when the recoded most significant digit of the multiplier is negative). The maximum column height may determine the delay and complexity of the reduction tree, authors showed that this extra column of one bit could be assimilated (with just a simplified three-bit addition) with the most significant part of the first partial product without increasing the critical path of the recoding and partial product generation stage. The result is that the partial product array has a maximum height of n/2. This reduction of one bit in the maximum height might be of interest for high-performance short-bit width two's complement multipliers (small n) with tight cycle time constraints, that are very common in SIMD digital signal processing applications. Moreover, if n is a power of two, the optimization allows to use only 4-2 carry-save adders for the reduction tree, potentially leading to regular layouts. These kind of optimizations can become particularly important as they may add flexibility to the "optimal" design of the pipelined multiplier.

II. EXISTING METHODS-MULTIPLERS

A. *Multipliers*

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets

- High speed,
- Low power consumption,
- Regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed,
- Low power and compact VLSI implementation.

The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, with increasing parallelism, the amount of shifts between the partial products and intermediate sums to be added will increase which may result in reduced speed, increase in silicon area due to irregularity of structure and also increased power consumption due to increase in interconnect resulting from complex routing. On the other hand "serial-parallel" multipliers compromise speed to achieve better performance for area and power consumption. The selection of a parallel or serial multiplier actually depends on the nature of application. In this lecture we introduce the multiplication algorithms and architecture and compare them in terms of speed, area, power and combination of these metrics. AND gates are used to generate the Partial Products (PP). If the multiplicand is N-bits and the Multiplier is M-bits then there is N* M partial product.

B. *History Of Multipliers*

The early computer systems had what are known as Multiply and Accumulate units to perform multiplication between two binary unsigned numbers. The Multiply and Accumulate unit was the simplest implementation of a multiplier. The basic block diagram of such a system is given below.

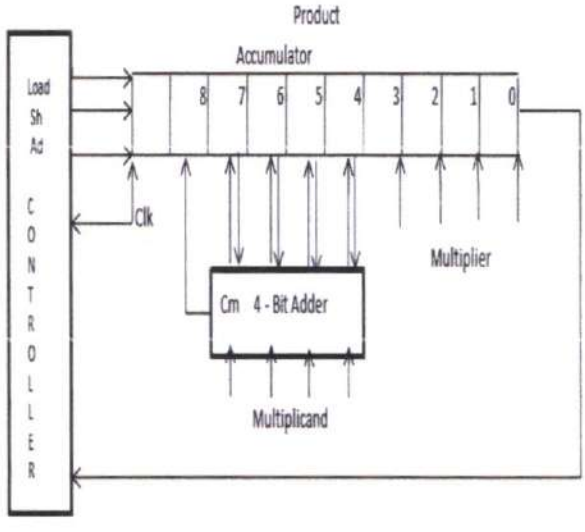


Figure 1: Multiplier Block Diagram

C. *Implementation*

The MAC unit requires a 4-bit multiplicand register, 4-bit multiplier register, a 4-

bit full adder and an 8-bit accumulator to hold the product. In the figure above the product register holds the 8-bit result. In a typical binary multiplication, based on the multiplier bit being processed, either zero or the multiplicand is shifted and then added.

III. PROPOSED MULTIPLIER

A. *Basic Radix-16 Booth Multiplier*

In this section, we describe briefly the architecture of the basic radix-16 Booth multiplier. For sake of simplicity, but without loss of generality, we consider unsigned operands with n = 64. Let us denote with X the multiplicand operand with bit components xi (i = 0 to n − 1, with the least-significant bit, LSB, at position 0) and with Y the multiplier operand and bit components yi. The first step is the recoding of the multiplier operand [8]: groups of four bits with relative values in the set {0, 1,..., 14, 15} are recoded to digits in the set {−8, −7,..., 0,..., 7, 8} (minimally redundant radix-16 digit set to reduce the number of multiples). This recoding is done with the help of a transfer digit ti and an interim digit wi [7]. The recoded digit zi is the sum of the interim and transfer digits

$$zi = wi + ti.$$

When the value of the four bits, vi, is less than 8, the transfer digit is zero and the interim digit wi = vi. For values of vi greater than or equal to 8, vi is transformed into vi = 16 − (16 − vi), so that a transfer digit is generated to the next radix-16 digit position (ti+1) and an interim digit of value wi = −(16 − v) is left. That is

$$0 \le vi < 8 : ti+1 = 0 \; wi = vi \; wi \in [0, 7]$$

$$8 \le vi \le 15 : ti+1 = 1 \; wi = -(16 - vi) \; wi \in [-8, -1].$$

The transfer digit corresponds to the most-significant bit (MSB) of the four-bit group, since this bit determines if the radix-16 digit is greater than or equal to 8. The final logical step is to add the interim digits and the transfer digits (0 or 1) from the radix-16 digit position to the right. Since the transfer digit is either 1 or 0, the addition of the interim digit and the transfer digit results in a final digit in the set {−8, −7,..., 0,..., 7, 8}.

Due to a possible transfer digit from the most significant radix-16 digit, the number of resultant radix-16 recoded digits is (n + 1)/4. Therefore, for n = 64 the number of recoded digits (and the number of partial products) is 17. Note that the most significant digit is 0 or 1 because it is in fact just a transfer digit. After recoding, the partial products are generated by digit multiplication of the recoded digits times the multiplicand X.

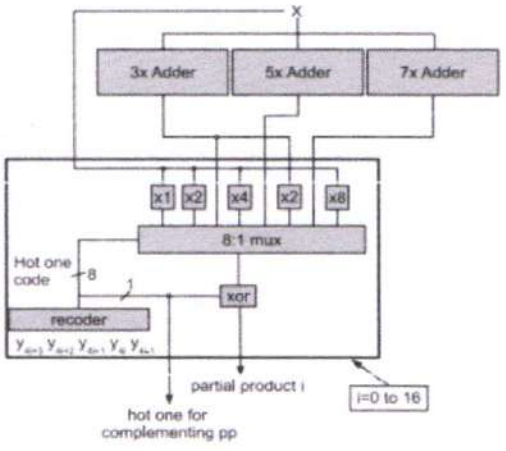


Figure 2: Partial product generation

For the set of digits {−8, −7,..., 0,..., 7, 8}, the multiples 1X, 2X, 4X, and 8X are easy to compute, since they are obtained by simple logic shifts. The negative versions of these multiples are obtained by bit inversion and addition of a 1 in the corresponding position in the bit array of the partial products. The generation of 3X, 5X, and 7X (odd multiples) requires carry-propagate adders (the negative versions of these multiples are obtained as before). Finally, 6X is obtained by a simple one bit left shift of 3X. Fig. 2.12 illustrates a possible implementation of the partial product generation. Five bits of the multiplier Y are used to obtain the recoded digit (four bits of one digit and one bit of the previous digit to determine the transfer digit to be added). The resultant digit is obtained as a one-hot code to directly drive a 8 to 1 multiplexer with an implicit zero output (output equal to zero when all the control signals of the multiplexer are zero).

The recoding requires the implementation of simple logic equations that are not in the critical path due to the generation in parallel of the odd multiples (carry-propagate addition). The XOR at the output of the multiplexer is for bit complementation (part of the computation of the two's complement when the multiplier digit is

negative). Fig. illustrates part of the resultant bit array for n = 64 after the simplification of the sign extension [7].

In general, each partial product has n + 4 bits including the sign in two's complement representation. The extra four bits are required to host a digit multiplication by up to 8 and a sign bit due to the possible multiplication by negative multiplier digits. Since the partial products are left-shifted four bit positions with respect to each other, a costly sign extension would be necessary. However, the sign extension is simplified by concatenation of some bits to each partial product (S is the sign bit of the partial product and C is S complemented): CSSS for the first partial product and 111C for the rest of partial products (except the partial product at the bottom that is non negative since the corresponding multiplier digit is 0 or 1). The bits denoted by b in Fig. corresponds to the logic 1 that is added for the two's complement for negative partial products.

After the generation of the partial product bit array, the reduction (multioperand addition) from a maximum height of 17 (for n = 64) to 2 is performed. The methods for multioperand addition are well known, with a common solution consisting of using 3 to 2 bit reduction with full adders (or 3:2 carry-save adders) or 4 to 2 bit reduction with 4:2 carry-save adders. The delay and design effort of this stage are highly dependent on the maximum height of the bit array. It is recognized that reduction arrays of 4:2 carry-save adders may lead to more regular layouts [16]. For instance, with a maximum height of 16, a total of 3 levels of 4:2 carry-save adders would be necessary. A maximum height of 17 leads to different approaches that may increase the delay and/or require to use arrays of 3:2 carry-save adders interconnected to minimize delay [20]. After the reduction to two operands, a carry-propagate addition is performed. This addition may take advantage of the specific signal arrival times from the partial product reduction step.

B. *Partial product generation stage including our proposed scheme*

To reduce the maximum height of the partial product bit array we perform a short carry-propagate addition in parallel to the regular partial product generation. This short addition reduces the maximum height by one row and it is faster than the regular partial product generation. Fig. shows the elements of the bit array to be added by the short adder.

Fig. shows the resulting partial product bit array after the short addition. Comparing both figures, we observe that the maximum height is reduced from 17 to 16 for n = 64. Fig. shows the specific elements of the bit array (boxes) to be added by the short carry-propagate addition. In this figure, pi,j corresponds to the bit j of partial product i, s0 is the sign bit of partial product 0, c0 = NOT(s0), bi is the bit for the two's complement of partial producti, and zi is the ith bit of the result of the short addition.

The selection of these specific bits to be added is justified by the fact that, in this way, the short addition delay is hidden from the critical path that corresponds to a regular partial product generation. We perform the computation in two concurrent parts A and B as indicated in Fig. The elements of the part A are generated faster than the elements of part B. Specifically the elements of part A are obtained from:

• the sign of the first partial product: this is directly obtained from bit y3 since there is no transfer digit from a previous radix-16 digit;

• bits 3 to 7 of partial product 16: the recoded digit for partial product 16 can only be 0 or 1, since it is just a transfer digit. Therefore the bits of this partial product are generated by a simple AND operation of the bits of the multiplicand X and bit y63 (that generates the transfer from the previous digit).

Therefore, we decided to implement part A as a speculative addition, by computing two results, a result with carry-in = 0 and a result with carry-in = 1. This can be computed efficiently with a compound add. Fig. shows the implementation of part A. The compound adder determines speculatively the two possible results. Once the carry-in is obtained (from part B), the correct result is selected by a multiplexer. Note that the compound adder is of only five bits, since the propagation of the carry through the most significant three ones is straightforward.

The computation of part B is more complicated. The main issue is that we need the 7 least-significant bits of partial product 15. Of course waiting for the generation of partial product 15 is not an option since we want to hide the short addition delay out of

the critical path. We decided to implement a specific circuit to embed the computation of the least-significanbits of partial product 15 in the computation of part B (and also the addition of the bit b15). Note that for the method to be correct the computation of the partial product embedded in part B should be consistent with the regular computation performed for the most significant bits of partial product 15.

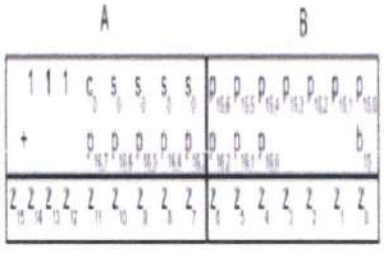


Figure 3: Detail of the elements to be added by the short addition.

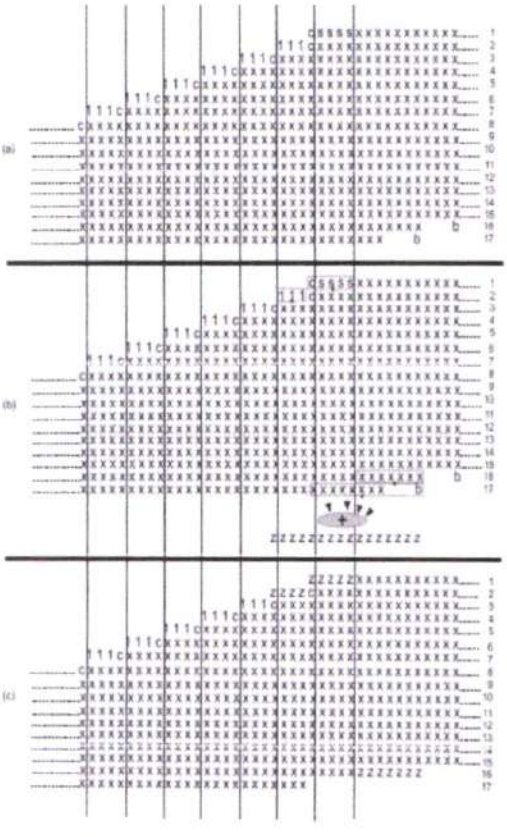


Figure 4: Radix-16 partial product reduction array

Fig. shows the computation of part B. We decided to compute part B as a three operand addition with a 3:2 carrysave adder and a carry-propagate adder. Two of the operands correspond to the least-significant bits of the partial product 15 and the other operand corresponds to the three least-significant bits of partial product 16 (that are easily obtained by an AND operation). We perform the computation of the bits of the radix-16 partial product 15 as the addition of two radix-4 partial products. Therefore, we perform two concurrent radix-4 recodings and multiple selection. The multiples of the least significant radix-4 digit are {−2, −1, 0, 1, 2}, while the multiples for the most significant radix-4 digit are {−8, −4, 0, 4, 8} (radix-4 digit set {−2, −1, 0, 1, 2}, but with relative weight of 4 with respect to the least-significant recoding). These two radix-4 recodings produce exactly the same digit as a direct radix-16 recoding for most of the bit combinations. However, among the 32 5-bit combinations for a full radix-16 digit recoding, there are six not consistent with the two concurrent radix-4 recodings. Specifically:

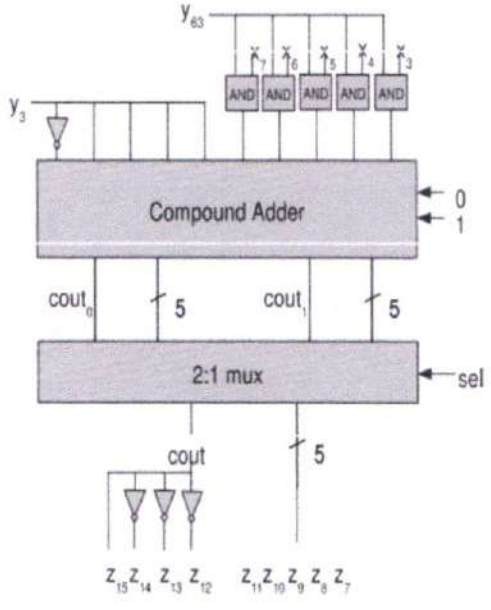


Figure 5: Speculative addition of part A

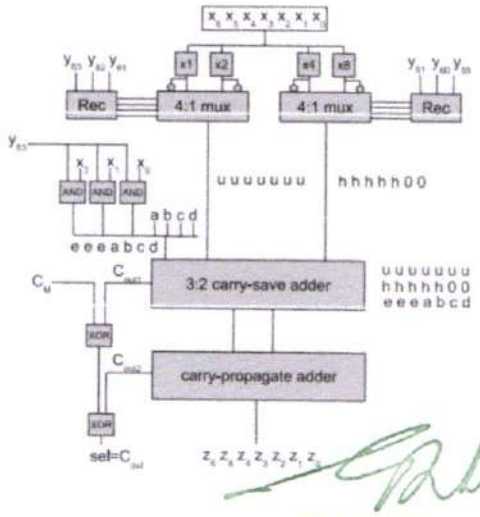


Figure 6: Computation of part B

• The bit strings 00100 and 11011 are recoded in radix-16 to 2 and −2 respectively. However, when performing two parallel radix-4 recodings the resulting digits are (4, −2) and (−4, 2) respectively. That is, the radix-4 recoding performs the computation of 2X (-2X) as 4X-2X (−4X + 2X). To have a consistent computation we modified the radix-4 recoders so that these strings produce radix-4 digits of the form (0, 2) and (0, −2).

• The bit strings 00101 and 00110 are recoded in radix-16 to 3 in both cases. However, the resulting radix-4 digits are (4, −1). This means that the radix-4 recoding performs the computation of 3X as 4X-X. To address this inconsistency problem, in this case, we decided to implement the radix-16 multiple 3X as 4X-X. This avoids the combination of radix-4 digits (2, 1) and simplifies the multiplexers in Fig.

• The bit strings 11001 and 11010 are recoded in radix-16 to −3 in both cases. However, the resulting radix-4 digits are (−4, 1). Therefore, for consistency, we proceed as in the previous case by generating the radix-16 multiple −3X as −4X + X.

In the multiplexers and place 1 in a slot of the input of the 3:2 carry-save adder with relative binary weight equal to the absolute value of the corresponding radix-4 digit. These hot ones for two's complement are indicated in Fig. 5 as the string "abcd." For instance, if the least-significant radix-4 digit is −2 and the most significant radix-4 digit is −4, then c = 1 and b = 1. Therefore, "abcd" signals are obtained directly from the selection bits of the 4:1 multiplexer. Fig. shows the recoding and partial product generation stage including the high-level view of the hardware scheme proposed. The way we compute part B may still lead to an inconsistency with the computation of the most significant part of partial product 15. Specifically, when partial product 15 is the result of an odd multiple, a possible carry from the 7 least-significant bits is already incorporated in the most significant part of the partial product. During the computation of part B we should not produce again this carry.

This issue is solved as follows. Let us consider first the case of positive odd multiples. Fig. shows that the computation of part B may generate two carry outs: the first from the 3:2 carry-save adder (Cout1), and the second from the carry-propagate adder (Cout2). To avoid inconsistencies, we detect the carry propagated to the most significant part of the partial product 15 (we call this CM) and subtract it from the two carries generated in part B. Specifically, Table I shows the truth table to generate the carry out of part B. This truth table corresponds to the XOR of the three inputs. The CM carry is obtained from a multiplexer that selects among the carry to bit position 7 from the odd multiple generators (×3, ×5, and ×7), the carry to bit position 6 from the multiple generator ×3 (to get the carry to position 7 of multiple ×6), or carry zero for the other multiples. The resultant carry out is the selection signal used in the multiplexer of part A.

For negative odd multiples we use a similar scheme. In this case the output of adder is complemented, but the only information available about the carry to position 7 is obtained directly from the adders that generate the positive odd multiple. Next, we show how to obtain the carry to the most significant part of the resultant complemented odd multiple from the carry to position 7 obtained from the adders. Let us call M the result of the positive odd multiple (output of the adder), and express

$$M \text{ as } M = N + P \qquad (1)$$

with P being the seven least-significant bits of the result from the adder, and N the remaining most significant bits of the result of the adder. Let us express N in terms of C7 (carry to position 7)

$$N = Q + C727 \qquad (2)$$

that is, Q are the remaining most significant bits of the positive odd multiple minus the carry to position 7. Assuming a m bit partial product, the complement of M is expressed as

$$M = 2n - 1 - M = 2n - 1 - N - C727 - Q \qquad (3)$$

By adding and subtracting 27 and rearranging terms results in

$$M = 2n - 27 - N - C727 + 27 - 1 - Q \qquad (4)$$

We identify the terms $N = 2n - 27 - N$ and $Q = 27 - 1 - Q$. Taking into account these terms and adding and subtracting 27 and 2n−1 results in

$$M = -2n-1 + N + (2n-1 - 27) + (1 - C7)27 + Q \qquad (5)$$

The term $(1 - C7)27 + Q = C7 + Q$ is computed in part B of the proposed scheme (see Fig. 2.17), but $(1 - C7)27 = C7$ is also part of the most significant part of partial product 15. Therefore, for a negative partial product we need to subtract C7. In summary, we take CM as the carry to position 7 of the adders that generates the multiple when the

partial product is positive, and complement this carry, when the partial product is negative.

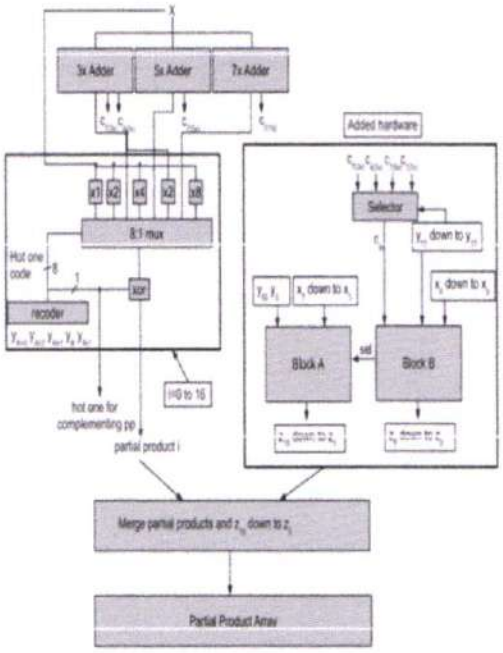


Figure 7: High level view of the recoding and partial product generation stage including our proposed scheme

IV. BOOTH MULTIPLICATION

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. The algorithm was invented by Andrew Donald Booth in 1950 while doing research on crystallography at Birkbeck College in Bloomsbury, London.[1] Booth's algorithm is of interest in the study of computer architecture.

A. *The algorithm*

Booth's algorithm examines adjacent pairs of bits of the 'N'-bit multiplier Y in signed two's complement representation, including an implicit bit below the least significant bit, $y_{-1} = 0$. For each bit y_i, for i running from 0 to $N - 1$, the bits y_i and y_{i-1} are considered. Where these two bits are equal, the product accumulator P is left unchanged. Where $y_i = 0$ and $y_{i-1} = 1$, the multiplicand times 2^i is added to P; and where $y_i = 1$ and $y_{i-1} = 0$, the multiplicand times 2^i is subtracted from P. The final value of P is the signed product. The representations of the multiplicand and product are not specified; typically, these are both also in two's complement representation, like the multiplier, but any number system that supports addition and subtraction will work as well. As stated here, the order of the steps is not determined. Typically, it proceeds from LSB to MSB, starting at $i = 0$; the multiplication by 2^i is then typically replaced by incremental shifting of the P accumulator to the right between steps; low bits can be shifted out, and subsequent additions and subtractions can then be done just on the highest N bits of P.[2] There are many variations and optimizations on these details. The algorithm is often described as converting strings of 1s in the multiplier to a high-order +1 and a low-order −1 at the ends of the string. When a string runs through the MSB, there is no high-order +1, and the net effect is interpretation as a negative of the appropriate value.

B. *Booth's Algorithm Flowchart*

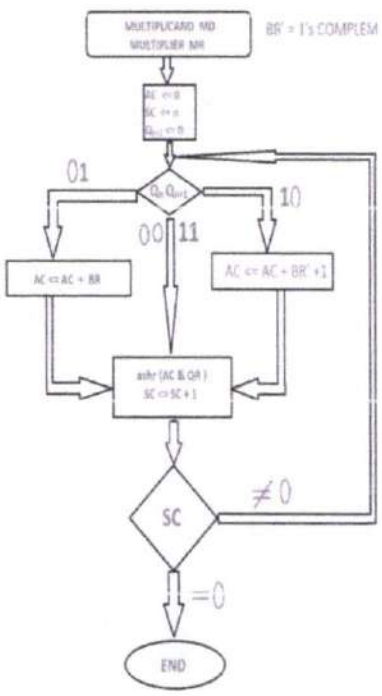


Figure 8: Booth's Algorithm Flowchart

AC and the appended bit Qn+1 are initially cleared to 0 and the sequence SC is set to a number n equal to the number of bits in the multiplier. The two bits of the multiplier in Qn and Qn+1are inspected. If the two bits are equal to 10, it means that the first 1 in a string has been encountered. This requires a subtraction of the multiplicand from the partial product in AC. If the 2 bits are equal to 01, it means that the first 0 in a string of 0's has n = been

encountered. This requires the addition of the multiplicand to the partial product in AC.

When the two bits are equal, the partial product does not change. An overflow cannot occur because the addition and subtraction of the multiplicand follow each other. As a consequence, the 2 numbers that are added always have a opposite signs, a condition that excludes an overflow. The next step is to shift right the partial product and the multiplier (including Qn+1). This is an arithmetic shift right (ashr) operation which AC and QR ti the right and leaves the sign bit in AC unchanged. The sequence counter is decremented and the computational loop is repeated n times.

V. SIMULATION RESULTS

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	21	4656	0%
Number of 4 input LUTs	37	9312	0%
Number of bonded IOBs	16	232	6%

Figure 9: Design summary

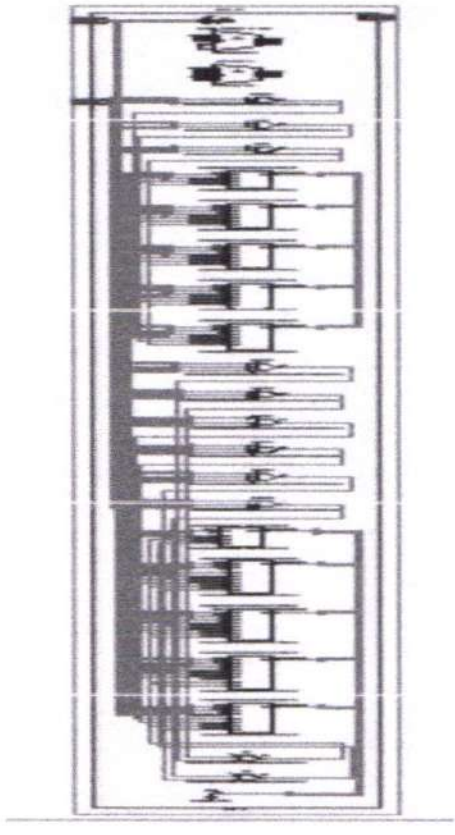


Figure 10: RTL schematic

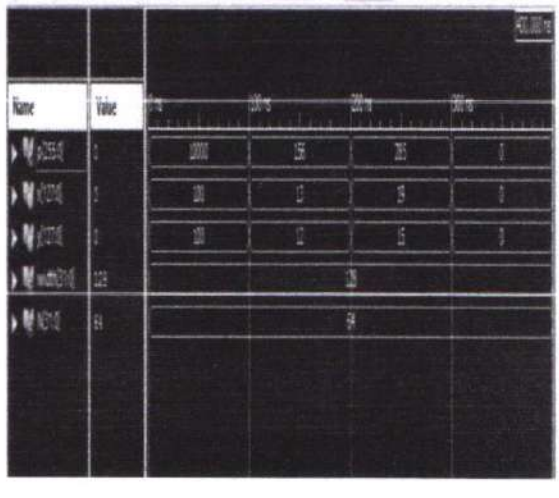


Figure 11: Simulation results

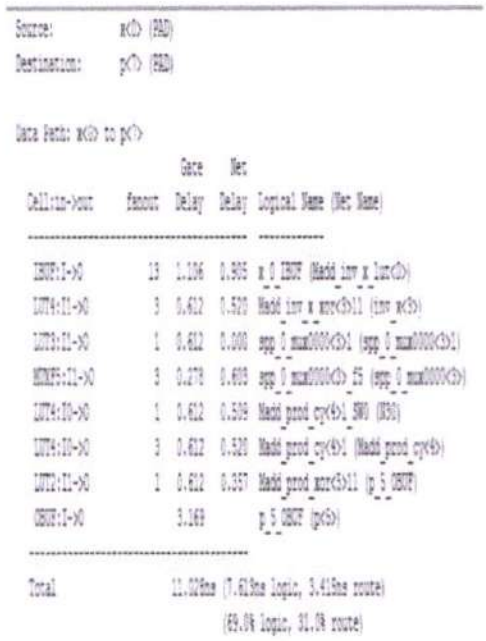


Figure 12: Time Summary

VI. CONCLUSION

Pipelined large wordlength digital multipliers are difficult to design under the constraints of core cycle time (for nominal voltage), pipeline depth, power and energy consumption and area. Low level optimizations might be required to meet these constraints. In this work, we have presented a method to reduce by one the maximum height of the partial product array for 64-bit radix-16 Booth recoded magnitude multipliers. This reduction may allow more flexibility in the design of the reduction tree of the pipelined multiplier. We have shown that this reduction is achieved with no extra delay for n $\geq$ 32 for a cell-based design. The method can be extended to Booth recoded radix-8 multipliers, signed multipliers and combined signed/unsigned multipliers. Radix-8 and radix-16 Booth recoded multipliers are attractive for low power designs, mainly to the lower complexity and depth of the reduction tree, and therefore they might be very popular in this era of power-constrained designs with increasing overheads due to wiring.

VII. FUTURE SCOPE

we will extend an optimization for binary radix-32 (modified) Booth recoded multipliers to reduce the maximum height of the partial product columns to [n/4] for n = N-bit unsigned operands. This is in contrast to the conventional maximum height of [(n + 1)/4]. Therefore, a reduction of one unit in the maximum height is achieved. This reduction may add flexibility during the design of the pipelined multiplier to meet the design goals, it may allow further optimizations of the partial product array reduction stage in terms of area/delay/power and/or may allow additional addends to be included in the partial product array without increasing the delay. The method can be extended to Booth recoded radix-8 multipliers, signed multipliers, combined signed/unsigned multipliers, and other values of n.

REFERENCES

[1] I. Blake, G. Seroussi, andN.P.Smart, Elliptic Curves in Cryptography,ser. London Mathematical Society Lecture Note Series.. Cambridge,U.K.: Cambridge Univ. Press, 1999.

[2] N. R. Murthy and M. N. S. Swamy, "Cryptographic applications of brahmaqupta-bha skara equation," IEEE Trans. Circuits Syst. I, Reg.Papers, vol. 53, no. 7, pp. 1565–1571, 2006.

[3] L. Song and K. K. Parhi, "Low-energy digit-serial/parallel finite field multipliers," J. VLSI Digit. Process., vol. 19, pp. 149–C166, 1998.

[4] P. K. Meher, "On efficient implementation of accumulation in finite field over GF(2^m) and its applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 4, pp. 541–550, 2009.

[5] L. Song, K. K. Parhi, I. Kuroda, and T.Nishitani, "Hardware/software codesign of finite field datapath for low-energy Reed-Solomn codecs,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8, no. 2, pp.160–172, Apr. 2000.

[6] G. Drolet, "A new representation of elements of finite fields GF(2^m) yielding small complexity arithmetic circuits," IEEE Trans. Comput.,vol. 47, no. 9, pp. 938–946, 1998.

[7] C.-Y. Lee, J.-S. Horng, I.-C. Jou, and E.-H. Lu, "Low-complexity bit-parallel systolic montgomery multipliers for special classes of GF(2^m)," IEEE Trans. Comput., vol. 54, no. 9, pp. 1061–1070, Sep. 2005.

[8] P. K. Meher, "Systolic and super-systolic multipliers for finite field GF(2^m) based on irreducible

trinomials," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 4, pp. 1031–1040, May 2008.

[9] J. Xie, J. He, and P. K. Meher, "Low latency systolic montgomery multiplier for finite field GF(2^m) based on pentanomials," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 2, pp. 385–389, Feb.2013.

[10] H.Wu, M. A. Hasan, I. F. Blake, and S. Gao, "Finite field multiplier using redundant representation," IEEE Trans. Comput., vol. 51, no. 11, pp. 1306–1316, Nov. 2002.

[11] A. H. Namin, H. Wu, and M. Ahmadi, "Comb architectures for finite field multiplication in F_{2^m} ," IEEE Trans. Comput., vol. 56, no. 7, pp. 909–916, Jul. 2007.

[12] A. H. Namin, H. Wu, and M. Ahmadi, "A new finite field multiplier using redundat representation," IEEE Trans. Comput., vol. 57, no. 5, pp. 716–720, May 2008.

[13] A. H. Namin, H.Wu, and M. Ahmadi, "A high-speed word level finite field multiplier in F_{2^m} using redundant representation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 10, pp. 1546–1550,Oct. 2009.

[14] A. H. Namin, H. Wu, and M. Ahmadi, "An efficient finite field multiplier using redundant representation," ACMTrans. Embedded Comput. Sys., vol. 11, no. 2, Jul. 2012, Art. 31.

[15] North Carolina State University, 45 nm FreePDK wiki [Online]. Available:http://www.eda.ncsu.edu/wiki/FreePDK 45:Manual

PRINCIPAL
Avanthi Institute of Engg. & Tech.
Guntihapally (V), Abdullapurmet (Mdl.), R.R. Dist.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Design Of High-Speed Area Efficient Mac Unit Using Reversible Logic

K Vamshinadh
MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kvamshinadh94@gmail.com

Dr.S. Kishore Reddy
Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

V Guravaiah
Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: guravaiahvemuri@gmail.com

Abstract—we propose a low-power high-speed pipeline multiply-accumulate (MAC) architecture. In a conventional MAC, carry propagations of additions (including additions in multiplications and additions in accumulations) often lead to large power consumption and large path delay. To resolve this problem, we integrate a part of additions into the partial product reduction (PPR) process. In the proposed MAC architecture, the addition and accumulation of higher significance bits are not performed until the PPR process of the next multiplication. To correctly deal with the overflow in the PPR process, a small-size adder is designed to accumulate the total number of carries. Compared with previous works, experimental results show that the proposed MAC architecture can greatly reduce both power consumption and circuit area under the same timing constraint.

***Index Terms*— MAC architecture, bits, adder, power consumption**

I. INTRODUCTION

The multiply-accumulate (MAC) unit is a fundamental block for digital signal processing (DSP) applications. Especially, in recent years, the development of real-time edge applications has become a design trend. Thus, there is a strong demand for high-speed low-power MAC units. A conventional MAC unit is composed of two individual blocks: a multiplier and an accumulator (i.e., an accumulate adder). An N-bit MAC unit includes an N-bit multiplier and a (2N+α-1)-bit accumulator (adder), where α is the number of guard bits used to avoid overflow (caused by long sequences of multiply-accumulate operations). A lot of previous works paid attention to the optimization of multiplier and the optimization of adder, respectively. A multiplier usually has three steps. The first step is the partial product generation (PPG) process. For example, AND gates can be used to generate a partial product matrix (PPM) for an unsigned multiplication. The second step is the partial product reduction (PPR) process. By using the Dadda tree approach or the Wallace tree approach, the PPM can be reduced to become two rows. The third step is the final addition. An adder (called the final adder) is used to perform the summation of the final two rows.

A. Multiplier

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has an important part in low-power VLSI system design. A system is generally determined by the performance of the multiplier because the multiplier is generally the slowest element and more area consuming in the system. Hence optimizing the speed and area of the multiplier is one of the major design issues. However, area and speed are usually conflicting constraints so

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

that improvements in speed results in larger areas. Multiplication is a mathematical operation that include process of adding an integer to itself a specified number of times. A number (multiplicand) is added itself a number of times as specified by another number (multiplier) to form a result (product). Multipliers play an important role in today's digital signal processing and various other applications. Multiplier design should offer high speed, low power consumption. Multiplication involves mainly 3 steps

1. Partial product generation

2. Partial product reduction

3. Final addition

II. EXISTING METHOD

In this section, we present the proposed two-stage (i.e., two cycle) MAC architecture. The first stage performs the PPG process, the PPR process (based on the PPM that combines the PPG result and the accumulation result), the (2N-k-1)-bit addition (i.e., a part of the final addition) and the αbit addition (for dealing with the overflow in the PPR process). Then, the second stage performs the (k+α)-bit addition to produce the accumulation result. The main features of the proposed architecture are below. λ To reduce the lengths of carry propagations, we integrate a part of additions into the PPR process. λ To handle overflow in the PPR process, a α-bit adder is used to count the total number of carries. λ By applying the gating technique, the second stage can only be executed in the last cycle (of the entire sequence of multiply-accumulate operations) for power saving. The proposed two-stage pipeline MAC unit is displayed in Fig. 2. Our PPM (for the PPR process) is composed of two PPMs: one PPM is derived by the PPG and the other PPM is derived by the accumulation. For an unsigned MAC unit, in the PPG process, "AND" gates can be directly used to generate the PPM. For a signed MAC unit, because the influences of the sign bit should be taken into account, several PPG algorithms have been proposed to generate the signed PPM. In the proposed architecture, the Baugh-Woolley algorithm is adopted in the PPG process to generate the signed PPM.

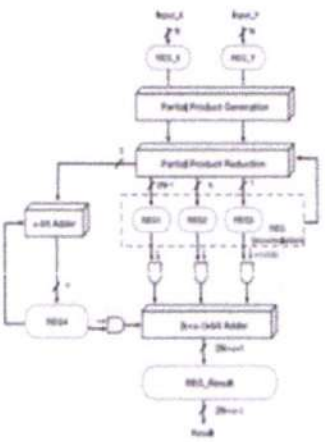


Figure 1.MAC architecture

We have implemented a tool (a C++ program) to automatically generate the proposed N-bit MAC in Verilog RTL description. The users can specify the value of N and the value of k for automatic generation, where k denotes the number of higher significance bits whose additions (accumulation) are not performed in the final addition. Note that the value of k is equal to the bit width of register REG2. In our experiments, we specify the value of N to be 16 (i.e., 16-bit MAC). Besides, we assume that the maximum number of multiplications in each multiply-accumulate operation is 256. Thus, the number of guard bits (i.e., the value of α) is set to be 8. We have implemented several different configurations of the proposed MAC architecture. For the convenience of presentation, we use the term Ours_k for the naming of each configuration, where k represents the bit width of register REG2. In our experiments, these Verilog RTL descriptions are synthesized to gate-level netlists and targeted to TSMC 40 nm cell library by using Synopsys Design Compiler.For comparisons, we also implemented the following two MAC architectures: the conventional MAC architecture and the state-of-the-art MAC architecture. In the conventional MAC architecture, the MAC unit is composed of two individual blocks (i.e., a multiplier and an accumulator). On the other hand, in the state-of-the-art MAC architecture, the multiplier and the accumulator are tightly integrated (i.e., a carry-save format is sent to the accumulator without being added to only one vector).

The systolic array has been widely used in the hardware acceleration for matrix multiplication. In recent years, several research efforts have been paid to map the inference of a convolutional neural network to a systolic array. Note that a systolic array is composed of multiple processing elements (PEs). Each PE corresponds to a MAC unit. In this section, we address the application of the proposed MAC architecture to a systolic array. Figure gives the block diagram of the PE based on the conventional MAC architecture. Note that the PE is a two-stage (i.e., two-cycle) pipeline design. The inputs of the PE are x and y. The block MUL denotes the multiplier. In the first stage, the multiplier performs the multiplication. Then, the output of the multiplier is stored in a register. In the second stage, the accumulator performs the accumulation. Then, the accumulation result is stored in register result.

III. Proposed Method

In data transmission applications, the widely used public-key cryptosystem is a simple and efficient Montgomery multiplication algorithm such that the low-cost and high-performance. In which includes encryption and decryption process. The Montgomery multiplier receives and outputs the data with binary representation and uses only one-level carry-save adder (CSA) to avoid the carry propagation at each addition operation. This CSA is also used to perform operand pre-computation and format conversion from the carry save format to the binary representation, leading to a low hardware cost and short critical path delay at the expense of extra clock cycles for completing one modular multiplication. To overcome the weakness, A configurable CSA (CCSA), which could be one full-adder or two serial half-adders, is proposed to reduce the extra clock cycles for operand pre-computation and format conversion by half. When modular multiplier is done with CCSA technique and it has some drawbacks. The drawbacks are short critical path, high power consumption. To overcome the drawbacks the CCSA is replaced with PASTA (Parallel Self Timed Adder) in the Montgomery modular multiplier. The PASTA adder can achieve less power consumption.

Modular Multiplication is the central operation in many application areas including public key cryptography for encryption and decryption. The widely used method for modular multiplication is Montgomery modular multiplier. In which there will be a carry save adder . X´Y mod M is the operation to be performed. In which X and Y are the inputs. It is necessary to find the value of mod M, henceforth going for this algorithm. Comparing all previously occurring algorithms, this algorithm will produce the optimized output. There are two cases, semi carry save addition and full carry save addition. In this semi carry save addition, the given inputs are in binary and the inter outputs alone in carry save. Whereas in full carry addition, both inputs and inter outputs are in carry save. On comparing, it can be seen that semi carry save is the most advantageous one because it has only one carry save and hence it has less area and high speed which is required for designing an VLSI based multipliers.

Consider the modulus N to be a k-bit odd number and an extra factor R is to be defined as 2k mod N, where $2k-1 \leq N < 2k$. Given two integers a and b, where a, b

$$A = a \times R \pmod{N} \qquad (1)$$

$$B = b \times R \pmod{N} \qquad (2)$$

In this existing system, carry save addition with semi-carry approach is described. In which all the multiplicands are not recycled, that is whatever the multiplicand is needed to be multiplied at that time alone is used for determining the output. The carry save approach has higher benefits since it is the basic key for operating a Montgomery modular multiplier. In such a way, using this semi carry save type only one carry level adder is implemented which may be two serial half adders or a full adder can be used based on the requirement. It thereby reduces the number of clock cycles and hence less delay. So the output will be optimized and it can be implemented using Verilog coding.

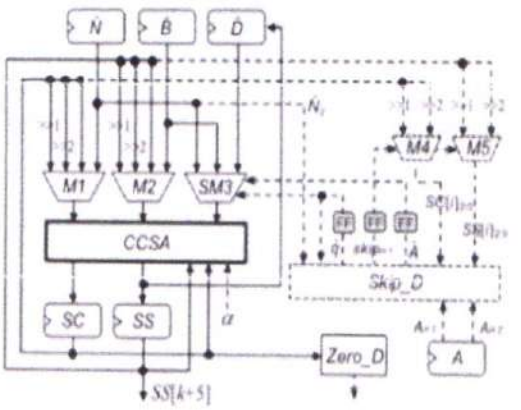


Figure 2. Block diagram of Montgomery Modular Multiplication using CCSA

The above architecture is the semi-carry save based Montgomery multiplier. In which the loop is reduced on comparing to the existing one. It consists of two multiplexers, one multiplier, one configurable carry save adder, flip-flops, skip detector and zero detector.

Illustrates the block diagram of proposed semi carry save multiplier. It is first used to precompute the four-to-two carry save additions. Then the required multiplication can be performed. The modulus N and inputs will be allowed inside the twomultiplexers. This partial product is then allowed inside the multiplier. Those partial outputs then enter into configurable carry save adder, where the carry save addition operation is performed. They are stored in the flip flops temporarily. When another partial output is executed, then that will be stored in the flip flop. The Skip detector will skip the previous multiplication which is not required in the operation so as to reduce the number of clock cycles. The partial product from SM3 is allowed to the multiplexers M4 and M5. Later on it allows inside the flip flops for temporary storage, then to the skip detector. The output can be obtained from semi carry. This process is repeated until the output is obtained. The zero detectors can also be used to detect zero in many situations, which is most required. The complexity is very less compared to the previous one.

Critical Path Delay Reduction In order to reduce the critical path delay, the operations in semi carry save and full carry save is performed jointly. The carry save format conversion as well as the binary format should be taken place. Then pre-computation must be done in order to reuse the multiplicand values. Another method is using zero detectors. SC will produce the output only when the zero is detected. Then the pre computation can be done i-1 iteration.

Clock Cycle Number Reduction In order to decrease the clock cycle number, a configurable carry save architecture to perform one three-input carry-save addition or two serial two-input carry-save addition is used. Furthermore the number of iteration can also be reduced to reduce number of clock cycles. Then a signal skip is used. In order to verify whether i+1 is required or not to be happen in the upcoming events. This can be found in the previous i iteration itself. By again using the same condition, signal skip will use i+1, so that it increases by a factor 2. Hence it directly goes to i+2. So that clock cycle gets reduced.

Quotient Pre-computation: Ai+1, Ai+2 and qi+1, qi+2 should be known already in order that the unwanted steps in the (i +1) iteration can be reduced by determining i iteration. So as to pre compute the quotients. Another method is using skip detector so that it will pre computes the values. And also since the shortest path in this multiplier is lengthened, it has to be minimized. As modulus N is an odd number, it can be used directly for the multiplication. So that time is consumed highly.

To increase the Speed of Operation we are replacing the CSA with PASTA (Parallel self timed adder) in the proposed architecture.

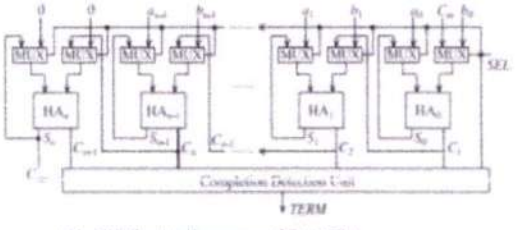


Fig.3.Block diagram of PASTA

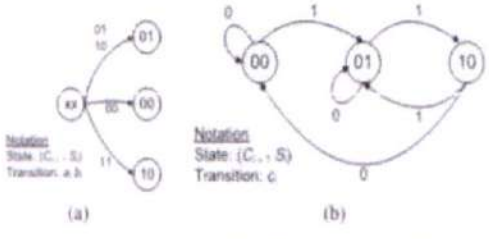


Fig.4. State diagram of PASTA (a).Initial Phase (b).Iterative Phase

Montgomery multiplication is to perform fast modular multiplication(MM).PASTA adder using in Montgomery modular multiplication is to reduced area and clock cycles.To design a simple and efficient radix-2 Montgomery Modular multiplication with Parallel Self Timed Adder (PASTA).The design of PASTA is uses half adders (HAs) along with multiplexers requiring minimal interconnections. The selection input for two-input multiplexers corresponds to the Request handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL=0andwill switch to feedback/carry paths for subsequent iterations using SEL=1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero values are show in Fig .3. In Fig. 4, two state diagrams are drawn for the initial phase and the iterative phase of the

proposed architecture. Each state is represented by (Ci+1 Si) pair where Ci+1, Si represent carry out and sum values, respectively, from the ith bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state (11) cannot appear.

The proposed architecture of Montgomery Modular Multiplication using PASTA adder, which consists of one one-level Parallel Self Timed Adder(PASTA) architecture, two 4-to-1 multiplexers (M1 and M2) one simplified multiplier SM3, one skip detector Skip_D, one zero detector Zero_D, and six registers. Zero detector Zero_D is used to detect SC is equal to zero. The Skip_D is composed of four XOR gates, three AND gates, one NOR gate, and two 2-to-1 multiplexers the skip detector is used to detect the unnecessary multiplication operations.

The design has been implemented using Xilinx Verilog coding. For further verification, the design can be done using Cadence. It can be clearly understand by the waveform shown below. It can be proven that it has reduced area complexity and speed complexity on comparing to all other multipliers. The method has been implemented using a configurable carry save adder so as to prove the maximum delay to be less comparing all. The delay and area can be minimized as much as possible as comparing to all other previous existing architectures.

IV. Conclusion

This paper presents low-power high-speed two-stage pipeline MAC architecture for real-time DSP applications. Our basic idea is to integrate a part of additions (including a part of the final addition in the multiplication and a part of the addition in the accumulation) into the PPR process. As a result, critical path delays and power dissipations caused bycarry propagations can be reduced. To correctly deal with the overflow during the PPR process, an α-bit accumulator is used to count the total number of carries. Experimental results consistently show that the proposed approach works well in practice. The proposed MAC architecture is applicable to both the design of an unsigned MAC unit and the design of a signed MAC unit. Note that the only differences between the unsigned MAC unit and the signed MAC unit are the PPM structure and the α-bit addition mechanism. Moreover, the proposed MAC architecture is also applicable to the systolic array (for performing the matrix multiplication). Implementation data show that, compared with the systolic array based on the conventional PE (i.e., the conventional MAC architecture), the systolic array based on the proposed PE (i.e., the proposed MAC architecture) can greatly reduce both circuit area and power consumption under the same timing constraint.SCS-based multipliers maintain the input and Output operands of the Montgomery MM in the carrysave format to escape from the format conversion, leading to fewer clock cycles but smaller area than FCS-based multiplier. In the existed architecture disadvantages are carry propagation delay and extra clock cycles. To overcome the disadvantages we go for PASTA adder. The PASTA adder is using in Montgomery Modular Multiplier in these advantages are low hard ware cost short critical path delay and required clock cycles are reduced for completing one MM operation.

References

[1] V.Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137,Jan. 2013.

[2] [2] E. J. King and E. E. Swartzlander, Jr., "Data-dependent truncation scheme for parallel multipliers," in Proc. 31st Asilomar Conf. Signals, Circuits Syst., Nov. 1998, pp. 1178–1182.

[3] [3] K.-J. Cho, K.-C. Lee, J.-G. Chung, and K. K. Parhi, "Design of low-error fixed-width modified booth multiplier," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 522–531, May 2004.

[4] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 850–862, Apr. 2010.

[5] Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," IEEE Trans. Comput., vol. 64, no. 4, pp. 984–994, Apr. 2015.

[6] S. Narayanamoorthy, H. A. Moghaddam, Z. Liu, T. Park, and N. S. Kim, "Energy-efficient approximate multiplication for digital signal processing and classification applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 6, pp. 1180–1184, Jun. 2015.

[7] G. Zervakis, K. Tsoumanis, S. Xydis, D. Soudris, and K. Pekmestzi, "Design-efficient approximate multiplication circuits through partial product perforation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,vol. 24, no. 10, pp. 3105–3117, Oct. 2016.

[8] P. Kulkarni, P. Gupta, and M. D. Ercegovac, "Trading accuracy for power in a multiplier architecture," J. Low Power Electron., vol. 7, no. 4, pp. 490–501, 2011.

[9] C.-H. Lin and C. Lin, "High accuracy approximate multiplier with error correction," in Proc. IEEE 31st Int. Conf. Comput. Design, Sep. 2013, pp. 33–38.

[10] Liu, J. Han, and F. Lombardi, "A low-power, high-performance approximate multiplier with configurable partial error recovery," in Proc. Conf. Exhibit. (DATE), 2014, pp. 1–4.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Design of Power and Area Efficient Approximate Multipliers

T Pooja

MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: poojahoney2025@gmail.com

Dr. S. Kishore Reddy

Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg.&Tech., India.
Email: kishorereddy416@gmail.com

***Abstract*-Compression of data is a common practise in the signal - processing & digital image analysis fields, and is often employed for multimedia & image processing purposes. Approximate computation is a prominent design approach in arithmetic. New high-speed areas may be opened up by high-speed multimedia applications. Error-tolerant circuits that use approximate computations. At the same time, these applications give great production at a reduced cost of accuracy In addition, the system's complexity is reduced as a result of their implementations. Power consumption and latency in the system's architecture are the main factors. It is proposed that two compressors be designed and analyzed that have smaller size, less delay, and more power than the present systems, all while maintaining precision that is equivalent to the current systems. All designs were tested and forecasted on area, delay, power (PDP), Margin Of error (ER), Range of Error (ED), & Accurate Output Count (AOC) before being implemented in 45 nm CMOS technology (the AOC). In comparison to an exact 4:2 compressor, the suggested 4:2 compressor with approximation has an overall decrease of 56.80 percent and 57.20 percent Power and delayed reduction of 73.30 percent Dadda multipliers of 8 × 8 and 16 x 16 are used in the suggested compressors. There's a comparable level of precision in these multipliers compared to current technology. Image smoothing & propagation are two examples of error-tolerant applications that will benefit from the architecture now under consideration.**

Keywords- Signal – processing, Digital image analysis, Multimedia, Error tolerant, AOC, CMOS.

1. INTRODUCTION

Exact computing units aren't necessarily essential in applications like data mining and multimedia signal processing. They may be substituted with a similar item. Research into error-tolerant applications using approximation computation is on the increase. These applications rely heavily on adders and multipliers.

Manuscript received Dec 10, 2022; Revised Dec 25, 2022; Accepted Dec 31, 2022

In digital signal processing, approximate complete adders are suggested at the transistor level. Partial product accumulation in multipliers is handled by their suggested full-adder design. The use of truncation in fixed-width multiplication designs is common to simplify the circuitry. In order to compensate again for quantization error induced by the reduced portion, a variable correction component is added.

Accumulation of bits is critical in terms pf power usage when using approximation methods in multipliers. If the least relevant bits of the inputs can be trimmed, then partial products may be formed in order to decrease hardware complexity. In partial product accumulations, the suggested multiplier saves just a few adder circuits. A partial product reduction trees of four 8 x 8Dadda multiplier variations is given and applied with two types of roughly 4-2 compressors. Mean relative error (MRE) is greatly affected by the suggested compressors in that they produce nonzero output for zero-valued inputs, which is a severe negative. In this brief, an estimated design is presented to address the current issue. As a result, accuracy is improved. When a segment multiplier (SSM) is used, the leading 1 bit of each operand is used to generate an output of m-bit segments. Then, instead of n n multiplication, m m multiplication is used. A partial product perforation (PPP) multiplier in an n-bit multiplier omits subsequent partial products beginning at position j, where j [0,n-1] and k [1, min (n-j, n-1)]. Multiplying an element in the Karnaugh map by 2 is used as a building block to produce 4 4 and 8 8 multiplications. Power-efficient Wallace tree multipliers might benefit from an inaccurate counter design. The multiplier partial product accumulation is handled by a new approximation adder. Compared to an accurate multiplier, a 16-bit

approximation multiplier achieves a 26% decrease in power.

Voltage over-scaling (VOS) is used to approximate an 8-bit Wallace tree multiplier. Errors may be caused by lowering the supply voltage, which produces routes that do not match delay restrictions. In the past, logic complexity reduction has been achieved by simply applying approximation adders and compressor to the partial products. Various probabilities are included into the partial products in this short. Systematic approximation is used to examine the likelihood statistics of the changing partial products.

Approximation is suggested using half-adder, full-adder, and 4-2 compressors. The complexity of the arithmetic units has been lowered, but the error value has also been taken into consideration. Systemic approximation improves accuracy, while lower logic architecture of approximation arithmetic units reduces power and area consumption. Image processing applications benefit from improved peak signal-to-noise ratio (PSNR) values achieved by the suggested multipliers over previous designs. The arithmetic separation between a proper output and an approximation output for just a given input may be characterised as the error distance (ED).

In order to assess and normalise approximation adders, It is argued that ED (NED) is a virtually invariant metric regardless of the approximate circuit's dimensions. For both current and proposed multiplier designs, the conventional error analysis, MRE, is discovered Here are the sections of this brief. Section II lays forth the architecture that is being suggested. Design & error metrics of proposed and current approximation multipliers are examined extensively in Section III. An image processing programme uses the suggested multipliers, and results are shown in Section IV. Finally, Section V wraps things off here.

2. LITERATURE SURVEY

A. Approximate Adders for approximate multiplication

Document It's becoming more difficult for CMOS technology to keep up with the demands of future applications. This gap may be narrowed greatly with the help of numerous viable design methods. Accurate computation is one of them, although it has received the most attention in recent years. Accuracy is sacrificed for speed and energy efficiency in approximation computing, which harnesses the inherent fault of applications and provides highly energetic hardware and software implementations (e.g., performance and energy). There has been a lot of study on approximate computing over the last decade, but much of it has focused on adders, which are hardware abstractions. There is a comparative study of the current state of the art in approximation adders. Both traditional design measurements and approximation computing metrics are available for comparison.

B. Approximate Compressors for Multiplication

At the nanometer scale, approximate computing is a promising paradigm for digital processing. For computer arithmetic designs, inexact computing is especially intriguing. In order to be used in a multiplier, the authors discuss the study and construction of two novel compressors with an approximate 4-2 compression ratio. In order to fulfil circuit-based figures of merit, these designs depend on various compression characteristics that allow imprecision in calculation (measured by error rate and so-called normalised error distance) to meet (number of transistors, delay and power consumption). A Dadda multiplier may be multiplied using four distinct techniques for using the suggested approximation compressors. Applicability of the approximation multipliers towards image processing is shown in a series of simulations. There are substantial decrease in power consumption, delay and number of transistors compared to that of an exact design; two of the suggested multiplicand designs provide performance of the system for image multiplication to respect to average normalised error distance as well as peak signal-to-noise ratio (and over 50dB again for considered image examples).

C. Approximate Wallace-Booth Multiplier

The potential benefits of improved performance and reduced power consumption offered by approximate and inexact computing have lately gained a lot of attention. There are three parts to this approximation multiplier: a Booth encoder, a 4-2 compressor, and an approximation tree structure. For 8x8, 16x16, & 32x32-bit signed multiplication schemes, the approximate design is built and tested. This paper presents and discusses simulation findings for 45 nm technology. The suggested approximate multiplier produces considerable improvements in energy usage, latency, and combined metrics when compared to an accurate Wallace-Booth multiplier and other approximate multipliers available in the technical literature. These findings support the feasibility of the concept as presented.

D. Two variants of approximate multipliers

For error-tolerant applications, approximate computing may reduce design complexity while increasing performance and power efficiency. A novel method for approximating multipliers is explored. Probability terms may be

added by altering the multiplier's partial products. The chance of accumulating changed partial products has an effect on the logic complexity of approximation. Two different kinds of 16-bit multipliers make use of the suggested approximation. The results of the synthesis show that two suggested multipliers save 72 percent and 38 percent of the power of an exact multiplier, respectively. When compared to other approximation multipliers, they are more precise. Image processing is used to test the suggested multipliers, and one model gets the best peak signal power of all of them.

Energy-constrained devices are increasingly being required to serve a wide range of digital signal analysis (DSP) and classifying applications. Such applications often use fixed-point arithmetic to execute matrix multiplications while allowing for certain computational mistakes. As a result, multiplication efficiency must be improved. Finally, the exhibited computational mistake has no significant influence on DSP quality or classification accuracy.

3. EXISTING METHOD

A redundant binary (RB) format may be utilised to create high-performance multipliers because of its flexibility and carry-free addition. The traditional RB multiplier adds an extra RB partial product (RBPP) row, since an error-correcting word (ECW) is produced both by the radix-4 Modified Booth encoding (MBE) or the RB encoding. For the MBE multiplier, this means an extra RBPP accumulation step. To save one RBPP accumulation step, a novel RB altered bits generator (RBMPPG) has been developed in this study. RBMPPG is less wasteful than RB MBE multiplier because it creates fewer incomplete product rows. When the length of each multiplier operand is at least 32 bits, simulation findings demonstrate that the proposed RBMPPG-based designs greatly lower area and power consumption; these reductions over earlier NB multiplier designs result in a minor latency gain (approximately 5 percent). The suggested RB multipliers may minimise the power-delay product by up to 59 percent when compared to current RB multipliers.

Exact computing units aren't usually required in applications that can tolerate mistake, including multimedia signals processing and data mining. They may be substituted with a similar item. Research into error-tolerant applications using approximation computation is on the increase. These applications rely heavily on adders and multipliers. In digital signal processing, approximate complete adders are suggested at the transistor level. Partial product accumulation in multipliers is handled by their suggested full-adder design The use of truncation in repaired multiplier designs is common to simplify the circuitry.

In order to compensate again for quantization error induced by the reduced portion, a variable corrective term is added Accumulation in partial products is critical in terms to power usage when using approximation methods in multipliers. If the least relevant bits of the inputs can be trimmed, then partial products may be formed in order to decrease hardware complexity. In the past, logic complexity reduction has been achieved by simply applying approximation full adder and compressors to the bits. Various probabilities are included into the partial products in this short. Systematic approximation is used to examine the likelihood statistics of the changing partial products. Approximation is suggested using half-adder, full-adder, & 4-2 compressors. The complexity of the arithmetic units is lowered, but effort is also made to ensure that the error value is kept low. Systemic approximation improves accuracy, while lower logic architecture of approximation arithmetic units reduces power and area consumption. Image processing applications benefit from improved peak signal-to-noise ratio (PSNR) values achieved by the suggested multipliers over previous designs. The mathematical distance between a proper output and an approximation output for an input signal may be characterised as the error distance (ED). Approximate adders are assessed, and a virtually invariant measure called normalised ED (NED) is suggested. For both current and proposed multiplier designs, the conventional error analysis, MRE, is discovered

Exact computing units aren't necessarily essential in applications like data mining and multimedia signal processing. They may be substituted with a similar item. Research into error-tolerant applications using approximation computation is on the increase. These applications rely heavily on adders and multipliers.

There are many different ways to express a binary number in the RBR system, which employs more bits than is necessary to represent one binary digit. In contrast to other binary numeral systems, such as two's complement, RBRs employ two bits for each digit instead of the normal one. As compared to ordinary binary representation systems, the RBR has a wide range of characteristics. RBRs are useful since they eliminate the need for a traditional carry in addition. The Rosberg makes bitwise logical operations slower when compared with untreated representation, but when the bit width is increased, arithmetic operations are quicker. Typically, each digit has a sign that is distinct from the sign of a number it represents. RBR is indeed a signed-digit form when the digits include signs.

An RBR is just a mechanism for notating location values. An RBR employs a pair or bits to represent a digit, which means that for every digit, an RBR needs two bits. Using a translation table, the value of a redundant digit may be determined. In this table, each possible pair or bits is represented by its numerical value.

The integer value of a particular representation is indeed a weighted summation of the digits, much as in traditional binary representation. Starting with the rightmost position, the weight increases by two for each subsequent position. Negative values are usually permitted in RBRs. If a redundantly recorded number is positively or negatively, there is no single message bit that identifies the difference between them. Integers may be represented in an RBR in a variety of ways.

Non-adjacent form & two's complement are prominent possibilities for the "canonical" form of an integer.

A. Modified Booth encoding

Two signed binary values in 2 's complement notation are multiplied using Booth's multiplication method. In 1950, while working on diffraction at Birkbeck University in Bloomsbury, London, Andrew Donald Booth came up with the algorithm. Algorithm for shifting was developed by Booth, who utilised desk computers that were more efficient in shifting than at adding. In the field of computer architecture, Booth's method is of interest.

An implicit bit underneath the most significant bit, y1 = 0, is examined using Booth's procedure for the N-bit multiplication Y in sign two's complement form. Bits yi and yi1 are examined for every bit yi, scale from zero to N - 1 for i. The product accumulation P remains unaffected if these two items are equivalent. The multiplicand times 2i is given to P when yi is zero or one, and the multiplyand times 2i is removed from P when yi is one or zero. The signed product is P's ultimate value.

However, the representations of a multiplicand & product are not defined and may be any number system that allows the addition and subtraction of numbers; as is the case with the multiplier. The sequence of the stages is left to the reader's imagination, as indicated before. This is usually done by shifting the P accumulator rightward in small stages, beginning at I = 0, and then working its way up from there, starting with the lowest N bits of P. Then, the multiplying by 2i is often substituted. In terms of these specifics, there are several modifications and optimizations available.

Strings of 1s inside the multiplier are typically characterised as being converted to high-order+1 and low-order-1 at the endpoints of the string using this process. In this case, there is no elevated +1 and the total consequence is that the appropriate value is interpreted as negative.

Step 1: Booth Encoder and Partial Product Generator stage (BEPPG stage): The partial product generator's efficiency is influenced by the booth encoder. The cost, performance, & energy usage of the RB summation tree or the multiplier everywhere are affected by the number of bits that may be avoided at this step. There are 16 CRBBE-4 slices used to regulate the multiplier in stage one. There is a five-fold increase in difficulty. Shifting and selecting the multiplicand bits results in 16 rows of RBPPG partial products.

Step 2: Redundant Binary Adder summing tree stage (RBA summing stage): A total of 128 bits are generated by the partial products. There are four Redundant Binary Adders (RBAs) that add these bits together: 1, 2, 3, and 4. Blocks of 128 bits each had been created using RBA.

Step 3: Redundant binary to NB conversion stage (RB-to- NB stage): The final aggregate result is converted to NB representation using an RB-NB converter. It is possible to do the conversion in groups of successive digits based on their arrival time due to the uneven delay pattern of the final Rbs result bits An RBA tree summation may be used to assess the carry production of the following set of digits because the summing results do not affect the carry generation.

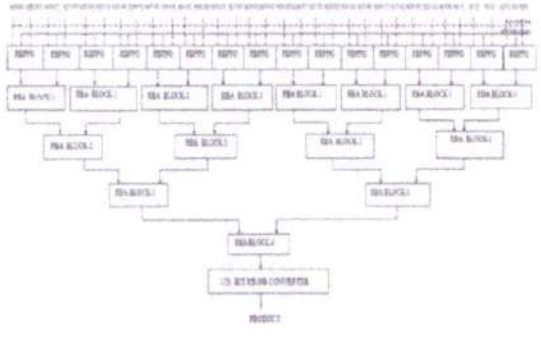


Fig 3.1: Block Diagram 8*8 bit High Performance Redundant Binary Multiplier

When two binary integers need to be multiplied, a binary multiplication is a digital electrical circuit, such as a computer. Binary adders are used to construct it.

A digital multiplier may be implemented using a number of computer arithmetic approaches. In most cases, a collection of partial products is computed, and then the partial products are added together. A base-2 (binary) numeral system has been adapted from the one taught to primary school pupils for lengthy multiplication on base-10 integers.

A student apprentice and then a research engineer, Arthur Alec Robin worked at English Electric Ltd. from 1947 until 1949. During this time, he also

worked on the early Marking 1 computer's hardware multiplier as part of his PhD studies at university of Manchester. [3] Most microcomputers did not get a multiply instruction till the late 1970s, which is why programmers devised a "multiply procedure" (typically implemented using loop unwinding) that continually shifted and accumulated incomplete results. Even though mainframe computers featured "multiply routines," they were just shifts and additions disguised as "multiply instructions."

Similarly, there was no multiply instruction in early microprocessors. There are at least two "improved" 8-bit microprocessors that have a multiply instruction, both of which were released in the 1980s, one of which was developed by Intel and was known as the MSC-51 family; the other was developed by Motorola and was known as the 6809; the advanced Atmel AVR 8-bit microcontroller can be found on ATMega, ATTiny & ATXMega microcontrollers.

To avoid reusing a single adder for each processing element one at a time, more transistors per board became accessible owing to larger-scale integration, making it feasible to place enough adders on one chip to total all the intermediate results at once.

The designers of early digital signal processors sacrificed a lot of chip space in addition to making the multiplication as fast as feasible; a solitary multiply–accumulate unit frequently utilised up most of the chip surface.

4. PROPOSED METHOD

Digital filters play a critical role in DSP. DSP's popularity is mostly due to its ability to perform at such a high level. Separation and restoration are the two primary functions of a filter. When the signal is tainted by interference, noise, or other signals, signal separation is required. Consider, for example, an EKG gadget for monitoring a baby's cardiac activity while still in the womb. The mother's breathing and pulse will likely distort the raw signal. These signals must be filtered out so that they may be evaluated separately. When a signal has been distorted in some manner, signal restoration is utilised. It's possible to improve an audio recording that was recorded with low standards by filtering it. Using a lens that is not properly focused or a camera that is shaken is another example. Analog or digital filters may be used to combat these issues. What's the best one? There is a wide dynamic range in the amplitude and frequency response of analogue filters. In contrast, the performance levels that may be obtained with digital filters are much better. Filters that use digital technology can outperform analogue ones by a factor of a thousand times. Filtering issues may now be tackled in a whole new way thanks to this discovery. There are a number of restrictions with analogue filters, such as a lack of precision in resistors and capacitor stability. Digital filters, in contrast, are so excellent that the filter's performance is often neglected. The focus now moves to the signal's inherent limits and theoretical difficulties surrounding its manipulation. In many digital signal processing (DSP) techniques, a variable is multiplied by a set of known constant coefficients. Multiplication is the most costly operation in DSP algorithms when compared to other frequent operations such as addition, subtraction, delay elements, etc. It's a trade-off between the quantity of silicon in the integrated circuit and how quickly the calculation can be done. Due to the fact that each operation must be performed within the same period of time, multiplication uses more logic resources than most other operations, even if the same number of logic resources are available. Any time you want to multiply two different variables, you'll need a generic multiplier. It is possible to use binary multiplication's features when multiplying by a known constant, such that we end up with a less costly logic circuit that is functionally similar to merely asserting the constant on a general multiplier. Because multiplication is costly, employing a cheaper solution for merely multiplication might result in considerable savings when looking at the full logic circuit. According on the application, multiplication may be the primary operation.

Throughout this thesis, we will suggest a number of algorithms that can be executed in software, but the solutions they provide allow for efficient hardware implementation of constant coefficient multiplication. Algorithms like this look for suitable hardware realisations based on a set of constant coefficients.

It is suggested that the proposed & existing approximation multipliers have their design and performance metrics thoroughly analysed and analysed. Image processing applications make use of the suggested multipliers, and the results are shown. Implementing multipliers involves three steps: creating partial products, creating a reduction tree from those partial products, and then combining those reduction tree sums and carry rows into a final result. The second phase is more demanding on the battery. The reduction tree step is when approximation is used in this short.

The second phase is more demanding on the battery. The reduction tree step is when approximation is used in this short. Using an 8-bit unsigned1 multiplier, the suggested approach for approximating multipliers is shown. Let _7m=0 and _7n=0 be two 8-bit unsigned input operands.

An example of an am,n partial product is mnin. As shown in Fig. , an AND operation here between bits of n and m produces the result. Signed multiplication, including Booth multipliers, may use the suggested approximation approach, but sign extension bits cannot.

Figure 4.1: Transformation of generated partial products into altered partial Products.

The probability of am,n is 1/4, statistically speaking. Signals for transmission and generation are built by combining am,n and am,m in columns using more than three partial products (1). Modifications to the PM,n and gm,n used to generate and send the signal have also been made. When bits am and an are exchanged for pm and gm, column 3 (with a weight of 23) becomes column 11 (with a weight of 211). See Figure 1 for an illustration of this partial product matrix. In Figure 1 we see both the initial partial product matrix and the transformed version. (1)

The chance of the modified partial product gm is 1/100, which is quite low in comparison to am,probability n's of 1/16. It is one-eighth as likely for pm,n to be one if it is an altered partial product, compared to the probability of gm,n. These factors are taken into account while approximating the modified partial product matrix.

In embedded system designs, power consumption and runtime management have always been at the forefront of difficulties. Image and video processing are common uses for digital signal processing methods, which are often implemented in embedded systems despite their computational demands. The time and power constraints of embedded systems may be satisfied with a specialised hardware implementation of the relevant algorithms. Multiple constants are multiplied by a variable in the centre of many of these methods (digital filtering, image processing, linear transforms, etc.). It is possible to significantly enhance the performance of the design in terms of characteristics like area and power consumption by focusing on optimising these multiplications. Multiple constant multiplication is the term for this kind of issue (MCM).

Two approaches to solving the MCM issue are the graph dependency algorithm and the common sub-expression elimination (CSE) methodology.

In this study, we examine the issue of quickly calculating a multiplier-less set of products tix, for I = 1,.., n, of a variable x with multiple known fixed-point constants ti. The term "multiple constant multiplication" describes this situation (MCM). Hardware implementations of, say, filters or transformations for digital signal processing, may greatly benefit from avoiding the use of expensive multipliers. However, in software implementations, it may also be useful to substitute constant adds and shifts for constant multiplications. For embedded processors, which may not even contain a multiplication unit, performance improvement may be necessary, since integer multipliers often have much lower throughput than adders. In the realm of computer mathematics, the MCM issue is perhaps one of the most basic challenges.

For the MCM issue, we provide a brand-new algorithm. As measured by the number of adds and subtractions required to arrive at a solution, our method consistently produces results that are superior than those obtained by any of the previously reported algorithms. The new algorithm also has a wider range of potential uses. We first provide a more thorough introduction to the subject at hand in order to more clearly clarify our contribution and place it in the context of prior work.

A. Single Constant Multiplication (SCM)

Binary shifts, additions, and subtractions may be used to break down the multiplication y = tx of a variable x by a given integer or fixed-point con-stant t. It is proved in [Cappello and Steiglitz 1984] that the issue of finding the decomposition with the fewest number of operations, known as the single constant multiplication (SCM) problem, is NP-complete. Because a fixed-point multiplication is similar to a multiplier by an integer followed by a right shift, we may assume without loss of generality that the constants are integers. Although similar, the SCM issue is not the same as the additive chain issue [Knuth 1969], which involves simply adds to multiply a constant by that value. The issue and the approaches to fixing it are both fundamentally changed when shifts are allowed.

Decomposing the division into adds and shifts is as simple as translating 1s in the binary of the constant t into shifts and adding up the shifted inputs. For t = 71, for instance, three additions are needed: 71x = 1000112x = x 6 + x 2 + x 1 + x. By converting zeroes to shifts and deducting from the nearest constant made up entirely of ones (i.e., of the type 2n 1), the

multiplication may be broken down into operations similar to addition and subtraction.

The formula for 71x is: 71x = 1000112x = (x 7 x) x 5 x 4 x Combining the best features of the two approaches leads to a solution that requires 2b + O(1) additions and subtractions, where b is the bitwidth of t, in the worst and average cases, respectively.

The canonical signed digit (CSD) form [Avizienis 1961] of a number permits negative digits 1, making it a superior digit-based technique for decomposing into addition and subtraction. When CSD is used, the above example may be simplified to require only two addition and subtraction operations instead of three.

x6 + x3 - x1 = 1001001CSDx = 1000112x

The average case cost is now 3b + O(1) with CSD, whereas the worst case cost is still 2b + O(1) [Wu and Hasan 1999].

Since the worst-case and average costs of CSD are unknown, it is not possible to determine whether or not it provides the best breakdown in terms of add/subtract operations. To determine the best decompositions for constants as large as 12 bits in size, [Dempster & Macleod 1994] developed a search method that performs a comprehensive search. The authors further demonstrated that shifts of no more than b + 1 are sufficient to provide excellent solutions for 12 bit constant. And now [Gustafsson et al. 2002] have expanded their work to constants as large as 19 bits, and once again, they get optimum answers independent of shift limits. As illustrated in Fig. 1, the optimum decomposition looks to have an asymptotic better cost than O(b), while the exponential worst case cost is still an ongoing research subject. The average number of additions and subtractions (y-axis) for 300 evenly distributed random constants with bitwidths ranging from 2 to 19 is shown to facilitate comparisons between the three decomposition techniques (x-axis).

Figure 1: 45-times multiplication with 3 adds and subtractions (CSD, top) and 2 adds and subtractions (bottom) (optimal, bottom). The nodes indicate addition and subtraction with output labels, while the edges represent transformations with scaling labels (a 2-power). If the scale is negative, then the operation being done is a subtraction.

that the CSD de-composition is inefficient and that the optimum decomposition employs a different graph topology. Intuitively, digit-based approaches like CSD provide unsatisfactory results since they only evaluate one kind of graph topology. On the other hand, while looking for optimum decompositions, the exhaustive search techniques described in [Dempster and Macleod 1994; Gustafsson et al. 2002] take into account all conceivable graph topologies.

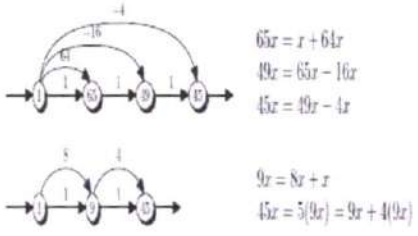
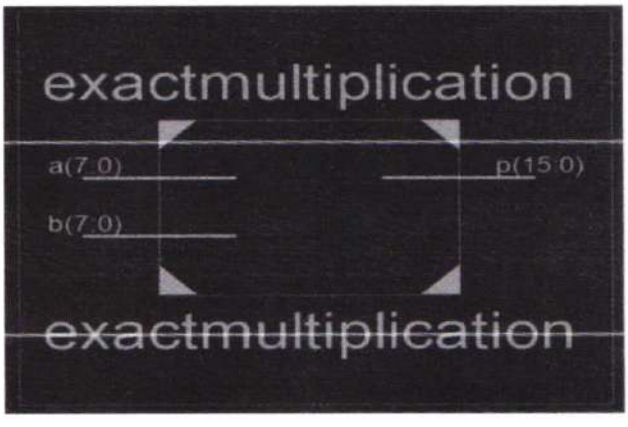


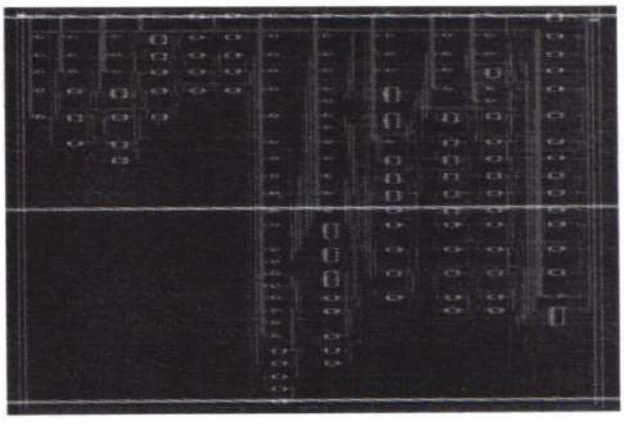
Figure 4.2: 45-times multiplication with 3 adds and subtractions (CSD, top) and 2 adds and subtractions (bottom) (optimal, bottom). The nodes indicate addition and subtraction with output labels, while the edges represent transformations with scaling labels (a 2-power). If the scale is negative, then the operation being done is a subtraction.

5. SIMULATION RESULTS

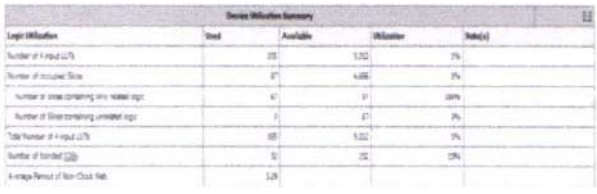
RTL



INTERNAL BLOCK DIAGRAM

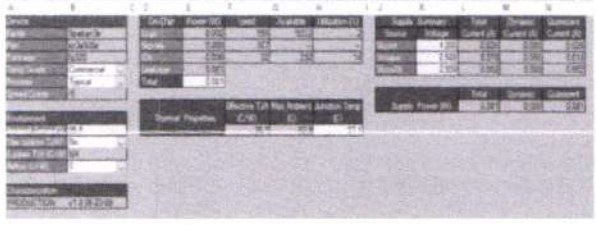


Area

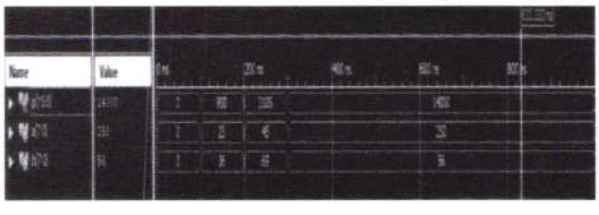


Delay

Power



Simulation



CONCLUSION

Using signals generated and propagated, this paper proposes efficient approximation multipliers. A basic OR gate is used to create changed partial products for approximation. Half-adder, full-adder, and 4-2 compressors are all recommended to minimise the leftover partial products in the final product. In Multiplier1, approximations are applied to all n bits, but in Multiplier2, they are applied just to the n 1 least significant bit. The space and power consumption of Multiplier1 and Multiplier2 are significantly reduced compared to exact designs. Both Multiplier1 and Multiplier2 save 87 and 58 percent, respectively, from accurate multipliers in APP compared to previous approximation solutions. When compared to previous approximation multiplier designs, they are proven to be more precise. Using the suggested multiplier designs, output quality may be maintained while substantial power and space are saved.

REFERENCES

[1] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digitalsignal processing using approximate adders," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137,Jan. 2013.

[2] E. J. King and E. E. Swartzlander, Jr., "Data-dependent truncationscheme for parallel multipliers," in Proc. 31st Asilomar Conf. Signals,Circuits Syst., Nov. 1998, pp. 1178–1182.

[3] K.-J. Cho, K.-C. Lee, J.-G. Chung, and K. K. Parhi, "Design low-error fixed-width modified booth multiplier," IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 522–531,May 2004.

[4] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspiredimprecise computational blocks for efficient VLSI implementation ofsoft-computing applications," IEEE Trans. Circuits Syst. I, Reg. Papers,vol. 57, no. 4, pp. 850–862, Apr. 2010.

[5] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design andanalysis of approximate compressors for multiplication," IEEE Trans.Comput., vol. 64, no. 4, pp. 984–994, Apr. 2015.

[6] S. Narayanamoorthy, H. A. Moghaddam, Z. Liu, T. Park, and N. S. Kim,"Energy-efficient approximate multiplication for digital signal processingand classification applications," IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst., vol. 23, no. 6, pp. 1180–1184, Jun. 2015.

[7] G. Zervakis, K. Tsoumanis, S. Xydis, D. Soudris, and K. Pekmestzi,"Design-efficient approximate multiplication circuits through partialproduct perforation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,vol. 24, no. 10, pp. 3105–3117, Oct. 2016.

[8] P. Kulkarni, P. Gupta, and M. D. Ercegovac, "Trading accuracy forpower in a multiplier architecture," J. Low Power Electron., vol. 7, no. 4,pp. 490–501, 2011.

[9] C.-H. Lin and C. Lin, "High accuracy approximate multiplier with errorcorrection," in Proc. IEEE 31st Int. Conf. Comput. Design, Sep. 2013,pp. 33–38.

[10] C. Liu, J. Han, and F. Lombardi, "A low-power, high-performanceapproximate multiplier with configurable partial error recovery," in Proc.Conf. Exhibit. (DATE), 2014, pp. 1–4.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Design Of Power And Area Efficient ECC Processor Using Reversible Technique

Charishmmaa G

MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: gunducherry4567@gmail.com

Dr.S. Kishore Reddy

Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.Email: kishorereddy416@gmail.com

V Guravaiah

Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: : guravaiahvemuri@gmail.com

***Abstract*— An exportable application-specific instruction-set elliptic curve cryptography processor based on redundant signed digit representation is proposed. The processor employs extensive pipelining. Furthermore, an efficient modular adder without comparison and a high through put modular divider, which results in a short data path form a ximiNISTreductionscheme.Thepropoprocessorerforms single point multiplication employing points in affine coordinates in 2.26 ms and runs at a maximum frequency of 160 MHz in Xilinx Virtex 5 (XC5VLX110T) field-programmable gate array.**

***Key Words*- field-programmable gate array, modular divider, digit representation.**

I. INTRODUCTION

Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum computing devices theoretically operate at ultrahigh speed and consume infinitesimally less power. Research done in this paper aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realise Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as a 4-bit Ripple-carry Adder, (8-bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates. The power and speed parameters for the circuits have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient. The designs presented in this paper were simulated using Xilinx 9.2 software.

Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information [1]. Basic reversible gates are employed to achieve the required functionality of a reversible circuit. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run backwards and while doing so, any intermediate design stage can be thoroughly examined.

A. Reversible Logic Gates

Boolean logic is said to be reversible if the set of inputs mapped have an equal number of outputs mapped i.e. they have one-to-one correspondence. This is realized employing reversible gates in the designs. Any circuit having only reversible gates is

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

capable of dissipating no power [2]. Goals of Reversible Logic: A. Quantum Cost: Quantum cost of a circuit is the measure of implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementary quantum operations needed to realize a gate.

There are many reversible gates such as Feynman, Toffoli, TSG, Fredkin, Peres, etc [3]. As the universal gates in boolean logic are Nand and Nor, for reversible logic, the universal gates are Feynman and Toffoli gates.

B. Feynman Gate

Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the input signal.

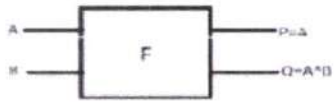


Figure 1 Feynman Gate

C. Fredkin Gate

It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2:

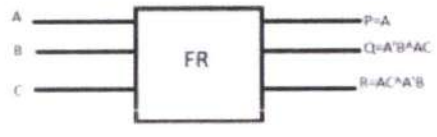


Figure 2 Fredkin Gate

D. Peres Gate

It is a basic reversible gate which has 3-inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R=(A.B)^C). The block diagram is as shown in fig. 3

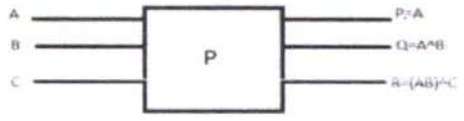


Figure 3 Peres Gate

E. Toffoli Gate

Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped to three outputs (P=A, Q=B, R= (A.B)^C). The block diagram of Toffoli gate is shown in fig. 4

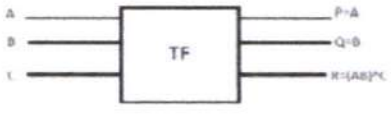


Figure 4 Toffoli Gate

F. TSG Gate

TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A, Q=A^B, R=A^B^D, S=(A^B)^D^AB^C). The block diagram of TSG Gate is shown in fig. 5

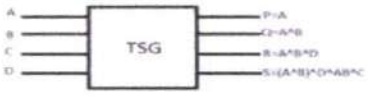


Figure 5 Tsg Gate

G. *Design Of Control Unit For Gcd Processor*

To illustrate the classical and reversible approaches to the Sequential Control Unit Design, reversible logic is employed for a special purpose processor that computes the GCD of two numbers. This GCD processor incorporates standard Euclid's Algorithm involving Subtract-Compare-Swap operation of two numbers. The basic principle is to subtract smaller of the two numbers repeatedly from the other number until we get the number that divides another [6]. A. Control Unit Control unit of GCD

processor generates the control signals to manipulate the operations in Data-path

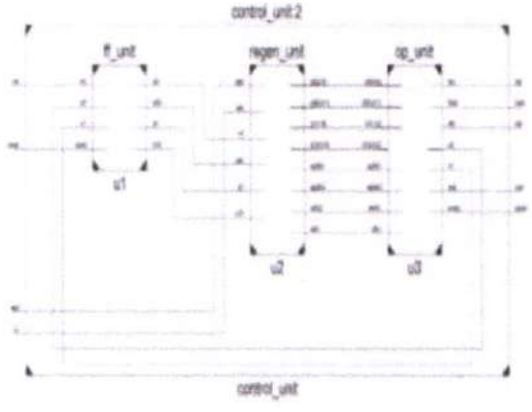


Figure 6 Block Diagram Of GCD Control Unit

H. Block Diagram Description

- *Flip-flop Module*

The control unit for GCD processor requires two Flipflops as binary state encoding is used for FSM. In this design reversible edge-triggered D Flip-flop is employed for state transitions [7]. Two D-latches are connected in Master-Slave mode to act as an edge-triggered D Flip-flop. Reversible D-latch is designed using Feynman and Fredkin gates [8]. RTL schematic of reversible D flip-flop obtained is shown in fig.

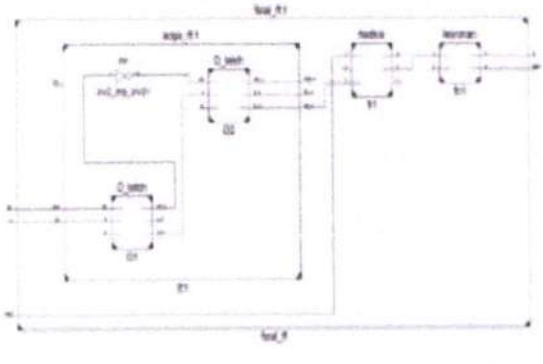


Figure 7 RTL schematic of Reversible D flip-flop

- *Regeneration Module*

To avoid multiple fan-out condition in the design, it is necessary to duplicate signals used for computation of output and next state. The duplication of input signals is achieved using Feynman gates.

- *Output Module*

The computation of the outputs and Next-state signals is done using reversible Fredkin gates. The functioning of output signals is driven by the algorithm. C. Final RTL schematic: The complete RTL schematic of GCD control unit is shown in fig.

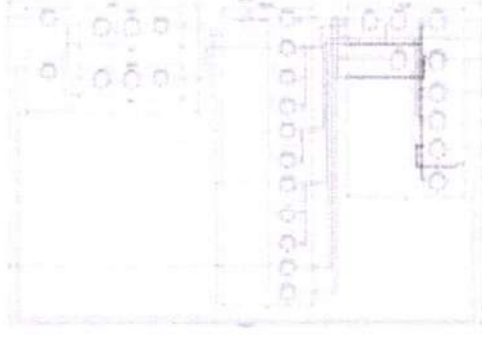


Figure 8 RTL Schematic Diagram Of Gcd Control Unit

I. *Speed and power analysis:*

Unit

Parameter (spartan3 xc3s50 family)	Irreversible GCD control unit	Reversible GCD control unit	Percentage improvement for reversible circuit
Speed(Max Clock freq)	434.33MHz	456.09MHz	5.01%
Power	25.02mW	24.19mW	3.31%

Table 1 Comparison of Reversible and Irreversible Control

J. *Applications*

Reversible logic design finds applications in various fields including Quantum computing, Nano-computing, optical computing, Quantum Computing Automata (QCA: study of mathematical objects called Abstract machines and the computational problems that can be solved using them), ultra- low power VLSI designing, Quantum dot cellular etc. The future of

computer chips is limited by Moore's law; hence an alternative is to build quantum chips. Our future research topic is designing a new reversible gate and to implement reversible logic into a complete Quantum processor capable of ultra-high speed and infinitesimally low power computing.

II. VLSI

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

A. ASIC

An Application-Specific Integrated Circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely to run a cell phone is an ASIC. Intermediate between ASICs and industry standard integrated circuits, like the 7400 or the 4000 series, are application specific standard products (ASSPs).

As feature sizes have shrunk and design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 gates to over 100 million. Modern ASICs often include entire 32-bit processors, memory blocks including ROM, RAM, EEPROM, Flash and other large building blocks. Such an ASIC is often termed a SoC (system-on-a-chip). Designers of digital ASICs use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

Field-programmable gate arrays (FPGA) are the modern-day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs and/or lower production volumes, FPGAs may be more cost effective than an ASIC design even in production.

B. Language– Verilog

In the semiconductor and electronic design industry, Verilog is a hardware description language(HDL) used to model electronic systems. Verilog *HDL*, not to be confused with VHDL (a competing language), is most commonly used in the design, verification, and implementation ofdigital logic chips at the register-transfer level of abstraction. It is also used in the verification ofanalog and mixed-signal circuits.

Hardware description languages such as Verilog differ from software programming languages because they include ways of describing the propagation of time and signal dependencies (sensitivity). There are two assignment operators, a blocking assignment (=), and a non-blocking (<=) assignment. The non-blocking assignment allows designers to describe a state-machine update without needing to declare and use temporary storage variables (in any general programming language we need to define some temporary storage spaces for the operands to be operated on subsequently; those are temporary storage variables). Since these concepts are part of Verilog's language semantics, designers could quickly write descriptions of large circuits in a relatively compact and concise form. At the time of Verilog's introduction (1984), Verilog represented a tremendous productivity improvement for circuit designers who were already using graphical schematic capturesoftware and specially-written software programs to document and simulate electronic circuits.

A Verilog design consists of a hierarchy of modules. Modules encapsulate *design hierarchy*, and communicate with other modules through a set of declared input, output, and bidirectional ports. Internally, a module can contain any combination of the following: net/variable declarations (wire, reg, integer, etc.), concurrent and sequential statement blocks, and instances of other modules (sub-hierarchies). Sequential statements are placed inside a begin/end block and executed in sequential order within the block. But the blocks themselves are executed concurrently, qualifying Verilog as a dataflow language.

A subset of statements in the Verilog language is synthesizable. Verilog modules that conform to a synthesizable coding style, known as RTL (register-transfer level), can be physically realized by synthesis software. Synthesis software algorithmically transforms the (abstract) Verilog source into a net list, a logically equivalent description consisting only of

elementary logic primitives (AND, OR, NOT, flip-flops, etc.) that are available in a specific FPGA or VLSI technology. Further manipulations to the net list ultimately lead to a circuit fabrication blueprint (such as a photo mask set for an ASIC or a bit stream file for an FPGA).

C. *System Verilog*

System Verilog is a superset of Verilog-2005, with many new features and capabilities to aid design verification and design modeling. As of 2009, the SystemVerilog and Verilog language standards were merged into System Verilog 2009 (IEEE Standard 1800-2009).

The advent of hardware verification languages such as Open Vera, and Verisity's e language encouraged the development of Super log by Co-Design Automation Inc. Co-Design Automation Inc was later purchased by Synopsys. The foundations of Super log and Vera were donated to Accellera, which later became the IEEE standard P1800-2005: System Verilog.

The most valuable benefit of SystemVerilog is that it allows the user to construct reliable, repeatable verification environments, in a consistent syntax, that can be used across multiple projects

Some of the typical features of an HVL that distinguish it from a Hardware Description Language such as Verilog or VHDL are

- Constrained-random stimulus generation
- Functional coverage
- Higher-level structures, especially Object Oriented Programming
- Multi-threading and interprocess communication
- Support for HDL types such as Verilog's 4-state values
- Tight integration with event-simulator for control of the design

There are many other useful features, but these allow you to create test benches at a higher level of abstraction than you are able to achieve with an HDL or a programming language such as C.

III. PROPOSED METHOD

Redundant signed digits Elliptic curve cryptography (ECC) is an asymmetric cryptographic system that provides an

equivalent security to the well-known Rivest, Shamir and Adleman system with much smaller key sizes. The basic operation in ECC is scalar point multiplication, where a point on the curve is multiplied by a scalar. A scalar point multiplication is performed by calculating series of point additions and point doublings. Using their geometrical properties, points are added or doubled through series of additions, subtractions, multiplications, and divisions of their respective coordinates. Point coordinates are the elements of finite fields closed under a prime or an irreducible polynomial. Various ECC processors have been proposed in the literature that either target binary fields, prime fields, or dual field operations. In prime field ECC processors, carry free arithmetic is necessary to avoid lengthy data paths caused by carry propagation. Redundant schemes, such as carry save arithmetic (CSA), redundant signed digits (RSDs), or residue number systems (RNSs), have been utilized in various designs. Carry logic or embedded digital signal processing (DSP) blocks within field programmable gate arrays (FPGAs) are also utilized in some designs to address the carry propagation problem. It is necessary to build an efficient addition data path since it is a fundamental operation employed in other modular arithmetic operations. Modular multiplication is an essential operation in ECC. Two main approaches may be employed. The first is known as interleaved modular multiplication using Montgomery's method. Montgomery multiplication is widely used in implementations where arbitrary curves are desired. Another approach is known as multiply-then-reduce and is used in elliptic curves built over finite fields of Messene primes. Messene primes are the special type of primes which allow for efficient modular reduction through series of additions and subtractions. In order to optimize the multiplication process, some ECC processors use the divide and conquer approach of Karatsuba–Ofman multiplications, where others use embedded multipliers and DSP blocks within FPGA fabrics.

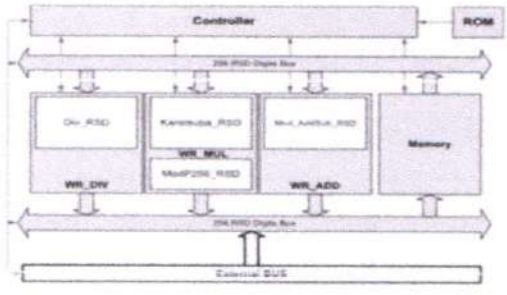


Figure 9 Overall Processor Architecture

External data enter the processor through the external bus to the 256 RSD digits input bus. Data are sent in binary format and a binary to RSD converter stuffs zeros in between the binary bits in order to create the RSD representation. Hence, 256-bits binary represented integers are converted to 512- bits RSD represented integers. To convert RSD digits to binary format, one needs to subtract the negative component from the positive component of the RSD digit.

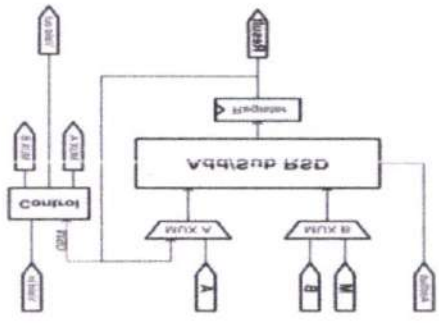


Figure 10 Modular Addition Subtraction Block Diagram

In order to overcome the problem of overflow introduced in the adder proposed in, a new adder is proposed based on the work proposed in. The proposed adder consists of two layers, where layer 1 generates the carry and the interim sum, and layer 2 generates the sum, as shown in Fig. 3. Table I shows the addition rules that are performed by layer 1 of the RSD adder, where RSD digits 0, +1, and −1 arerepresented by Z, P, andN, respectively. It works by assuring that layer 2 does not generate overflow through the use of previous digits in layer 1. The proposed adder is used as the main block in the modular addition component to take advantage of the reduced overflow feature. However, overflow is not an issue in both the multiplier and the divider when an RSD adder is used as an internal block. Hence, the reduced area is taken as an advantage in instantiating adders within the multiplier and the divider. The n-digits modular addition is performed by three levels of RSD addition. Level 1 performs the basic addition of the operands which produces n+1 digits as a result. If the most significant digit (MSD) of level 1 output has a value of 1/−1, then level 2 adds/subtracts the modulo P256 from the level 1 output correspondingly. The result of level 2 RSD addition has n+2 digits; however, only the n+1th digit may have a value of 1/−1. This assertion is backed up by the fact that the operation of level 2 is a reversed operation with the modulo P256, and most importantly, the proposed adder assures that no unnecessary overflow is produced. If the n+1th digit of level 2 result has a value 1 or −1, then level 3 is used to reduce the output to the n-digit range. Algorithm 3 shows the sequence of operations performed by the modular addition block. Notice that one modular addition is performed within one, two, or three clock cycles.

IV. CONCLUSION

a NIST 256 prime field ECC processor implementation in FPGA has been presented. An RSD as a carry free representation is utilized which resulted in short data paths and increased maximumfrequency. We introduced enhanced pipelining techniques within Karatsuba multiplier to achieve high throughput performance by a fully LUT-based FPGA implementation. An efficient binary GCD modular divider with three adders and shifting operations is introduced as well. Furthermore, an efficient modular addition/subtraction is introduced based on checking the LSD of the operands only. A control unit with add-on like architecture is proposed as a reconfigurability feature to support different point multiplication algorithms and coordinate systems. The implementation results of the proposed processor showed the shortest data path with a maximum frequency of 160 MHz, which is the fastest reported in the literature for ECC processors with fully LUT-based design. A single point multiplication is achieved by the processor within 2.26 ms, which is comparable with ECC processors that are based on embedded multipliers and DSP blocks within the FPGA. The main advantages of our processor include the exportability to other FPGA and ASIC technologies and expandability to support different coordinate systems and point multiplication algorithms.

REFERENCES

[1] Landauer, Rolf, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development ,vol.44, no.1.2, pp.261,269, Jan. 2000

doi: 10.1147/rd.441.0261

[2] Bennett, C.H., "Logical Reversibility of Computation," IBM Journal of Research and Development , vol.17, no.6, pp.525,532, Nov. 1973

doi: 10.1147/rd.176.0525

[3] B, Raghu Kanth; B, Murali Krishna; G, Phani Kumar; J, Poornima, "A Comparative Study of Reversible Logic Gates", InternationalJournal of VLSI & Signal Processing Applications, vol.2, Issue 1, Feb 2012, (51-55), ISSN 2231-3133 (Online).

[4] Morrison, M.; Ranganathan, N., "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," VLSI (ISVLSI), 2011 IEEE Computer Society AnnualSymposium on , vol., no., pp.126,131, 4-6 July 2011

doi: 10.1109/ISVLSI.2011.30.

[5] Nachtigal, M.; Thapliyal, H.; Ranganathan, N., "Design of a reversible single precision floating point multiplier based on operand decomposition," Nanotechnology (IEEE-NANO), 2010 10thIEEE Conference on , vol., no., pp.233,237, 17-20 Aug. 2010

doi: 10.1109/NANO.2010.5697746 (Nachtigal, Thapliyal, &Ranganathan, 2010)

[6] John P. Hayes, "Computer Architecture and Organization", McGraw-Hill, 1998. ISBN 10: 0070273553 / ISBN 13: 9780070273559

[7] Min-Lun Chuang; Chun-Yao Wang, "Synthesis of Reversible Sequential Elements," Design Automation Conference, 2007. ASPDAC'07. Asia and South Pacific , vol., no., pp.420,425, 23-26 Jan. 2007 doi: 10.1109/ASPDAC.2007.358022

[8] Yelekar, P.R.; Chiwande, S.S., "Design of sequential circuit using reversible logic," Advances in Engineering, Science andManagement (ICAESM), 2012 International Conference on , vol., no., pp.321,326, 30-31 March 2012.

OPEN ACCESS

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Design Of Power Efficient 12T Sram Using Adiabatic Technique For Charge Recovery Application

J Sudhakar
MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: prasannavemuganti@gmail.com

Dr.S. Kishore Reddy
Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

G Srinivas
Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

***Abstract*—As per the requirement of a design with minimal power has been a cardinal matter for the systems based on digital technology & greater performance like microprocessors, DSPs & various applications apart. The rise in market of mobile & electronic products powered by portable batteries needs chips which intake minimal power. SRAM incorporates around 60% of VLSI circuitries. Also memories are considered as the major flaw for decadence of power in a circuitry but no digital circuitry is accomplished by nor using memories. The absorption of power & SRAM's speed are major concern which followed several designs in accordance to the minimal absorption of power. The main concern of this document is on decadence of power while operation of Write is executed in 6-T CMOS SRAM. In this paper we mainly focus on decadence of power during short circuits also the fluctuating decadence of power which can also be termed as power which is dynamic. The tool of Tanner is deployed to evaluate the circuitry, the schema of cell of SRAM is formulated on S Edit & simulation of net list is furnished by making use of T Spice & also assessment of waveforms is done by W Edit.**

***Index Terms*—Minimal Power, SRAM, 130nm, 7T SRAM cell**

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

I. INTRODUCTION

A memory of semiconductor which is also ARAM is a bistate circuitry that is ployed to retain every single bit. The static & dynamic RAM which should be refreshed in a defined period of time. Reminisce is also explained by SRAM but it has volatile nature in a traditional way that means that data will not be retained if memory is turned off.

While commencing the particulars of design to formulation of layout of mask, the design of layout of an integral circuitry have various steps in processing which needed to be focused while execution. The steps invades design of schema at level of transistor, simulation of SPICE at circuitry as per designed proportions of W/L of a distinct transistor, formation of layout by making use of editor of layout, designing check rule, extraction in parasitic manner & exact evaluation & simulation. Such methodologies for processing can't be changed for operations which are free from error & same king of methodology is deployed for design of IC of SRAM of 1 kilobyte. The cell of SRAM is its main constituent which accumulates one bit of information ata time. The lines of bit that are common can be written & read over cell of SRAM. A standard tool for industry which is SPICE is ployed for purpose of simulation & assessment of cell of SRAM & eventually for complete design. The

circuitry which is already charged, the amplifier of sense & circuitry of read & write accomplish memory of one SRAM. The arrangement of matrix is done in form of rows & columns that enhance the addressing of memory in an easy wayof bits of memory & also furnish flexibility in design. As the working of array of cells of memory is evaluated, its imitation can be done for various times by making fewer variations in design in regulatory circuitry of I/O.

A. Plan of the chip

The diagram of whole chip is presented in the Figure1. There are 6 transistors that are arrangedin 8 blocks. Each cell of SRAM can retain 1 kilobyte of information. There are address lines 10in number like from A0-A9 which are ployed to label the locations. From these A0, A1,A2 are taken as lines for decoding of address of column, and A3-A9 are used for purpose to decode rows. Every single row has 8 cells of memory & formulates a single byte. So the lines of address points to every byte but not bit.

There are 8 columns & 128 rows in every block. So total of 49,152 transistors, 8 blocks* 128 rows * 8 columns * 6 transistors are there. The decoding of rows of every block is done by making use of decoder based on NOR as 7 *128. There are 1024 transistors for this circuitry. The decoder of outcomes is linked to every row of block. Parallel every single block is chosen bya decoder of column of 3*8. There are 32 transistors in total.

The amplifier of sense is ployed to sensation of information located in cell of memory. The blockof control for output & input information is comprised of circuitry for write & read in relation to circuits of driver. The data for 8 bits are from D0 to D7 is either written or read in parallel. The WE & RE are the lines of control that are furnished for chip. As by its name, RE is triggered before operation of read for the operations of reading. Just like to this, the WE signal is triggered for operations of write.

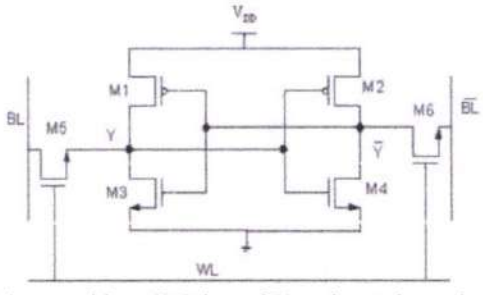
B. SRAM cell: schematic and working

The figure presents memory cell of SRAM for an individual bit. The latches which are static are deployed in cell of SRAM. The cell is formulated from a flip flop that is consisted ofinverters which are coupled as cross. The transistors of access which are 2 in number are ployed to evaluate the information retained in cell. The line for control that is WL, word line turns the transistors OFF or ON. In general, the WL is linked to outcome of circuitry of decoder of row. As the WL is equal to Vdd, BL is linked to cell of SRAM & its complementary, which allows both write & read operations. The function of read & write is executed by transistors of access.

C. Read operation:

The Y node is taken as the node for reference for cell of SRAM. As the node of Y at Vdd is high,value

Figure 1. Schema for cell of SRAM



1 is stored in cell & bar of Y node retains value 0. For the circumstances that have reverse voltage, cell retains value 0. It is taken that cell retains the value of 0. As the operation of read commences, the lines of BL & BL bar are charged to Vdd/2. As by the initiation of WL, the flowof current is by M5 & M6. Though current will flow through Vdd by M1 & M5 fluctuating the capacitance of line of bit, like Cbl. The present capacitance on line of BLbar like CBLbar dispenses the transistors by M6 & M4. The process formulates a difference in voltage among the node Y &Y bar which is detected by amplifier to sense value of 1. To parallel to this, value of 0 is sensed by amplifier.

D. *Write operation*:

Here the operation to write value 0 is presumed to store 1 value. By this, amplifiers of sensing & circuitries which are pre charged are disabled. This cell is chosen by triggering the associating signal of WL. In order to write value of 0 to cell, line of BL is taken down to the line of BLbar, which is enhanced to Vdd

by the circuitry of write. So the Ybar node is raised to Vdd/2 eventually Y node is brought down to the same. As the voltage gets over the level on 2 node feedback, action commences. The capacitances are formulated by M4, M6 & M3, M5 which are discharged & charged consequentially. Eventually the Y node is made stable at 1 value. As the capacitances of parasitic are furnished by transistors, which has value much lesser than capacitance of line of bits, and operation of write works fast than read.

E. Transistor sizing:

The proportion of W/L is chosen to furnish the gate with the ability of driving in all directions that is in relation to a standard inverter. From a standard design of inverter, W/L value is 1.5 or 2for a relative design, $(W/L)_p=(\mu_n/\mu_p)(W/L)_n$. The cell of SRAM is formulated in a way that whilefunctioning of operation of read, variations in Ybar & Y are minimal in order to avert cell to varyits state. In general, 2 inverters which are coupled together of cell of SRAM are formulated like Kp & Kn are countered. The threshold is put at Vdd/2 at the place of design. The extent of transistors of access is formulated around 3 times greater in width to the inverter's Kn. In orderto attain the optimal functioning of cell followed by proportion of W/L is selected for various transistors. Minimal proportion of 2 is needed for transistors of inverters of NMOS & 4 are mandatory for transistors of PMOS. Transistors of access are formulated by doubling the width or even more by furnishing a proportion of W/L greater than 4. Though the proportion of set don't get in accordance to the rule of design of Cadence Virtuoso editor of layout for technology of 0.18 micron. The minimal width for the transistor of NMOS is 0.6 micron for technology of 0.18 micron. So the proportion of W/L is 3.33. The proportion of PMOS will be 6.66. This leads to a width of 1.2 micron. On the formulation of simulation of SPICE are the assessments & outcomes, proportion of W/L is for transistor of access is retained at 9.99. This incorporates the width of gate of 1.8 micron.

II. EXISTING DESIGN DESCRIPTION

SRAM is basically a cell of memory in semiconductor. In accumulates a bit of data. it functions fast & absorbs minimal power in contrast to other cells of memory. As it is robust & has much more stability, more improvisations are being done in cells of SRAM. SRAM is considered as a cardinal element on a microprocessor chip. Formulating a cell of SRAM on a nanoscale is formulated as a task that is challengeable as margins in noise are deduced & sensitivity has been raised to fluctuations in voltage of threshold. The cell of 10T-SRAM has better performance than6T-SRAM on the factors of stability & reliability. Cell of 6T-SRAM is not much reliable when supply of power is less because margins in noise get degraded.

There are 6 transistors in a cell of 6T-SRAM. The figure presents a standard cell. The transistors for access are N2 & N3 and other 4 transistors, N1, N2, P1, P2 formulates 2 inverters. Information is latched by these 2 inverters. The information gets invaded to inverter of latching by transistor of access. The method to introduce information is termed as operation of writing & process to retrieve information is termed as process of reading. A row of cell of SRAM is chosen by WL. A column is chosen by BLbar & BL. A defined cell of SRAM is chosen as BL & WLare turned on. A 6T-SRAM & extra circuitry of reading can formulate cell of 10T-SRAM.

A cell of 10T-SRAM gets designed by making use of cadence virtuoso in technology of CMOS180mm & characteristics of the performance like delay, power, delay in power areassessed.

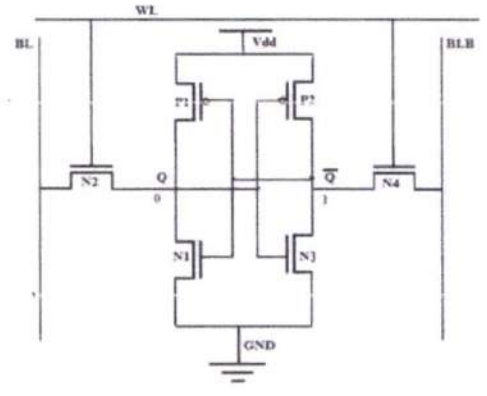


Figure 2. A 6T cell of SRAMs

A. *Design And Simulation Of A 10t Sram Cell*

Architecture of cell of 10T-SRAM is alike to cell of SRAM of 6T, but difference is that it has an extra circuitry for read. Figure 2 presents cell of SRAM designed for 10T. In cell of 10T-SRAM, 10 transistors are ployed. It comprise of traditional cells of 6T-SRAM & extra circuitry to read. The issue arises in traditional cells of 6T-SRAM is that there are chances to data to be lost while execution of operation of read. Flipping can occur at voltage at node at Q & Qbar because of inverters aligned back to back.

This problem can be eliminated by putting an additional circuitry. The operations of read in 6T and 10T-SRAM cells are similar. While in scenario of operation of reading, sharing of charges occurs in RBL

& no-transformed BL-BLB while operation of read is executed. As charge are shared, so lines of reading bit don't get discharged fully & remains at a mid level of voltage. Thus, working of cell becomes like an automated limiter for swinging lines of bit.

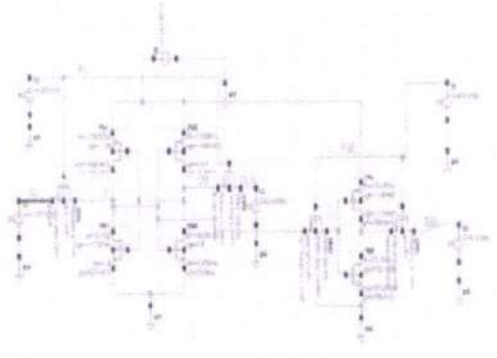


Figure 3. Design of a 10T SRAM cell

III. PROPOSED METHODOLOGY

A. *PROPOSED 7T SRAM CELL*

The given Figure 5 presents schema of cell of SRAM with less power & signals related to it wherever, CS, WL are required for making a selection for writing & data can be written from bit bar & bar.

As represented by Figure . cell with minimal power is comprised of an additional transistor & gate of that

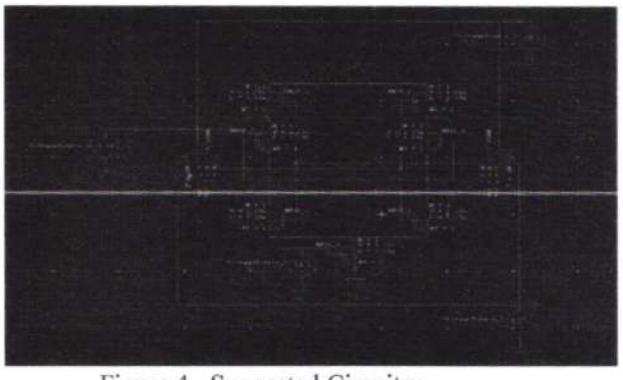


Figure 4. Suggested Circuitry

additional transistor will regulate operation of reading or writing information & also when operation of write is executed as the additional transistor cuts down the path in Vdd & ground & save circuitry from short circuit. We can make use of input, bit data or its complementary to execute operation of writing.

Functioning of cell of SRAM with less power & operation is explained in the modes of write & read as below:

A. *Read Mode*

Generally, cell of SRAM with less power in mode of reading is alike to traditional cell of SRAM. In this mode, value 1 is assigned to CS & an additional transistor will be activated on the basic operation of reading for cell of SRAM when a high voltage is provided to WLs, both the transistors of access will get activated & data needed will be out by the sensing amplifier.

B. *Write Mode*

In mode of writing, node of B should be assigned higher value which is achieved by putting CS as 0 invading signals of WL value of data is implemented to BL. There may be a possibility to write state of cell from 1 to 1. As bodes of B & CS, both are 0, no transition in state occurs. As conductance of N4 transistor has greater conductance than P2, the state of cell is flipped easily from 0 to 1 as node B is discharged by N4. As data can be written from 0 to the corresponding path as presented in figure .

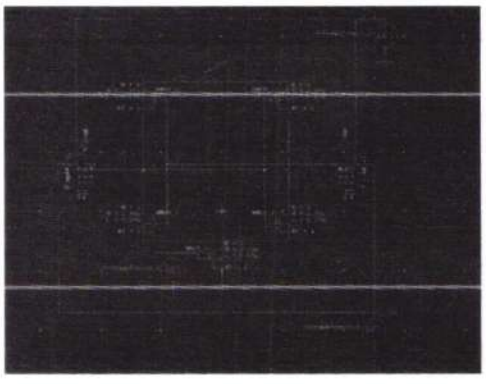


Figure 5. 6T traditional circuitry

IV. RESULTS

A. 6T Conventional Circuit

In this circuitry, we deploy transistors 6 in numbers. BL & WL is defined for write & readoperations. The absorption of power for figure 6.1 is 7.028097e-006 W & delay is 1.34ns.

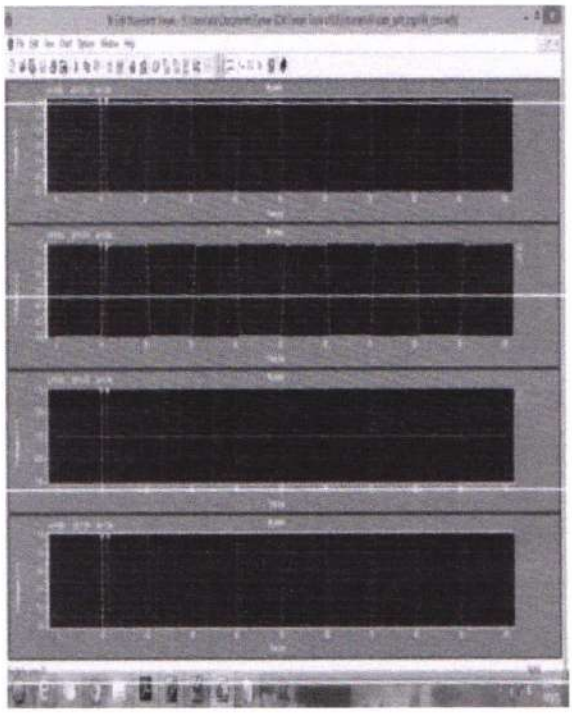


Figure 6. Waveform of 6T traditional circuitry

B. PROPOSED 7T SRAM DESIGN

The absorption of power for design of 7T SRAM is 4.184023e-006W with delay of 840.06ps.

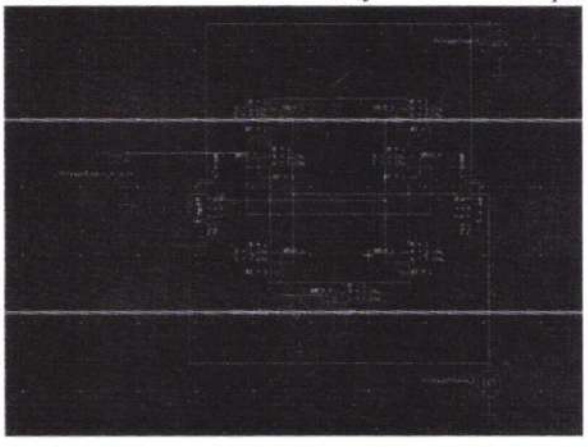


Figure 7. Suggested Circuitry

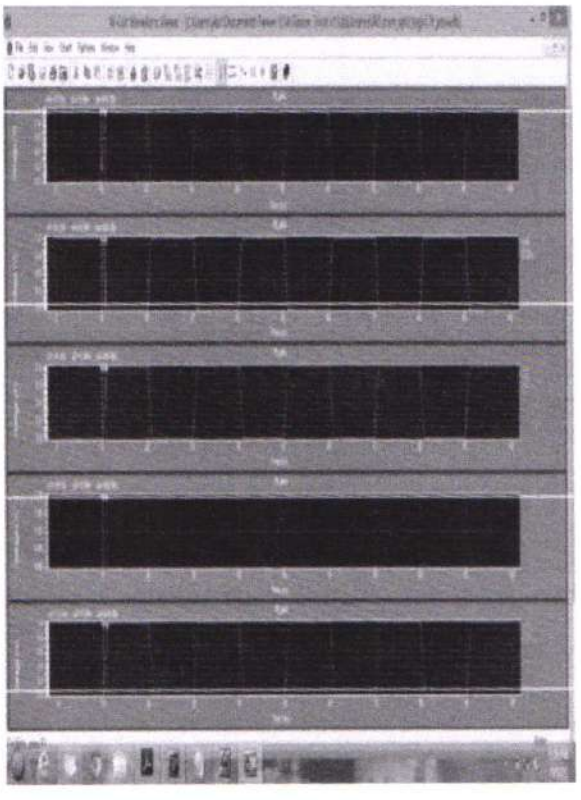


Figure 8. Outcome of waveform for suggested 7T SRAM

V. CONCLUSION

As observations from outcomes reveal that in cells of SRAAM with less power, aggregated power gets brought down by 43%. It presents that cell of memory will absorb low power in contrast to traditional cells of SRAM whose outcomes are imitated in this document. In a situation of power with short circuits, decadence of power gets down by 43% that is less in contrast to traditional cells of SRAM. Thus, the cell of SRAM which is newly formulatedabsorbs low power & it can be said that it is aware of power that can be accepted in the present market of VLSI. The delay is also improvised by 74%. So, cell of SRAM absorbs low power & executes operation faster than a standard cell of SRAM. In this cell lesser amount of power s taken in & so it saves around 43% of power in contrast to the present cells of SRAM. Thus these cells are deployed in electronics which are portable & are operated by battery & so will need lowcost sink of heat to furnish heat to surroundings.

VI. FUTURE SCOPE

This documentation can be elaborated for future work in order to bring down need of area that is around 16.72 % greater than the present cell of SRAM. A methodology can be searched to reduce this area & also there are no improvisations in cells of low power when operation to write1 is executed& so work can be extended for improvisation in delay whenever, operation of writing is executed.

REFERENCE

[1] Shunji Nakata, Hiroki Hanazono, Hiroshi Makino, Hiroki Morimura, Masayuki Miyama, and Yoshio Matsuda" Increase in Read Noise Margin of Single-Bit-Line SRAM Using Adiabatic Change of Word Line Voltage" IEEE Trans. Very Large Scale Integr. (VLSI) Syst. , vol. 22, no. 3, March 2014.

[2] Ho, K. Iniewski, S. Kasnavi, A. Ivanov, and S. Natarajan, "Ultra-low power 90 nm 6T SRAM cell for wireless sensor network application,"in Proc. IEEE Int. Symp. Circuits Syst. . , May 2006, pp. 4131–4134.

[3] S. R. Singh and K. Moez, "Ultra-low leakage 90 nm content addressable memory design for wireless sensor network applications," inProc. IEEE Int. Midwest Symp. Circuits Syst. , Aug. 2009, pp. 1191–1194.

[4] Frustaci, P. Corsonello, S. Perri, and G. Cocorullo, "Techniques for leakage energy reduction in deep sub micrometer cache memories, "IEEE Trans. Very Large Scale Integr. (VLSI) Syst. , vol. 14, no. 11,pp. 1238–1249, Nov. 2006.

[5] L. Chang, D. M. Fried, J. Hergenro ther,J. W. Sleight,R. H. Dennard. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams,K. W. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in Proc. Symp. VLSI Technol. , Jun. 2005,pp. 128–129.

[6] S. Ohbayashi, M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Imaoka, Y. Oda, M. Igarashi, M. Takeuchi, H. Kawashima, H. Makino, Y. Yamaguchi, K. Tsukamoto, M. Inuishi, K. Ishibashi, and H. Shinohara, "A 65-nm SoC embedded 6T-SRAM design for manufacturing with read and write cell stabilizing circuits," in Proc. Symp. VLSI Circuits, 2006,pp. 17–18.

[7] S. Nakata, H. Suzuki, H. Maki no, S. Mutoh, M. Miyama, and Y. Mat-suda, "Increasing static noise margin of single-bit-line SRAM by lowering bit-line voltage during reading," in Proc. IEEE Int. Midwest Symp. Circuits Syst. , Aug. 2011, pp. 1–4.

[8] Koushik K. Das and Richard B. Brown, "Ultra Low-Leakage Power Strategies for Sub-1 V VLSI: Novel Circuit Styles and Design Methodologies for Partially Depleted Silicon-On-Insulator (PD-SOI) CMOS Technology" International Conference on VLSI Design, July 2003.

[9] Blotti and R. Saletti, "Ultralow-power adiabatic circuit semi-custom design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. , vol. 12, no. 11, pp. 1248–1253, Nov. 2004.

[10] S. Kim and M. C. Papaefthymiou, "True single-phase adiabatic circuitry," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. , vol. 9, no. 1, pp. 52–63, Feb. 2001.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Efficient Design for Fixed-Width Adder-Tree

G santhoshini

MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India. Email: gundeboinasanthoshini@gmail.com

Dr. S. Kishore Reddy

Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India. Email: kishorereddy416@gmail.com

P V Raju

Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India. Email: vijnatharaju@gmail.com

Abstract - **There are many applications where multiplication is essential, including multimedia processing and artificial neural network (ANN. Multiplier is a substantial contribution to the energy usage, critical path latency, and resource usage in these applications. In FPGA-based designs, these impacts are more severe. ASIC-based systems, on the other hand, are the most up-to-date designs. Furthermore, the few Device designs that do exist are usually restricted to unsigned integers, requiring additional circuitry to provide signed operations. This work proposes an area-optimized, low-latency, and energy-efficient design for an accurate signed multiplier for FPGA-based solutions of applications that use signed integers. In order to speed up a multiplier, the best strategy is to limit the amount of incomplete products. With a modified Booth multiplier, adjustable arithmetic capacity and trade-offs in output accuracy are achieved.**

Keywords- ASCI, ANN, FPGA, Arithmetic capacity, Multiplier.

1.INTRODUCTION

Because of the increased complexity of VLSI design and application today, the manual approach of design is no longer a viable option. Automated design has become the standard practice. The present level of VLSI technology may be attributed to the rapid technological breakthroughs that have place over the course of the last two decades. Continuous growth in both the size and functionality of integrated circuits (ICs): The size of individual features has been steadily becoming smaller, which has resulted in a rise in both the speed and the gate device transistor density. Additionally, there has been a slow but steady improvement in the predictability of the behavior of circuits. Because of the aforementioned developments, there has been an explosion in the number of different approaches to VLSI design.

In the 1970s, when very large-scale integration (VLSI) was invented, complicated technologies for both semiconductors and communications were being developed. The VLSI technology was used in the construction of the microprocessor. Because of the dramatic increase in complexity brought about by the inclusion of hundreds of transistors in modern processors, this expression is not used nearly as often as it formerly was. This industry is becoming more obsessed with cramming more logic devices into ever-smaller spaces. At this time, very large scale integrated circuits can be built in very compact devices in a few of millimeters. VLSI circuits are used in a wide variety of modern electronic products including computers, automobiles, digital cameras, and mobile phones.

Interconnection variations: Because a huge number of transistors needed to be packed into a single chip in order to produce a functional design, it was necessary to approach this work with great attention to detail in terms of planning.

Using the technology that was available at the time, it was impossible to fit more than a few transistors on a single integrated circuit chip because of its vast size and the poor manufacturing yields that were available at the time. The design was simple because to the low number of links that were present. Because there are now a substantially greater number of transistors on a single chip than there were in the past, it is now significantly more difficult to create an efficient design.

Manuscript received Dec 10, 2022; Revised Dec 25, 2022; Accepted Dec 31, 2022

A. SSI Technology

Only very few transistors were used in the initial integrated circuits. Digital circuits with transistor counts in the tens offered a few logic gates, whereas early linear ICs like the Plessey SL201 or perhaps the Philips TAA320 contained as little as two transistors, a process known as "small-scale integration" (SSI). IBM engineer Rolf Landauer originally introduced the phrase "Large Scale Integration" while discussing the theoretical notion from which the names "SSI," "MSI," "VLSI," and "ULSI" were derived.

B. MSI Technology

Devices that had hundreds of transistor on each chip were known as "medium-scale integration" when they were first developed in the late Sixties (MSI).

C. Large Scale Integration

The same economic forces that resulted in "large-scale integration" (LSI) in the middle of the 1970s also resulted in thousands of transistors being packed onto one chip. Fewer than 4000 transistors were included in the first integrated circuits, which were manufactured in very limited numbers in the 1970s. In 1974, the first LSI circuits with more than 10,000 transistors were built for primary memory in computers and second-generation microprocessors. These circuits were developed in the United States.

As of 2009, very large-scale integration (VLSI), which was first created in the 1980s and is still being developed today, consists of more than a few billion transistors.

In 1986, consumers had the option of purchasing memory devices that included more than a million transistors. In 1989, a single computer chip included one million transistors; by 2005, that number had increased to one billion. Since 2007, when the first tens of billions of memory transistors were put into use, this pattern has been consistently maintained.

D. VLSI Design Flow

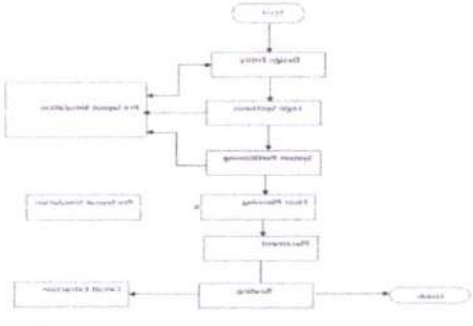


Fig 1.1: VLSI design flow

2. LITERATURE SURVEY

A. MULTIPLIERS

Multipliers are essential to the operation of a great number of extra applications in addition to digital signal processing. A substantial amount of focus and effort has been directed into the research and development of multipliers that are capable of achieving any of the following goals.

1. little power consumption,

2. lightning-fast speed

3.Due to the fact that they are so regular and take up such a little space, they are suitable for a wide variety of high-speed applications.

4. The use of very low power and very small integrated circuit technologies.

The "add and shift" method of multiplication is by far the most frequent approach. The performance of a parallel multiplier is significantly impacted when there is a greater number of sub-blocks that need to be added. The results of increasing parallelism and moving the partial products of intermediate sums that need to be added are a reduction in speed, an increase in the amount of silicon space required, and an increase in the amount of power required because of the increased number of connections caused by complex routing. On the other hand, multipliers that use the "serial-parallel" architecture sacrifice speed in order to save both space and power. It is possible that a parallel multiplier might be selected over a serial multiplier depending on the application in question. During this presentation, several multiplication algorithms and architectural frameworks will be discussed. We compare them using performance indicators such as the efficiency of their use of space, the amount of electricity they use, and the total amount of power they produce. It is possible to make the partial products by using AND gates (PP). You could find out how many partial products you have by multiplying an N-bit integer by an M-bit number. This might be done, for example, in Excel.

B. IMPLEMENTATION

An 8-bit accumulator is required to hold the result of the four bit multiplicand registers and the four bit multiplier registers that are included inside the MAC unit. The 8-bit result is stored in the product register, which can be seen in the picture. First, the multiplicand or even zero is shifted, and then, in the same manner as conventional binary multiplication, the result is added. This behavior is dependent on the multiplier bit. In order to do the same task, an adder with 8 bits would be required to be used. On the

other hand, this configuration adds a multiplicand with a value of 5 and shifts the contents of the product register to the right by one space. The processing of multiplier values sequentially while adding in parallel is referred to as a "serial-parallel multiplier," and it is described by this term. A parallel array multiplier is the second kind of multiplier that may be used.

Attempts were made to speed up the pace of output production, which led to the development of this form of multiplier. The data in the serial-parallel multiplier is processed one bit at a time, one clock cycle at a time, as was previously described. An input of N bits would need about N clock cycles before it could be converted into the final output. As soon as the multiplier's inputs are provided, the result may be found in the output. The majority of the responsibility for this problem may be placed on the calculation of the 1-bit terms using an AND array structure. Because the adders have to total these partial product terms column by column in order to obtain the result, the process takes a little bit more time than it would otherwise. The illustration that may be seen below depicts a parallel array multiplier that has N equal to 8 bits.

3. EXISTING SYSTEM

It is shown how to make array multipliers by making use of a two-operand adding circuit. This circuit combines the production of radix-2 partial products with addition operations. Modern FPGAs manufactured by Xilinx may make use of this circuit if the LUT design in question has six inputs. As a result of the lower LUT footprint that array multipliers have, it is possible for them to be deployed in the same logic fabric as equivalent Logic core IP multipliers. When pipelined to a substantial degree, these multipliers are often slower than the multipliers found in Logic core IP.

Why It takes up more space to produce the signed multiplier, so be sure you have enough. It will take much longer.

A. Architecture of A Booth Multiplier

After all of the partial products have been computed in parallel, this configuration adds the resultant partial products with the help of a rippling carry adder and a number of 4:2 compressors (RCA). The critical route time of the multiplier may be greatly cut down when concurrent manufacture of partial products is used. The length of the carry chain in a N x M multiplier is always N+4 bits for each bit row. It is possible that the length of the carry chain might be shortened to N+1 bits in order to enhance the critical path latency of the multiplier. The perfect application of our brand new multiplier's essential route delay is shown in the following picture. Each row of partial products needs two bits of multiplicand for the partial product expressions, with one bit reserved for the pp(x, 0) operation and the other two bits devoted to the pp operation (x, 1). Using a lookup table (LUT) with six inputs allows for the feasible execution of both of these partial product phrases. Each row of the partial product may have its own unique implementation of the pp(x, 2) function by making use of a second 6-input LUT. To calculate the appropriate input carry for each bit row, one may make use of a separate 6-input LUT that was given the designation "CG." The multiplier that we have presented is superior than multipliers that are already in use since it has a higher level of precision and accuracy.

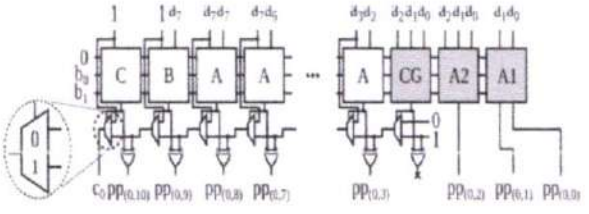


Fig.3.1: Architecture of Optimized version of multiplier

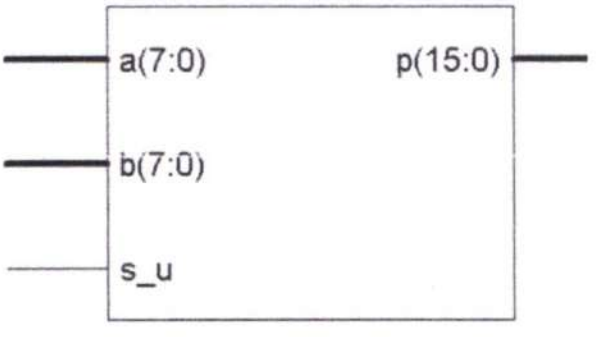


Fig.3.2: Block diagram of 8-bit booth multiplier

B. Partial Product Generation

In this work, signed-and-undated booth encoding multiplication is presented. Only signed values may be utilized with the modified booth encoding multiplier or the Baugh Wooley multiplier. When using the Braun array multiplier, unsigned values are the only kind of value that may be multiplied. When multiplying fixed numbers, every multiplier works in the same way. However, on current processors, we only need a single multiplier, regardless of whether the integers being multiplied are signed or unsigned. Efforts are being made to find a solution to this issue. The SUMBE multiplier may be found on the paper. One half of the partial product is represented by a revised Booth encoder, which acts

as a parallel representation of the circuit for the other half. As a direct result of the expanded operand signal bit, the SUMBE multiplier will produce one more partial product than usual. The Carry save adder (CSA) tree and the final carry look ahead will be used in order to quicken the acceleration of the multiplier (CLA). Using the MBE approach, this multiplier is able to handle signed and unsigned data equally well.

4. PROPOSED SYSTEM

It has previously been established that the multiplier is a very important component of microprocessors, microcontrollers, and graphics systems. The multiplier level that was provided by Booth Furnisha serves as the foundation for the algorithms that will be utilized in the future generation of multipliers. These multipliers will have improved performance and quicker speeds. By using a small-scale function, negatively oriented fragmented products are ejected from the system. When it comes to first-level booths, making use of a multiplier results in a more reliable coding standard. The topic of this study is partial products, both positive and negative, in their many forms. The key aims of this study are to develop more efficient processes and to cut down on the number of incomplete goods that are generated.

The effort that was made during the research project to solve the problem of negative partial products. Calculating the 2's complement requires bypassing the extra adding1 step and generating a lengthy carry chain for this assignment. Reduce the unfinished product to the smallest possible size using the design that was supplied. Modified By using Booth's technique n/2, which outperforms n/2+1 partial products, the number of partial products may be reduced, hence improving overall performance. Verilog HDL is used to create the actual workings of the proposed system. In order to put the suggested plan into action, it is necessary to be aware of the total amount of bits that will be multiplied. There are many different approaches of putting a design through its paces. Xilinx's own synthesis tool is what's utilized for the actual synthesis process.

The technique of multiplication for producing a more useful partial product is the subject of this study's investigation. There is no longer a need for additional adders to perform an addition of 1'b1 at each step when the suggested approach requires a 2's complement since it seeks to prevent the construction of extended carry chains. It is feasible to produce the radix 4 multiplier with the same hardware by employing the ways that have been described, while simultaneously lowering the number of partial products to n/2+1 from the original n. The approaches that have been discussed work very well with a dataset that is 16 bits by 16 bits, but they can also be used to larger datasets that have greater bit counts.

Utilizing high-radix Booth encoding is an alternate way that may be used to cut down on the amount of goods that are missing necessary components. On the other hand, hard multiples, which aren't powers of two and can't be created by shifting and/or complementation, are becoming more commonplace. Hard multiples are defined as multiples that can't be obtained in this way. Besli and Desmukh came to the conclusion that some difficult multiples may be computed by subtracting two simple power-of-two multiplies from each other. The problem of hard multiples may be solved by using a radix-4-Booth coding scheme (also known as RBBE-4) that does not make use of ECW. It is possible to eliminate the hard multiple issue as well as the additional ECW by using a radix-2 RB Booth encoder; however, this requires using twice as many rows of RBPP. Both the MBE represented by radix-2 RBPP and the MBE represented by radix-4 RBPP contain the same amount of rows. Although the output of the RBPP generator and the MBE generator can be the same, the RBPP generator has a more complicated circuit design and runs at a slower speed than the MBE generator.

By using the RBPP generator, we are able to create the same number of total product rows in a 2n-bit RB multiplier while simultaneously reducing the number of partial product rows produced. MBE-based RBMPPG-2 is the name of the new product generator that is based on modifying existing partial products (RBMPPG). In the RBMPPG-2 that was designed, the ECW from each row is moved to the row that comes after it in the next column. This extra ECW is coupled with the ECW of the very final partial product row, in addition to the two MSBs, which are comprised of the very first partial product row and its two LSBs. This further simplifies the reasoning (the second partial product row). As a direct result of this, an RBPP accumulation stage is maintained despite the fact that the number of RBPP rows was decreased from N=4 1 to N=4. When compared to typical designs, the multiplier architecture being proposed needs each operand to be at least 32 bits long. This results in considerable savings in both space and power when the operand word length is at least 32 bits. Even though there is a 5% increase in delay for words that are larger than 32 bits, the suggested designs are still optimal in terms of power-delay product (PDP) at these lengths.

The next paragraphs will offer an explanation of the structure of this paper. In the second part of this chapter, the radix-4Booth encoding is discussed. The structure of the traditional RBPP generator is likewise subjected to intensive research and

development. The RBMPPG diagram may be found in Section 3. The RBMPPG that has been suggested is presented in this section and is used by a variety of different word-length RB multipliers. New RB multipliers based on the proposed RBMPPG are evaluated and compared with prior best designs found in the technical literature for a variety of word lengths. These evaluations and comparisons are carried out.

A. Radix-4 Booth Encoding

In order to simplify the process of multiplying binary values with a two's complement, the Booth encoding has been devised. It was first implemented as either radix-4 Booth encoding or modified Booth encoding. Table 1 provides a concise overview of the MBE system. There are three sets of three multiplier bits that are next to one another. The two side bits overlap with the groups that are next to them, with the exception of the group that contains the first multiplier bit. According to Table 1, each group may be accessed by choosing the partial product that is shown there. In this context, the symbol 2A denotes the double of the multiplicand, which can be acquired by left-shifting the supplied value. By inverting each and every piece a The simple method is accomplished when a "1" (the correction bit) is added to the least significant bit (LSB). It has been suggested that correction bits might be used as a solution for problems with NB radix-4 Booth (NBBE-2) multipliers. On the other hand, this issue continues to have an impact on RB MBE multipliers.

B. RB Partial Product Generator

A RBPP is formed of two NB partial products since two bits are utilised to represent one RB digit. A two's complement representation may be used to indicate the integration of two N-bit NB partial products X and Y.

$$\begin{aligned} |X + Y &= X - \overline{Y} - 1 \\ &= \left(-x_N 2^N + \sum_{i=0}^{N-1} x_i 2^i\right) - \left(-\overline{y_N} 2^N + \sum_{i=0}^{N-1} \overline{y_i} 2^i\right) - 1 \\ &= -(x_N - \overline{y_N}) 2^N + \sum_{i=0}^{N-1} (x_i - \overline{y_i}) 2^i - 1 \\ &= (X, \overline{Y}) - 1. \end{aligned}$$

(1)

There is a convention throughout the remainder of the paper where Y inverses Y. As an RB number, the composite number may be deduced. When one of two NB partial products is inverted, and the LSB is multiplied by 1, the RBPP is formed. Each RB digit Xi is encoded by 2 bits as the pair '1; 0; 1'.

TABLE 2
RB Encoding Used in This Work [6]

X_i^+	X_i^-	RB digit (X_i)
0	0	0
0	1	$\bar{1}$
1	0	1
1	1	0

Table 1: RB Encoding

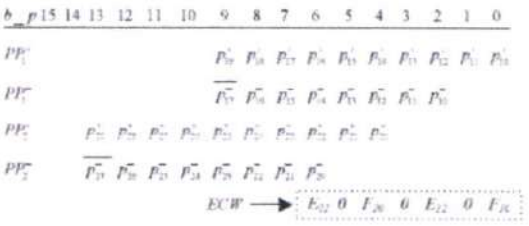


Fig.4.1: Conventional RBPP architecture for an 8-bit MBE multiplier

both negative and positive Xi effects. There are a variety of methods that may be used in order to encode an RB number. Table 2 presents a particular case of RB encoding; in this particular scenario, the RB digit is generated by using the Xi+ - Xi- procedure. The MBE and RB coding systems need the following terms to be changed as appropriate: When the modulated signal is multiplied by -1 or -2 during Booth encoding, the LSB of the second input must always be inverted and +1 must be added to it; consequently, -1 must be added to the LSB of the second input. This is because the LSB of the second input must always be inverted and +1 must be added to it. It's possible that a single ECW might handle both the radix-4 Booth recoding and the RB encoding. Figure 1 presents a common example of a partial product design for an 8-bit MBE multiplier that makes use of an encoder and a decoder. The produced bit position is denoted by the notation b p in this figure. A CRBBE-2 multiplier with N bits has four rows, with N equal to the number of RBPP rows plus one ECW row.

5. COMPARISION OF PARAMETERS

In the past, we have had an in-depth conversation on the modified Booth's algorithm as well as the Booth's multiplication algorithm. They were already working on their schematic implementation when they wrote down the techniques for estimating hardware parameters and modifying the bit width of input operands. This was done when they were working on their implementation. These parameters are compared by simulation in a virtex 4 xilinx area:

while conducting multiplication, the system output is optimized for area and has a maximum latency. These results are based on parameter comparisons and timing simulation results for the provided booth's multiplication. In order to compare the multipliers that are being offered here, it is necessary to compare the multipliers' parameters.

Table 5: Comparison of parameters

Booth Multiplier	Number of LUT's	Delay(ns)	Power(W)
Existing system 8-bit	144	23.333	0.081
Proposed system16-bit	297	5.116	0.065

Because of the new booth multiplier's slower working speed, it seems that the time delay will be reduced in this particular situation. However, the results that are produced by a 16-bit modified booth's multiplier are equivalent in area to the results that are produced by the booth's multiplier in terms of the complexity of the hardware and software.

6. SIMULATION AND SYNTHESIS REPORT

A. 8-Bit Unsigned Booth Multiplier

Fig.6.1: Simulation results of 8-bit unsigned Booth Multiplier

B.-Bit Signed Booth Multiplier

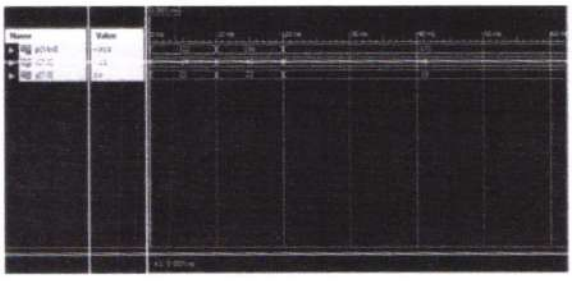


Fig.6.2: Simulation result of 8-bit signed Booth Multiplier

C. 16-Bit Unsigned Modified Booth Multiplier

Fig.6.3: Simulation result of 16-bit unsigned Modified BM

D.16-Bit Signed Modified Booth Multiplier

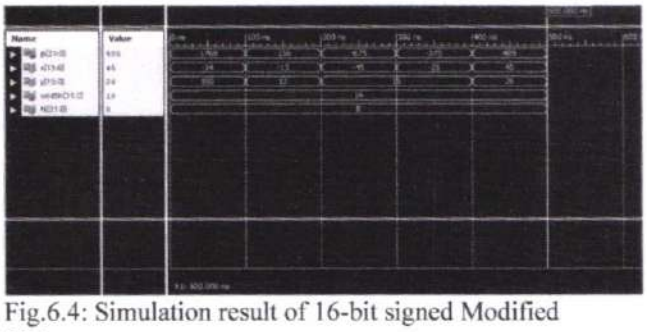
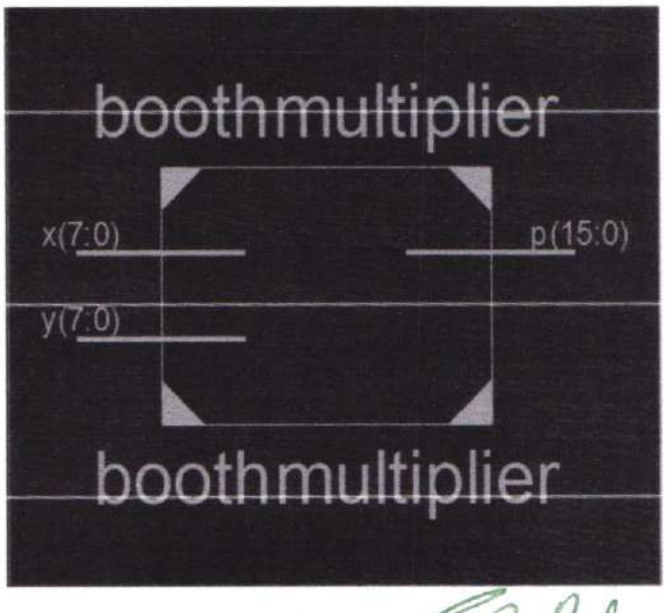


Fig.6.4: Simulation result of 16-bit signed Modified BM

E. RTL and Technology Schematics

8-Bit Booth Multiplier



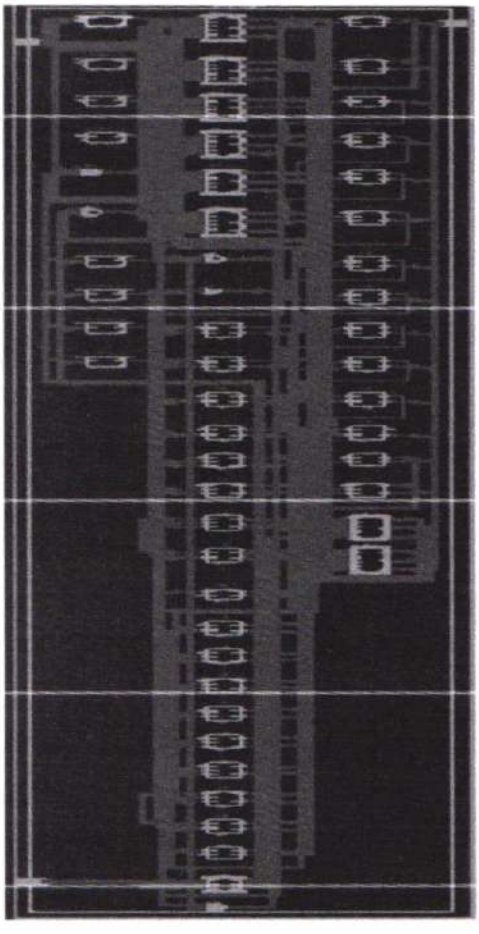


Fig.6.5: 8-bit RTL view of Booth Multiplier

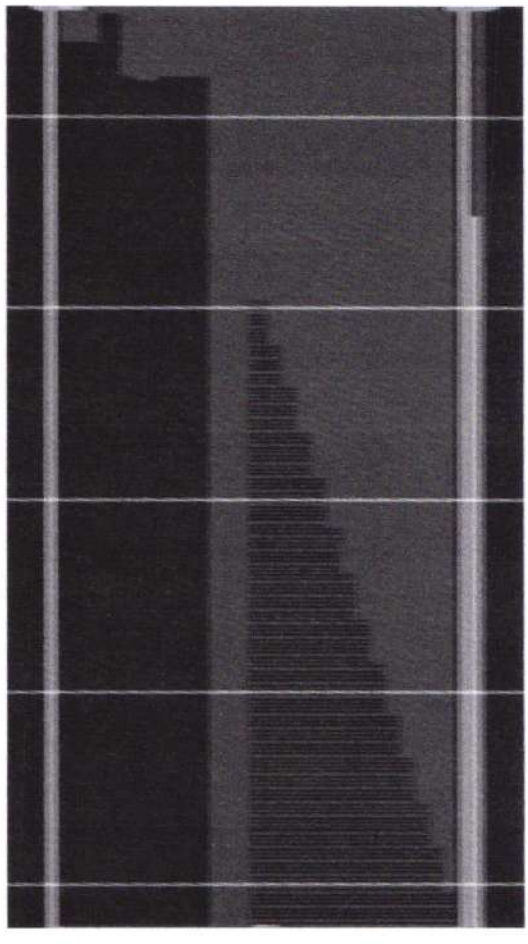
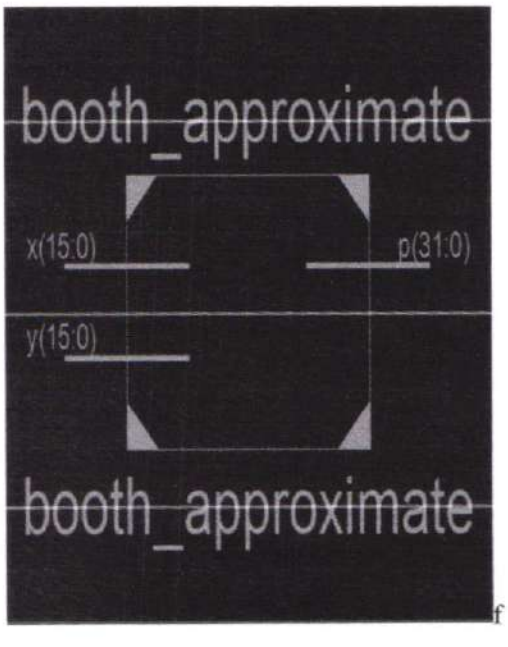


Fig.6.6: 16-bit RTL view of Modified Booth Multiplier

F. 16-Bit Modified booth multiplier



f

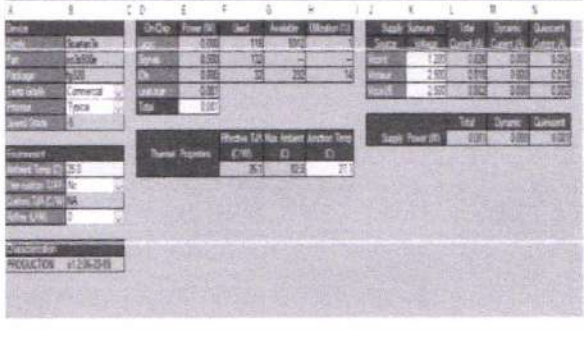


Fig.6.7: 8-bit Booth Multiplier Power Result

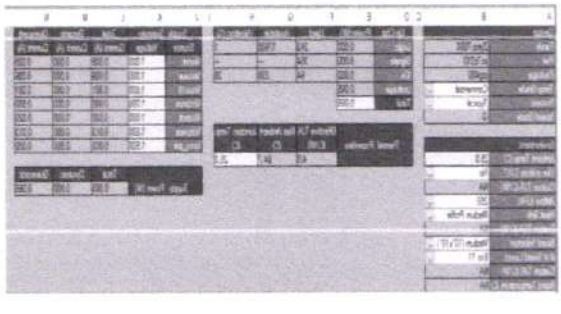


Fig.6.8: 16-bit Modified Booth Multiplier Power Result

CONCLUSION

The technique that has been presented produces power-delay products that are of a higher quality than those that are manufactured utilizing Booth multipliers. With the help of radix-4 Booth multipliers, we have seen how to bring the maximum height of the bits array down by one in this article. Because of this reduction, the pipelined multiplier's reduction tree may have access to an increased number of design alternatives in the case that a cell-based design is used. This method is one that may be used by conventional processors, digital signal chipmakers, mobile application processing units, and other arithmetic units. These are all examples of units that use Booth encoded data.

The incorporation of a comprehensive paradigm for approximate accumulator arithmetic computation makes it easier to develop approximation Booth multipliers and squares. In order to solve two key design challenges in the ECU (Electronic Control Unit) design, which is essential to the design of a AAAC (All Aluminum Alloy Conductor), it is necessary to have four theorems. These challenges are finding the best post-failure values and determining the best error compensation scheme. There is no need to be concerned about the ECU logic simplification that has been included since it will further lower the amount of energy used and take up less space.

REFERENCES

[1] 7 Series DSP48E1 Slice, document UG479, Xilinx, San Jose, CA, 321USA, 2018. 322

[2] S. Ullah et al., "Area-optimized low-latency approximate multipliers for 323FPGA-based hardware accelerators," in Proc. ACM/ESDA/IEEE Design 324Autom. Conf. (DAC), 2018, pp. 1–6. 325

[3] I. Kuon and J. Rose, "Measuring the gap between FPGAs and ASICs," 326IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 26, no. 2, 327pp. 203–215, Feb. 2007. 328

[4] LogiCORE IP Multiplier v12.0, document PG108, Xilinx, San Jose, 329CA, USA, 2015. 330

[5] A. D. Booth, "A signed binary multiplication technique," Quart. J. 331Mech. Appl. Math., vol. 4, no. 2, pp. 236–240, 1951. 332

[6] C. R. Baugh and B. A. Wooley, "A two's complement parallel array 333multiplication algorithm," IEEE Trans. Comput., vol. C-22, no. 12, 334pp. 1045–1047, Dec. 1973. 335

[7] M. Kumm, S. Abbas, and P. Zipf, "An efficient softcore multiplier 336architecture for Xilinx FPGAs," in Proc. IEEE Symp. Comput. Arithmetic 337(ARITH), 2015, pp. 18–25. 338

[8] E. G. Walters, "Array multipliers for high throughput in Xilinx FPGAs 339with 6-input LUTs," Computers, vol. 5, no. 4, p. 20, 2016. 340

[9] H. Parandeh-Afshar and P. Ienne, "Measuring and reducing the 341performance gap between embedded and soft multipliers on FPGAs," in 342Proc. Int. Conf. Field Program. Logic Appl. (FPL), 2011, pp. 225–231. 343

[10] 7 Series FPGAs Configurable Logic Block, document UG474, Xilinx, 344San Jose, CA, USA, 2016. 345

[11] H. Parandeh-Afshar, P. Brisk, and P. Ienne, "Exploiting fast carry-chains 346of FPGAs for designing compressor trees," in Proc. Int. Conf. Field 347Program. Logic Appl. (FPL), 2009, pp. 242–249. 348

ISSN: 0974-5823 Vol. 7 No. 5 May, 2022

International Journal of Mechanical Engineering

EXPERIMENTATION AND ANALYSIS OF NATURAL FIBER REINFORCED POLYMER MATRIX COMPOSITE

Dr Ramesh Babu Yeluri
Associate Professor, Department of Mechanical Engineering
Avanthi Institute of Engineering and Technology, Hyderabad, Telangana, India-501512,
yrameshbabu321@gmail.com

Kolla Sumanth
Assistant Professor, MED, Avanthi Institute of Engineering and Technology,
Hyderabad, Telangana, India-501512

Mallikanti Venkateswarlu
Assistant Professor, MED,
Avanthi Institute of Engineering and Technology, Hyderabad, Telangana, India-501512

G Vinod Kumar
Assistant Professor, MED,
Avanthi Institute of Engineering and Technology, Hyderabad, Telangana, India-501512

Abstract - The high cost of synthetic fibers such as glass, carbon, etc, results in high cost of production and products derived from these materials which has necessitated alternative means of materials development. This has also informed the utilization of locally available bamboo fiber for composite materials development. Natural fiber has emerged as a renewable and cheaper substitute to synthetic materials such as glass, carbon and afraid, which are used as reinforcements. In this work, the objective was to develop, investigate and analyze the mechanical properties of a composite material using bamboo fiber and jute fiber sandwich type composite. The long bamboo fiber was extracted using chemical digestion and maceration methods. The fabrication of the composite was carried out using epoxy resin as the matrix and the bamboo fiber and jute fiber as reinforcement. Tests were carried out to determine the mechanical properties such as tensile, hardness strengths. The results were studied and compared with the composite of bamboo fiber with epoxy resin and it process that the material developed can be used in structural applications with strong dependence on its mechanical properties

Index Terms - composites, types of fiber, reinforcement materials, and mechanical properties.

INTRODUCTION

Composites are combination of two materials in which one of the material act as Reinforcement and the other as matrix. The reinforcement may be in the form of fiber woven cloth or in particulate form which may be embedded in the other material called matrix. The reinforcement material may be of ceramic, polymer or metallic and matrix material may be of polymer, metallic or ceramic in nature. Composites are used, as the mechanical properties of the composite as a whole is superior to that of the individual components.

Composites are able to meet diverse design requirements with appreciable weight saving. The high strength to weight ratio is an important aspect to be considered making these materials for automotive applications,

Epoxy resin is one of the excellent thermosetting polymer resins. The cost-to- performance ratio of epoxy resin is outstanding. Epoxy resins possess characteristics such as high strength low creep, good adhesion to

most of the substrate materials, low shrinkage during curing and low viscosity. Due to these reasons epoxy resins are significantly used as matrix material in many applications such as aerospace, structural applications, ship building, and automobile industries and so on. The tensile strength and the tensile modulus of Glass fiber/Epoxy composite increases in fiber loading and the addition of Nano-clay particles to the Glass fiber/ Epoxy composite increase the tensile strength and the tensile.

- **Types of Composites**: The 3 Basic Types of Composites are generally identified as Particle-Reinforced (Aggregates), Fiber-Reinforced (Continuous Fiber or Chopped Fiber), Natural Composites (Examples: Wood and Bone).

NANO COMPOSITE

Composite is a multiphase solid material where one of the phases has one, two or three dimensions of less than 100 nanometers (nm), or structures having nano-scale repeat distances between the different phases that make up the material. In the broadest sense this definition can include porous media, colloids, gels and copolymers, but is more usually taken to mean the solid combination of a bulk matrix and nano-dimensional phase(s) differing in properties due to dissimilarities in structure and chemistry. The mechanical, electrical, thermal, optical, electrochemical, catalytic properties of the nano-composite will differ markedly from that of the component materials. Size limits for these effects have been proposed, <5 nm for catalytic activity, <20 nm for making a hard magnetic material soft, <50 nm for refractive index changes, and <100 nm for achieving super para magnetism, mechanical strengthening or restricting matrix dislocation movement.

Nano composites are found in nature, for example in the structure of the abalone shell and bone. The use of nano particle-rich materials long predates the understanding of the physical and chemical nature of these materials. In mechanical terms, nano composites differ from conventional composite materials due to the exceptionally high surface to volume ratio of the reinforcing phase and/or its exceptionally high aspect ratio. The reinforcing material can be made up of particles (e.g. minerals), sheets (e.g. exfoliated clay stacks) or fibers (e.g. carbon nano-tubes or electro spun fibers).

The area of the interface between the matrix and reinforcement phase(s) is typically an order of magnitude greater than for conventional composite materials. The matrix material properties are significantly affected in the vicinity of there inforcement.

Other kinds of Nano particulates may result in enhanced optical properties, dielectric properties, heat resistance or mechanical properties such as stiffness, strength and resistance to wear and damage. In general, the nano reinforcement is dispersed into the matrix during processing. The percentage by weight (called mass fraction) of the Nano particulates introduced can remain very low (on the order of 0.5% to 5%) due to the low filler percolation threshold, especially for the most commonly used non-spherical, high aspect ratio fillers (e.g. nanometer-thin platelets, such as clays, or nanometer-diameter cylinders, such as carbon nano-tubes). The orientation and arrangement of asymmetric nano-particles, thermal property mismatch at the interface, interface density per unit volume of nano composite, and polydispersity of nano particles significantly affect the effective thermal conductivity of nano composites.

Nano composites are further classified into 3-types are Ceramic-matrix nano composites, Metal-matrix nano composites, Polymer-matrix nano composites.

- **PMC manufacturing processes:** They are lot of well-established manufacturing processes which are available to produce components with polymer composite materials few of them are Wet lay-up/hand lay-up method, Spray up Molding, Resin Transfer Molding, Filament winding Method

In the present work epoxy resin is chosen as matrix, E-glass fiber, Wollastonite / Silicon is chosen as reinforcement. Room temperature cured Epoxy System filled with glass Fiber and Wollastonite / Silicon were synthesized by mechanical shear mixer, and then the mixture of epoxy and Wollastonite / Silicon is blended.

Mechanical properties like Flexural strength, Tensile strength of the micro hybrid composite are studied by UTM (Universal Testing Machine). The images of the fractured structures are taken using Scanning

Electron Microscope. The observation established good miscibility of Epoxy and Homogenous dispersion of silicon / Wollastonite in the matrix.

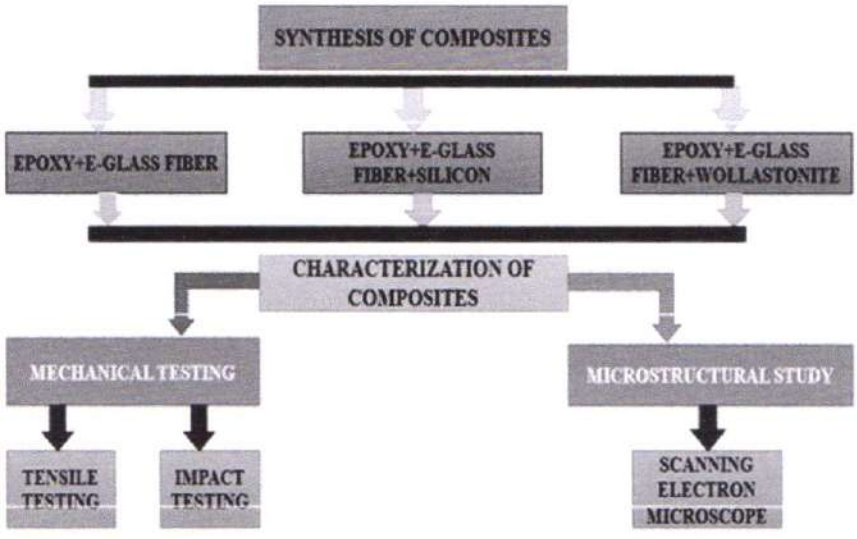


Figure 1

OVERVIEW OF THE WORK

PREPARATION OF COMPOSITES

4.1 PROCEDURE FOR PREPARING TEST SAMPLES:

The present problem has been formulated to implement different test to the structures so as to establish facts related to the flexural behavior of glass epoxy. the experimental work consist of preparing test samples, the samples are prepared made of e-glass woven fabric epoxy laminates made of various orientation sequences have been prepared as per ASTMD

- **Design and Fabrication of Metallic Mould:** The pressure to be applied to consolidate laminate after impregnating resign should be applied by compression as the required specimen are to be manufactured as per ASTM specifications. The mould is made of MS material.
- **Pressure plate:** Pressure plate is made of the MS plate with surface finish ensuring perfect flatness 5mm thickness is maintain to meet the requirement to withstand the compressive force. This particular method of making laminate to ensure that the thickness of the laminates will be uniform with constant volume fraction of matrix and reinforcement.

In the present work composite templates are prepared as per the required dimensions. According to the required dimensions the glass fiber mat has been cut, by making use of different mechanical equipment and measuring equipment's. And then excess material is removed on the surface of the mould and poly vinyl alcohol viscous liquid is applied on the surface of the mould uniformly and left for drying about 15 minutes. This liquid creates an invisible film which works as impervious layer prevents sticking to the mould surface.

Spacers are placed on the borders of the mould to get exact thickness of the laminate and uniform distribution of resin. Each layer of the fiber is kept in the mould and applying resin on to it, then the rolling is done by roller to distribute the resin evenly on to the layers. After completion of distribution of resin on to the layers amylar film is placed to get the surface finish, while after a pressure plate is placed onthe layers by that the uniform load is distributed and exact thickness occurs by the spacers. To get the required laminate it has been taken 24 hours while after remove the pressure plate and mylar film and removes the laminate from the mould. The same processes have done for various different layers of

sandwich composite laminates. And finally cut the laminates by using cutter machine in to a required ASTM standard dimension.

The excess sides of the laminate which are formed because of pressure plate during the fabrication is chopped out and according to the required dimension i.e. ASTM638 standards, the sample pieces are taken out with the help of wood cutting machine as shown below.

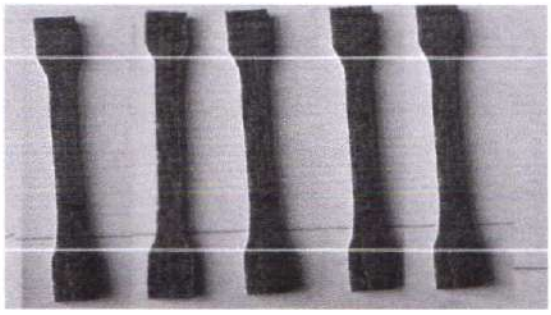


Figure 2

WORK CUTTING THE LAMINATE IN TO A REQUIRED DIMENSION

DATA EXPERIMENTATION AND ANALYSIS

There are two stages in the process of familiarizing with plastics. The first is rather general and involves an introduction to the unique molecular structures of polymers, their physical and transitions which have a marked influence on their behaviour. The study of specific properties of plastics reveals their application. Besides the relative ease of their moulding and fabrication, many plastics offer range of important advantages in terms of high strength/weight ratio, toughness, corrosion-resistance, wear-resistance, frictional co-efficient, tensile, flexural, compression, impact strength and chemical resistance. Due to these qualities, plastics are acceptable as materials for wide variety of engineering applications. It is important therefore, that an engineer be aware of the performance characteristics and significant properties of plastics. Plastics are generally dealt with, in respect of broad categories of properties, namely, mechanical, thermal and chemical. An important facet of materials development and proper materials selection is testing and standardization. This chapter represents schematically (in simplified form) a number of standard test methods for plastics, highlighting the principles of the mechanical tests and the properties measured with them. List of salient features of testing has been stated below.

- To assess numerically the fundamental mechanical properties of ductility, malleability, resilience, stress-strain and visco elastic behaviour.
- To determine data (i.e. force deformation or stress values) to draw up sets of specifications, upon which the engineer can depend for his design.
- To determine the surface or subsurface defects in raw materials or processed parts.
- To check chemical composition.
- To determine the stability of a materials for particular applications.

The most common testing machine used in tensile testing is the UTM. This type of machine has two crossheads; one is adjusted for the length of the specimen and the other is driven to apply tension to the test specimen.

The machine must have the proper capabilities for the test specimen being tested. There are three main parameters: force capacity, speed, and precision and accuracy. Force capacity refers to the fact that the machine must be able to generate enough force to fracture the specimen. The machine must be able to apply the force quickly or slowly enough to properly mimic the actual application. Finally, the machine must be able to accurately and precisely measure the gage length and forces applied; for instance, a large machine

that is designed to measure long elongations may not work with a brittle material that experiences short elongations prior to fracturing.

Alignment of the test specimen in the testing machine is critical, because if the specimen is misaligned, either at an angle or offset to one side, the machine will exert bending force on the specimen. This is especially bad for brittle materials, because it will dramatically skew the results. This situation can be minimized by using spherical seats between the grips and the test machine. A misalignment is indicated when running the test if the initial portion of the stress-strain curve is curved and not linear.

The strain measurements are most commonly measured with an extensometer, but gauges are also frequently used on small test specimen or when Poisson's is being measured. Newer test machines have digital time, force, and elongation measurement systems consisting of electronic sensors connected to a data collection device (often a computer) and software to manipulate and output the data.

The test process involves placing the test specimen in the testing machine and applying tension to it until it fracture. During the application of tension, the elongation of the gauge section is recorded against the applied force. The data is manipulated so that it is not specific to the geometry of the test sample.

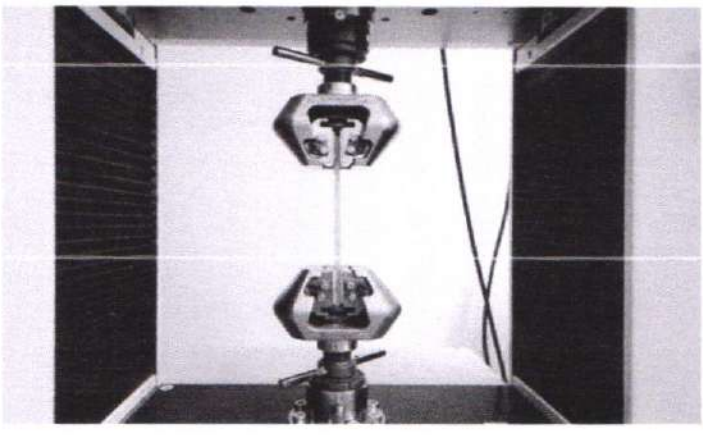


Figure 3

LAMINATE IS FIXED BETWEEN JAWS FOR TENSILE LOADING

RESULTS AND DISCUSSIONS

The Tensile test (UTM), hardness test has been done and the results obtained were furnished in the form of Data Sheets and the output screen shots and the results were published by performing these testing in the KELVIN LAB Hyderabad are as follows:

TABLE I

TENSILE AND ELONGATION TEST REPORT
SAMPLE-01

Test Sr. No.	**3813**	Test Date	**16/10/2021**
		Test Time	**3:15:09 PM**
Customer Name	**AVIH HYD**		
Customer Code	**BAMBOO+**		
Sample Details:			
Specimen code	**JF-01**		
Ref. Standard	**ASTM D638**		
Grip Length	**55**	Guage Length	**65**
Sample Width	**11.31**	Sample Thickness	**5.67**
Speed of testing (mm/min): **5**			

TABLE II

Obtained Results	Value	Unit
Area	64.1277	mm^2
Yield Force	837.37	N
Yield Elongation	3.13	Mm
Break Force	926.3	N
Break Elongation	3.34	Mm
Tensile Strength at Yield	13.06	N/mm^2
Tensile Strength at Break	14.44	N/mm^2
Tensile Strength at Max	14.48	N/mm^2
% Elongation	5.14	%
Max Force	928.69	N
Max Elongation	3.34	Mm
Modulus of Elasticity	330.71	N/mm^2

CONCLUSION

Sandwich type composite with bamboo and jute fiber were prepared by Hand Lay Up Techniques and characterized by mechanical tests (tensile Test, hardness test). The test results of the sandwich type composite are compared with bamboo fiber composite laminate.

The tensile test results of composite with bamboo improved with addition bamboo and jute sandwich type composite. This test was performed by universal testing machine; it was found that tensile strength addition jute and bamboo shown very good results compare to the bamboo fiber with epoxy resin.

REFERENCES

1. Sivasaravanan. S, V.K. Bupesh Raja, Manikandan, Glass Fiber and Nanoclay Reinforced Polypropylene Composites: Morphological, Thermal and Mechanical Properties, Sains Malaysiana 42(4) (2013):537–546. 2.
2. Ajith Gopinath, Senthil Kumar, Elayaperumal, "Review of low-velocity impact properties of composite materials", Composites Part A 1996; 27: 1123–1131.
3. M.Mohith, C.B.N Murthy, V.Nikhil murthy, Chacterization of Epoxy Hybrid composition: Effect of Glass/carbon fiber on Mechanical & Thermal Properties, International Journal & Management Engineering, Technology, Management and Research, volume no. 2(2015), Issue No:7 (July).
4. B.H. HUANG1, and Y.L. CHENG, "Mechanical characterization of Glass/Epoxy composite material with Nano clays", 19th International Congress of Mechanical Engineering.
5. P.M. Bhagvat, M.Ramachandran, and Pramod Raichurkar, "Mechanical Properties of Hybrid Glass/carbon fiber Reinforced epoxy composites", ICAAMM-2016, Materials Today Proceedings 4(2017) 7375-7380.
6. Milan Z mindaka, Martin Dubinsky. Mo-lin Chan, Kin-tak Lau, Tsun-tat Wong, Mei- po Ho, David Hui, "Mechanism of reinforcement in a nanoclay/polymer composite", Composites: Part B 42 (2011)1708–1712.
7. R.M. Jones, "Mechanics of Composite Materials", Taylor and Francis Publishers.
8. A.Vikram, V.Nikhil Murthy, C.B.N Murthy, Mechanical & Thermal Properties of carbon fiber/Epoxy composites with Different fiber Orientation, International Journal& Magazine of Engineering, Technology, Management and Research, Volume .2 (2015), Issue no:7(july), ISSN No:2348-4845.

FUZZY LOGIC CONTROLLER BASED DVR TO COMPENSATE VOLTAGE SAG AND SWELL WITH SRF THEORY

BODA HARIPRIYA[1] | M.RAGINI[2]

[1]PG SCHOLAR, Dept of EPS, AVANTHI INSTITUE OF ENGINEERING AND TECHNOLOGY, HYD, TS, INDIA.

[2] ASSISTANT PROFESSOR, Dept of EEE, AVANTHI INSTITUE OF ENGINEERING AND TECHNOLOGY, HYD, TS, INDIA.

ABSTRACT: In this paper we propose DVR based Realities regulator to compensate voltage related power quality issues. These days, power quality under the unreasonable execution of power gadgets is very difficult issue. The pay of non-sinusoidal; reactive and consonant; parts is the primary job for power quality gadgets which profoundly rely upon the heartiness of the control framework. Some normal control frameworks are executed utilizing Coordinated Fixed Casing (DQ) hypothesis. This paper proposes another form of DQ control procedure to control dynamic voltage restorer under extreme transient voltage conditions. The power framework network with the new DQ control method is considered and broke down under various situations to make up for extreme adjusted and uneven voltage droops and enlarges. This new plan depends on extraction of positive succession parts to execute the control calculation. A numerical model of the powerful voltage restorer (DVR), hysteresis voltage control, converter regulator model, new DQ plot with complete framework conditions are done and checked utilizing Simulink/MATLAB. They got consequences of the proposed remuneration calculation are contrasted and the outcomes got from the conventional DQ strategy. Simulation results are associated and show adequacy of the proposed DQ control plot.

KEYWORDS: DVR, SAG, DQ control, Power quality.

I.INTRODUCTION: Clinical equipment, processing plant computerization, semiconductor gadget producers, and paper factories are a number of the sensitive burdens that are sensitive to force-delivering unsettling impacts [1], [2]. The enlargement popular of excessive electricity and voltage security will become a dynamically simple worry with severe hazards and plenty of time taking place strength-best difficulty in the present strength networks. Voltage dangle and growth are presently perceived as excessively steeply priced outcomes, for instance, sensitive burdens stumbling and introduction misfortune [3]. Voltage droop and swell are important power problems that appear frequently throughout opportunity, exchange, and startling burden changes [4]. Extreme temperatures and lightning on electricity lines cause line-to-floor trouble, prompting a voltage hunch over a huge part

of the electric corporation. A few unique variables that have consequences in this aggravation are shortcircuits at the beginning of the force transmission line, the same energy dispersion line related to the reason in like manner coupling (PCC), high inrush flows related to the beginning of significant machines, unexpected modifications in load, the stimulating of force transformers, and exchanging tasks inside the electricity framework community. [5]. Voltage hold is the impermanent drop of the root implying rectangular (R.M.S.) voltage at a place inside the electric framework beneath a foreordained limit. It is a short-duration type of RMS that is really worth the voltage, ranging from 10 to 90% of the ostensible voltage throughout a length longer than zero. 5 cycles (10 ms) of force recurrence, yet now not precisely or equivalent to 60 seconds [6]. The terms used to describe the degree of voltage cling are habitually misjudged [7], [8]. As consistent with IEEE 1159-2019, a slump to 70% is permitted, which demonstrates that the line voltage is dropped to 70% of its widespread worth, not dropped via 70%. A voltage plunge of 70% will imply voltage dwindling by using 70% of the everyday 100 percent voltage. The excess voltage will be 30%, or a droop to 30% [9]. The consequences of a hold are habitually more recognisable than the influences of a swell. A hold with more than one cycle is frequently sizeable as a lower voltage yield. Lists are occasionally unrecognisable from quick blackouts in view that the impacts on the hardware are comparative [2], [10], [11]. PCs and other delicate hardware would possibly enjoy sudden closures or mutilated voltage waveforms [6]. Indeed, even engine starter transfers and contactors may be without difficulty affected by voltage droops, bringing about manner closure when the dropout takes place. For greater than one thousand cycles, a huge forte has been determined, converting from 20% to 65% hangs [12]. Enlarges are due to great burdens last down, fast changes in load resistivity, and distinct variables. Voltage growth is an electromagnetic aggravation that occurs in factors [12], [13]. At the factor when a voltage increase takes place, the RMS voltage will increment in short at a point over a predetermined degree. Both voltage stage and length of term impact the voltage amplify; the voltage swell's beginning area is each ounce of attempt, and the duration is going from 0.Five cycles (10 ms) to 60 seconds. The repercussions of a swell are habitually more harmful than those of a cling. The overvoltage trouble brings

about system faults in the energy supply hardware, but the impact is probably gradual and mixed. On the occasion that the span is longer than three cycles, the expansion in yield at a voltage is probably perceptible [7]. At the point when the agencies were using sturdy country gadgets, there was not a lot of importance to the nature of the furnished voltage. In any case, when the ventures supplant the strong kingdom gadgets with the energy digital gadgets, the character of the voltage supplied was the primary angle [14], [15]. The brief scope arrangements handy for voltage hang and swell are making use of an all-inclusive power deliver (85V–264V), utilising Semiconductor Gear and Materials Worldwide (SEMI F47) consistence power deliver, converting the day-out aspect, reinventing the reaction of bendy speed drives (ASD), utilising opposite-fueled transfers, single-level power conditioners, non-stop energy substances, constant voltage transformers, trickle-prong inverters, and so forth. The large-scope preparations available include making use of 3-degree electricity conditioners, 3-degree non-stop power resources, dynamic voltage conditioners, statistics wave, y wheel, dynamic voltage restorer (DVR), and so on [9].

A few power digital gadgets have been created to similarly expand voltage dependability and conquer the adverse effects of voltage droop or growth. DVR is a possible component for remuneration of voltage aggravation that is commonly utilised by and by [16] and [18]. Among the power hardware gadgets, DVR is a changing gadget that instigates simultaneous voltage and can be taken into consideration as a sequence dynamic strength lter. To have a financial and efficient power supply, DVR is utilized. It's an energy digital reality gadget applied for remuneration of voltage droops and enlarges electrical power dispersion [19]. The first DVR framework with static VAR devices, which was introduced in 1996 in Anderson, South Carolina, became a 12.47 kV framework. DVRs assist in settling issues in an energy framework that has voltage-unsettling effects. A functioning inverter modifies the voltage, either through a transformer or without a transformer, in series and in synchronisation with the matrix at the PCC [20], [21]. The estimation of the remuneration voltage is completed with the aid of contrasting the reference load voltage and the real voltage of the lattice. Under a voltage list or swell, the regulator recognises the quantity and duration of the repaid voltage required. The created reference

voltages are shipped off the modulator to supply the changing beats. These heartbeats would shoot the DVR switches, and the voltage from the DVR might be infused into the PCC to fill in for the voltage aggravations. Subsequently, DVR can be thought of or assumed as a channel that isolates the network from the heap and makes up for any voltage listing or swell. Accordingly, the give-up customer would not have the choice to stumble on or get affected by the difficulty of the voltage-unsettling influence instigated by the utility [4]. The major fear in the use of DVR is the efficient manipulation of DVR while infusing real and receptive energy [22]. In a DVR, the essential elements of the manage framework are to apprehend the voltage drops or expands, produce a voltage reference signal, control the converter, and ensure the safety of the framework [21], [23]. The first-class precision of the place techniques will have an enormous effect on the exhibition of the manage calculation. For instance, identity calculations like discrete Fourier change (DFT), quick fourier change (FFT), and Kalman sifting (KF) are applied to precisely anticipate voltage aggravations inside the inventory voltage [23], [24]. These calculations are known as identity calculations. The KF is a fair method for finding out which lists are adjusted and uneven. Clark's change and Park's exchange are utilised by the Coordinated Turning Edge (SRF) to distinguish slumps and swells [25]. The recreation area's trade or DQ change must be applied to the adjusted 3-degree lists. The severa DQ exchange is a trade approach that can be utilised for sounds and choppy hunch conditions. Different DQ exchanges became extra sincere through having separate modules for improving wonderful and terrible succession elements from important and symphonious waves [26], [27]. However, simple extraction of association elements is inconsistent for a single-degree framework; it neglects to differentiate the unbalanced stoop and swell voltages, and it has a complex method to get the reference voltage to manipulate the DVR. The DQ enjoys a brief span for the popularity of slump/amplify in a three-stage framework.

II.PROPOSED SYSTEM: This postulation proposes a changed DQ strategy for DVR control. The proposed recognition method depends on a period space calculation for distinguishing positive grouping part of framework voltage. This DQ strategy depends on identification procedure of succession parts which doesn't comprise both versatile instrument (like PI regulator)

and sign sifting [26], [28]. This gives less computational time prompting quick reaction of the control framework with nice strength and extensive variety of working circumstances including outrageous hangs and enlarges. Dissimilar to other technique, the proposed strategy is viable for both adjusted and uneven frameworks. Furthermore, this control strategy accomplishes right around zero following blunder in all strange working circumstances. The control framework is numerically addressed and confirmed in reproduction. At last, the proposed control is contrasted with the customary DQ technique to affirm the prevalence of the proposed strategy.

DYNAMIC VOLTAGE RESTORER (DVR)

To reestablish the heap side voltage to the ideal sufficiency and waveform, infusion of remuneration voltage with wanted extent and recurrence is fundamental [16]. The framework can infuse up to half of ostensible voltage, however just for a brief time frame (up to 0.1 second). Be that as it may, most voltage droops are considerably less than 50%. This is supposed to be Dynamic voltage reclamation or guideline. The controlling gadget is supposed to be DVR [29]. DVRs might give great answers for end-clients subject to undesirable power quality unsettling influences [30]. Figure 1 shows a fundamental DVR power framework circuit upheld with control circuit to infuse repaid voltage for keeping up with the voltage at wanted esteem [24], [31]. DVRs normally introduced on a basic feeder providing the dynamic power through DC energy capacity and the expected responsive power is produced inside [4].

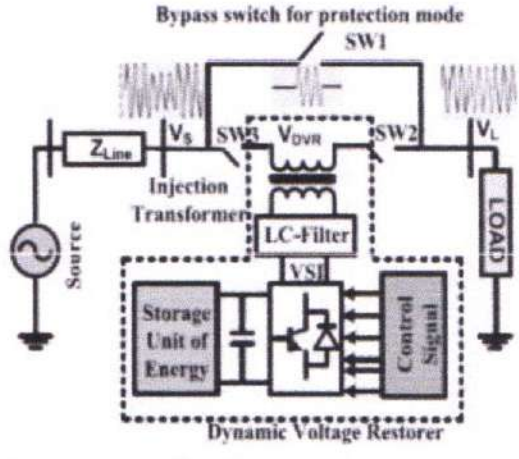


FIGURE 1. Basic circuit of power system with DVR.

A. Activity Methods OF DVR

In light of the working, a DVR methods of activity are partitioned in to three modes, which are, Security, Backup and voltage infusion [21], [32]. In security mode, surpassing the heap current over reasonable worth due the short out or enormous inrush current, DVR will be confined from the power framework utilizing switches, SW2 and SW3 as displayed in Figure 1 and

accordingly giving an elective way to the heap current course through SW1 [32], [13]. In backup mode, the low voltage twisting of the promoter transformer is shorted by the converter and full burden current is gone through the essential of the sponsor transformer. In this method of activity, the DVR won't infuse any remuneration voltage into the power framework organization. This method of activity is started when an unsettling influence in voltage is identified and closes when the voltage is recuperated to its not unexpected working condition.

B. COMPENSATION Techniques

Voltage remuneration techniques are chosen in view of the DVR power rate, load types, circumstances, shortcoming types, etc [14]. The remuneration techniques are separated into pre-list, in-stage, and energy limited. In pre-droop, the regulator screens the stockpile voltage and recognize any voltage vacillations, then creates and infuses the distinction of voltage. Thus, the heap voltage stays unaltered as the pre-hang voltage. In-stage pay approach, the infused voltage and voltage of supply are in stage with each another [33]. This approach isn't reasonable for touchy burdens as stage shift happen during most voltage hang situations. Then again, it is appropriate for straight loads when the voltage greatness is huge. The principal disadvantage of the pre-hang and in-stage strategies is to give genuine power at the DC-connect. This can be overwhelmed by Energy-limited (EM) technique, as the trading of dynamic power isn't done during the remuneration stage. It very well may be expressed exceptionally for droop alleviation that genuine power is neither infused into the organization or ingested from the power supply [21].

C. DVR CONTROL TYPES DVR

Control plans are separated into two classifications: direct and nonlinear [35]. While working with static power converters, direct control is normally utilized as the regular technique. This control is generally utilized in the power quality frameworks, for example, to carry out pay of voltage or current aggravations, to shield basic hardware from falling flat, to lessen monetary misfortune [36], [37]. Clinical and modern frameworks that are delicate and significant ought to be safeguarded in a solid and savvy way. Nonlinear regulators are more proper than straight regulators. One huge hindrance of the nonlinear regulator is that subsidiary tasks can make issues with electromagnetic impedance on inverter exchanging, bringing about significant control blunders. in reality, a high pass channel can be utilized to substitute the

subordinate way of behaving, which further develops execution while constricting high recurrence commotion in sensors and links.

D. CONTROL Systems AND Calculations OF DVR

The revelation of voltage aggravations is the critical highlight of the DVR's control structure. Expressly with sensitive weights, the perceiving system should be rapidly sufficient to recognize the voltage disrupting impact exactly for assessment of DVR execution [22][23]. As shown in Figure 2, distinct procedures for voltage disturbance area have been proposed, including RMS, Apex Worth, DFT, Fourier Change (FT), Wavelet Change (WT),Windowed Fast FT (WFFT), ABC to DQ center point change, KF, Stage Locked Circle (PLL), and SRF [39], [41]. The benefits and disadvantages of the most serious voltage irritation acknowledgment strategies are given in Table 1.

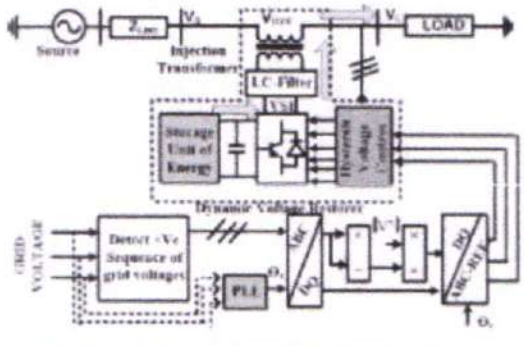


FIGURE 2. Schematic diagram of the proposed system with DVR.

E. PROPOSED SYSTEM DESCRIPTION

The proposed design displayed in Figure 3 incorporates a stockpile (network) voltage with lattice impedance, a three-stage load, an infusion transformer, and the DVR framework. The DVR framework contains a Voltage Source Inverter (VSI) controlled by a DC power source with a dc connect capacitor, and a symphonious latent channel. A three-stage adjusted and lopsided burden is viewed as in this framework [39], [41].

1) ENERGY Stockpiling UNIT AND DC-Connection CAPACITOR The energy stockpiling framework (ESS) and the dc connect capacitor are two fundamental parts in a DVR framework that provisions the dynamic power expected to safeguard against delayed disturbances. The dc interface capacitor is an energy stockpiling gadget that produces high-power brief time frame heartbeats to offer unique reaction [12], [22]. A DVR's ESS is for the most part comprised of a battery. Table 2 represents the energy and power thickness of normal capacitors and batteries, as well as their life cycle count and release times. A battery and a capacitor can be utilized together to meet the energy prerequisites of a DVR, as demonstrated in Table 2. The application

decides the size of an energy stockpiling gadget [45]. The typical energy stockpiling necessities for power lattice evening out, power quality, and specific apparatuses are introduced in Table 3. A DVR framework's energy stockpiling limit should be adequate to satisfy the power quality and custom gadget prerequisites for a couple of moments and cycles, individually.

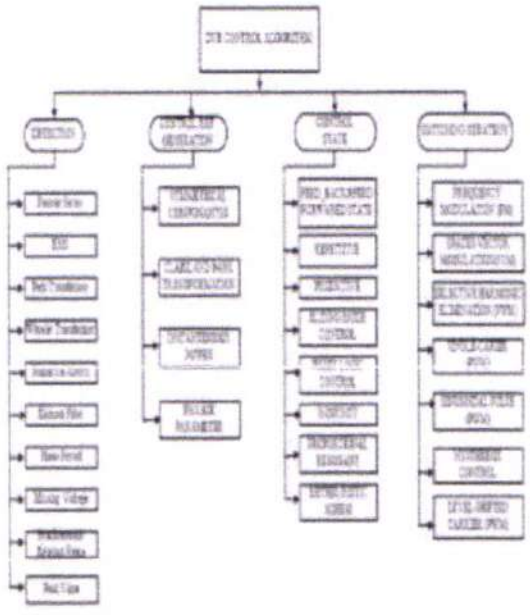
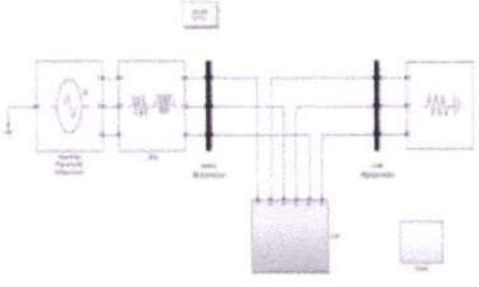


FIGURE 2. Flow chart for control strategies of DVR.

III.SIMULATION RESULTS



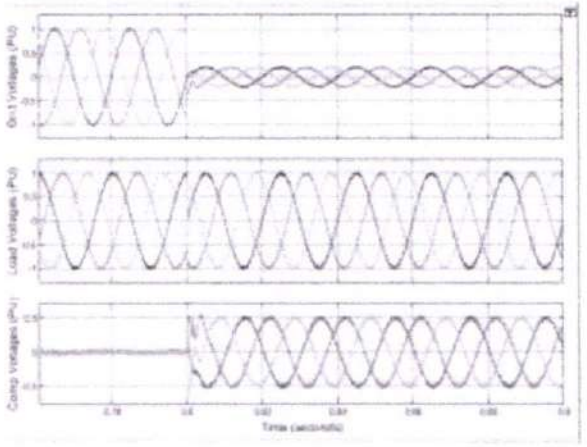


FIGURE 3.1. Simulation results of grid voltages, load voltage and DVR voltages (modified DQ) under balanced 3ϕ grid voltage sag of 20%.

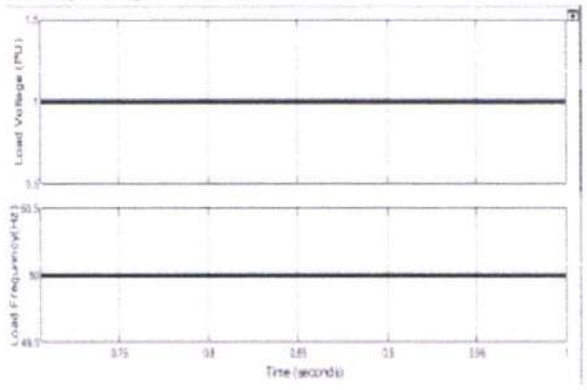


FIGURE 3.2. [Upper] pu load voltage, [Lower] load frequency under balanced 3ϕ grid voltage sag of 20%.

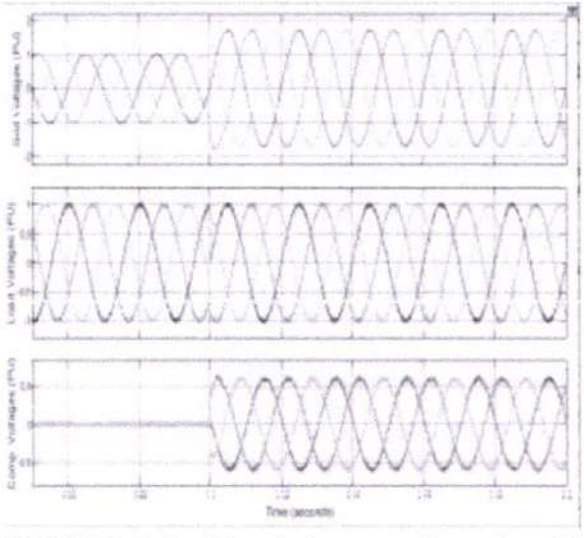


FIGURE 3.3. Simulation results of grid voltages, load voltage and DVR voltages (modified DQ) under balanced 3ϕ grid voltage swell of 70%.

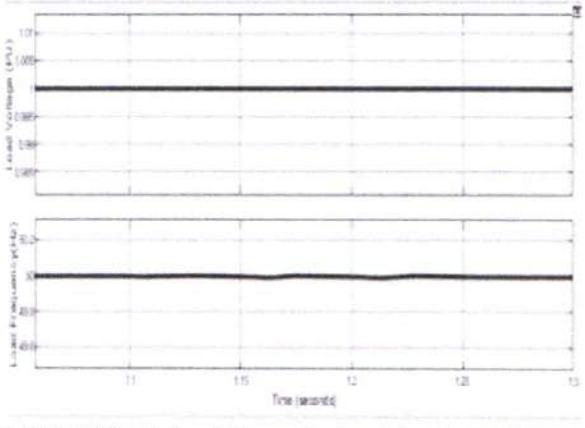


FIGURE 3.4. [Upper] pu load voltage, [Lower] lower load frequency under balanced 3ϕ grid voltage swell of 70%.

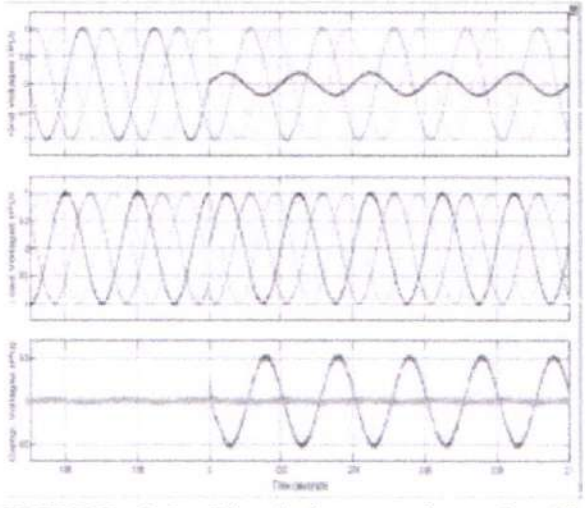


FIGURE 3.5. Simulation results of grid voltages, load voltage and DVR voltages (modified DQ) under unbalanced 3ϕ grid voltage sag of 20%.

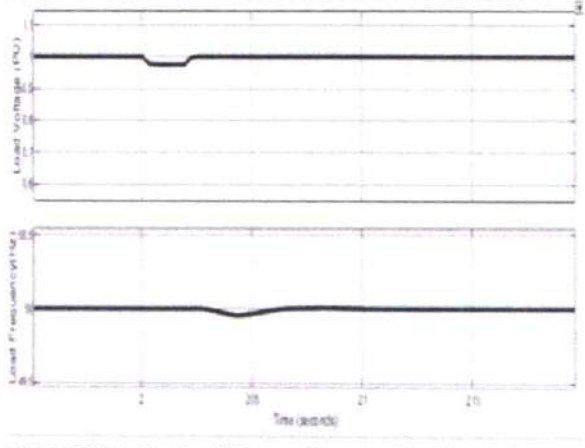


FIGURE 3.6. [Upper] pu load voltage, [lower] load frequency under balanced 3ϕ grid voltage sag of 20%

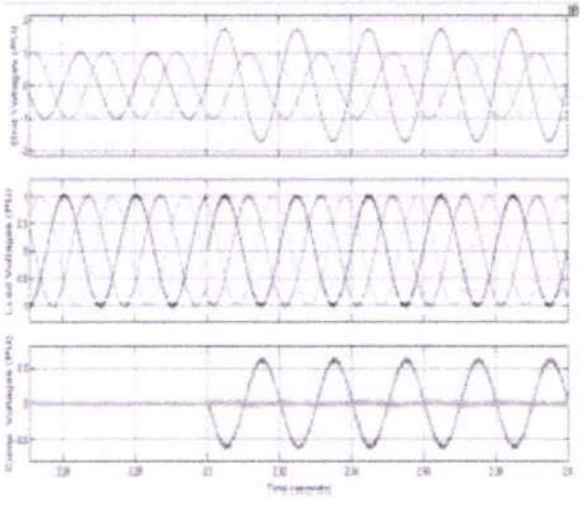


FIGURE 3.7. Simulation results of grid voltages, load voltage and DVR voltages (modified DQ) under unbalanced 3ϕ grid voltage swell of 70%.

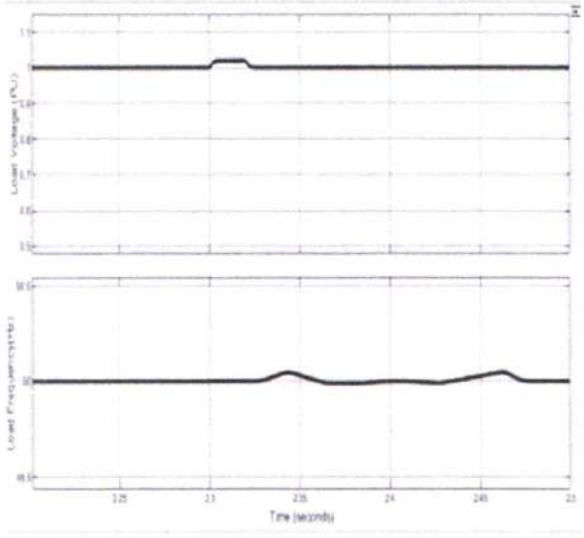


FIGURE 3.8. [Upper] pu load voltage, [lower] load frequency under balanced 3ϕ grid voltage swell of 70%.

IV.CONCLUSION

This paper assesses the control of DVR with changed DQ calculation to produce reference voltage signs to control the DVR. The proposed DVR control technique depends on a changed rendition of DQ hypothesis with a discovery strategy for the positive and negative succession parts. The demonstrated reproductions are done in MATLAB Simulink. The outcomes are shown great connection among's proposed and ordinary outcomes. The control of adjusted DQ strategy is contrasted and the conventional DQ control method under the states of serious hang and swell. The presentation of the regulators is likewise contrasted during adjusted and lopsided circumstance and serious instances of hang and swell. The near results recommend that the new adjusted DQ control strategy shows compelling in remunerating voltage during extreme hang enlarge in offset and unbalance conditions with benefits of

- Less computational exertion.
- Quicker reaction.
- Less transient wavering in the key recurrence under lopsided voltage sag and swell.

REFERENCES

[1] S. Hasan, K. Muttaqi, D. Sutanto, and M. A. Rahman, ``A novel dual slope delta modulation technique for a current source inverter based dynamic voltage restorer for mitigation of voltage sags," IEEE Trans. Ind. Appl., vol. 57, no. 5, pp. 54375447, Scp. 2021, doi: 10.1109/TIA.2021.3089984.

[2] B. Bae, J. Jeong, J. Lee, and B. Hen, ``Novel sag detection method for lineinteractive dynamic voltage restorer," IEEE Trans. Power Del., vol. 25, no. 2, pp.

12101211, Apr. 2010, doi: 10.1109/TPWRD.2009.2037520.

[3] M. Vilathgamuwa, A. A. D. Ranjith, S. S. Choi, and K. J. Tseng, ``Control of energy optimized dynamic voltage restorer,'' in Proc. IECON Conf. 25th Annu. Conf. IEEE Ind. Electron. Soc., vol. 3, Dec. 1999, pp. 873878.

[4] P. Li, L. Xie, J. Han, S. Pang, and P. Li, ``New decentralized control scheme for a dynamic voltage restorer based on the elliptical trajectory compensation,'' IEEE Trans. Ind. Electron., vol. 64, no. 8, pp. 64846495, Aug. 2017, doi: 10.1109/TIE.2017.2682785.

[5] N. C. S. Sarita, S. S. Reddy, and P. Sujatha, ``Control strategies for power quality enrichment in distribution network using UPQC,'' Mater. Today, Proc., vol. 10, Feb. 2022, doi: 10.1016/j.matpr.2021.07.053.

[6] S. M. Deckmann and A. A. Ferrira, ``About voltage sags and swells analysis,'' in Proc. 10th Int. Conf. Harmon. Quality Power, Oct. 2002, pp. 144148, doi: 10.1109/ICHQP.2002.1221423.

[7] F. K. de Araújo Lima, J. M. Guerrero, F. L. Tofoli, C. G. C. Branco, and J. L. Dantas, ``Fast and accurate voltage sag detection algorithm,'' Int. J. Electr. Power Energy Syst., vol. 135, Feb. 2022, Art. no. 107516, doi: 10.1016/j.ijepes.2021.107516.

[8] Z. Elkady, N. Abdel-Rahim, A. A. Mansour, and F. M. Bendary, ``Enhanced DVR control system based on the Harris hawks optimization algorithm,'' IEEE Access, vol. 8, pp. 177721177733, 2020, doi: 10.1109/ACCESS.2020.3024733.

[9] IEEE Recommended Practice for Monitoring Electric Power Quality, Standard 1159-2019, IEEE Standards Association, 2019.

[10] M. I. Hossain, I. Rahaman, M. N. Rahman, M. F. Hasan, M. M. Hasan, and R. C. Sarker, ``Voltage sag compensation in distribution system using dynamic voltage restorer,'' in Proc. 2nd Int. Conf. Adv. Inf. Commun. Technol. (ICAICT), Nov. 2020, pp. 492497, doi: 10.1109/ICAICT51780.2020.9333502.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Implementation Of Cryptography Using Rom Sub Modules And Exclusion Of Shift Rows

K Narsimha
MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: prasannavemuganti@gmail.com

Dr.S. Kishore Reddy
Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

G Srinivas
Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: sri414china@gmail.com

Abstract-In this article, we present a simple, yet energy- and area-efficient method for tolerating the stuck-at faults caused by an endurance issue in secure-resistive main memories. In the proposed method, by employing the random characteristics of the encrypted data encoded by the Advanced Encryption Standard (AES) as well as a rotational shift operation, a large number of memory locations with stuck-at faults could be employed for correctly storing the data. The technique may be employed along with other error correction methods, including the error correction code (ECC) and the error correction pointer (ECP). To assess the efficacy of the proposed method, it is implemented in a phase-change memory (PCM)- based main memory system and compared with three error tolerating methods. The results reveal that for a stuck at fault occurrence rate of 10−2 and with the method is similar to that of the state-of-the-art method.

Keywords- **Advanced Encryption Standard, error correction code, phase-change memory**

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

I. INTRODUCTION

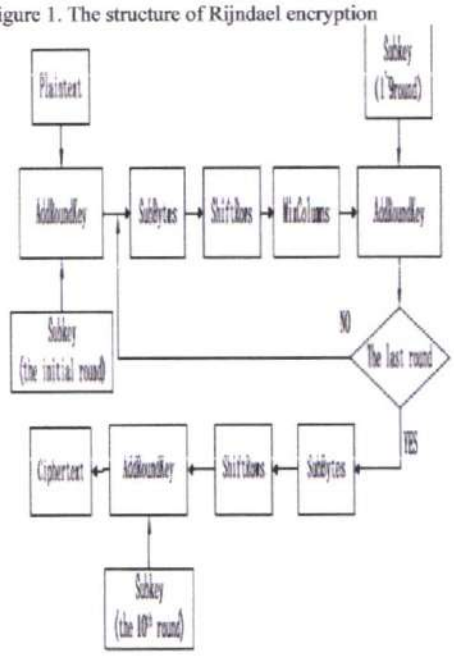
AES is short for Advanced Encryption Standard and is a United States encryption standard defined in Federal Information Processing Standard (FIPS) 192, published in November 2001. It was ratified as a federal standard in May 2002. AES is the most recent of the four current algorithms approved for federal us in the United States. One should not comparison with RSA, another standard algorithm, as RSA is a different category of algorithm. Bulk encryption of information itself is seldom performed with RSA.RSA is used to transfer other encryption keys for use by AES for example, and for digital signatures. AES is a symmetric encryption algorithm processing data in block of 128 bits. A bit can take the values zero and one, in effect a binary digit with two possible values as opposed to decimal digits, which can take one of 10 values. Under the influence of a key, a 128-bit block is encrypted by transforming it in a unique way into a new block of the same size.. Each additional bit in the key effectively doubles the strength of the algorithm, when defined as the time necessary for an attacker to stage a brute force attack, i.e., an exhaustive search of all possible key combinations in order to find the right one.

II. EXISTING METHOD

A. *Brief Description of Rijndael Algorithm*

Rijndael algorithm consists of encryption, decryption and key schedule algorithm. The main operations of the encryption algorithm among the three parts of Rijndael algorithm include: bytes substitution (Sub Bytes), the row shift (Shift Rows), column mixing (Mix Columns), and the round key adding (AddRoundKey). It is shown as Fig. 1.

figure 1. The structure of Rijndael encryption



algorithm

Encryption algorithm processes Nr+1 rounds of transformation of the plaintext for the ciphertext. The value of Nr in AES algorithm whose packet length is 128 bits should be 10, 12, or 14 respectively, corresponding to the key length of 128,192,256 bits. In this paper, only the (AES-128) encryption scheme with 128-bit keys is considered.

B. *The Design of Improved AES-128 Encryption Algorithm:*

- Two main processes of AES encryption algorithm:

The AES encryption algorithm can be divided into two parts, the key schedule and round transformation. Key schedule consists of two modules: key expansion and round key selection. Key expansion means mapping Nk bits initial key to the so-called expanded key, while the round key selection selects Nb bits of round key from the expanded key module.

Round Transformation involves four modules by Byte Substitution, Byte Rotation, MixColumn and AddRoundKey.

C. *The Process of New algorithms*

From the above analysis, we can find that the process of AES encryption can be mainly divided into two parts: key schedule and round transformation. The improved structure is also divided into these two major processes. The initial key will be sent to the two modules: Key expansion and Key selection, while the plaintext is to be sent to the round transformation after the roundkey is selected. But the operand of data transmission is turned into a 32-bit unit. The process of new algorithm is shown as Fig.

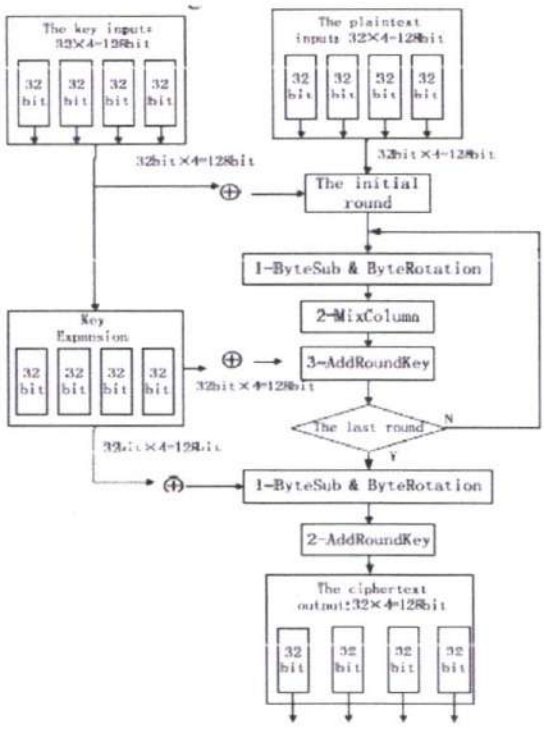


Figure 2. The new improved structure of AES algorithm

The functions of various parts of the structure shown above are described as follow:

- The initial round of encryption:

The four packets of consecutive 32-bit plaintext (128 bits) have been put into the corresponding registers. Meanwhile, another four packets of consecutive 32-bit initial key (128 bits) have been put into other registers by the control of the enable clock signal. Furthermore, this module should combine the plaintext and initial key by using the XOR operators.

D. Round Transformation in the intermediate steps:

A round transformation mainly realizes the function of SubBytes and MixColumns with 32-bit columns. Four packets of round transformation are processed independently. Then the results of MixColumns and the 32-bit keys sourced from Keyexpansion are combined by using XOR operators. Here, the round transformation is a module with 64 input ports (32-bit plaintext+32-bit key) and 32 output ports.

The function of SubByte is realized by Look-Up Table (LUT). It means that the operation is completed by the Find and Replace after all replacement units are stored in a memory (256×8bit = 1024 bit).

The implementation of MixColumn is mainly based on the mathematical analysis in the Galois field GF(28). Only the multiplication module and the 32-bit XOR module of each processing unit(one column) are needed to design, because the elements of the multiplication and addition in Galois field are commutative and associative. Then the function of MixColumn can be achieved. Fig.5 is a block diagram for the introduction of pipelining technology used in the round transformation.

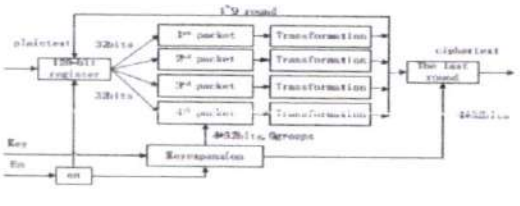


Figure 3. The round processing with pipeline technology

In the process of pipelining, the 128-bit data is divided into four consecutive 32-bit packets that take ound transformation independently.

The operation of the above four groups of data can be realized in pipelining technology. In brief, it can be described as follow: store the unprocessed data in the 128-bit register, and

control the clock for re-starting the 128-bit register to read the new data when the four groups' operations have been overcome. Thus the 128-bit round-operating unit has been transformed into four 32-bit round-operating elements. The internal pipelining processing should be implemented during the whole nine intermediate Round Transformations of the four packets before achieving the 128-bit ciphertext.

- The process of the last round

The final round is a 128-bit processor. After nine rounds of operations included Shiftrows, SubByte and Mixclumns, the 128-bit intermediate encrypted data will be used in XOR

operation with the final expanded key(4*32bit), which is provided by the key expansion module. The output of final round in the processor is the desired 128-bit ciphertext. Similarly, the ciphertext is divided into four packets of 32- bit data by an external enable signal.

- Key expansion and Key extraction

This module is implemented basically the same with the traditional way as another part of the AES encryption algorithm. The only difference lies on the mode of data transmission. The

initial key and expanded keys are divided into four 32-bit data before being extracted.

All of the above modules can be decomposed into basic operations of seeking and XOR if the AES algorithm is implemented on FPGA. So the basic processing unit (look-uptable)of FPGA can be used. The operation of AddRoundKey is taken first in each round. When the plaintext and initial key are input, the encryption module starts running, and the expanded keys are stored into the registers at the

same time. This implementation method is independent on a specific FPGA.

III. VLSI

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

A. VLSI and systems

These advantages of integrated circuits translate into advantages at the system level:

Smaller physical size. Smallness is often an advantage in itself-consider portable televisions or handheld cellular telephones.

Lower power consumption. Replacing a handful of standard parts with a single chip reduces total power consumption. Reducing power consumption has a ripple effect on the rest of the system: a smaller, cheaper power supply can be used; since less power consumption means less heat, a fan may no longer be necessary; a simpler cabinet with less shielding for electromagnetic shielding may be feasible, too.

Reduced cost. Reducing the number of components, the power supply requirements, cabinet costs, and so on, will inevitably reduce system cost. The ripple effect of integration is such that the cost of a system built from custom ICs can be less, even though the individual ICs cost more than the standard parts they replace.

A. ASIC

An Application-Specific Integrated Circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely to run a cell phone is an ASIC. Intermediate between ASICs and industry standard integrated circuits, like the 7400 or the 4000 series, are application specific standard products (ASSPs).

As feature sizes have shrunk and design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 gates to over 100 million. Modern ASICs often include entire 32-bit processors, memory blocks including ROM, RAM, EEPROM, Flash and other large building blocks. Such an ASIC is often termed a SoC (system-on-a-chip). Designers of digital ASICs use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

Field-programmable gate arrays (FPGA) are the modern-day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs and/or lower production volumes, FPGAs may be more cost effective than an ASIC design even in production.

- An application-specific integrated circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use.
- A Structured ASIC falls between an FPGA and a Standard Cell-based ASIC

Structured ASIC's are used mainly for mid-volume level design. The design task for structured ASIC's is to map the circuit into a

IV. PROPOSED METHOD

A. Introduction

Computational processing has increased in cloud servers, requiring larger core counts and higher memory densities. The number of processor cores doubles every two years, while the DRAM DIMM capacities double every three years [1]. This causes a large gap between the core count and the memory density. On the other hand, traditional DRAM chips consume more than 40% of power of the servers [2]. Also, DRAM scaling to reach a higher memory density has some challenges such as high leakage current, reduced memory cell reliability, and more

complex fabrication processes [3]. Emerging memory technologies, which are categorized into volatile (DRAM-based) and nonvolatile (resistive-based (have been introduced to solve scaling and power consumption problems [4]. Some of the volatile DRAM-based memories include reduced latency and tiered latency DRAM (RL-DRAM and TL-DRAM) and low power DDR DRAM (e.g., LPDDR3, LPDDR4) architecture. While they have lower latency and power consumption, they suffer from higher costs of the fabrication process [5]. algorithms increase by enlarging the number of errors imposing considerable overheads on the system .

B. Randshift Method

As mentioned before, owing to the limited write endurance of the PCM, some of the cells are worn-out, permanently become stuck-at "1" or "0" value. The idea of fault coverage based on "ST-R" and "ST-W" is demonstrated by a memory word shown in Fig. 1, where 4-bit positions have stuck-at faults (i.e., the bit positions of 0, 4, 10, and 13). For example, in this memory word, storing "0xB3A8" leads to ST-W at the 4th- and 13th-bit positions. In this case, a 1-bit circular shift to the right causes the value to become "0x59D4" giving rise to ST-R at the 4th- and 13th-bits without inducing any other ST-W. As stated previously, the correlation of any two AES encrypted data is almost zero, and thus one may consider the output of the AES encryption as a random number.

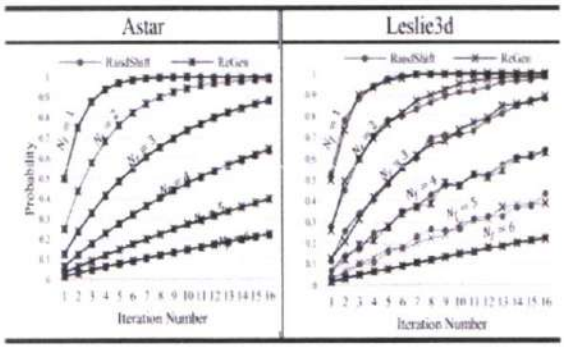


Figure 4 Probability of fault coverage.

In Fig, the average correlation coefficient of AES-128 encryption for 50K 128-bit encrypted memory data in the "astar" benchmark from CPU2006 is shown [22]. As Fig. indicates, the illustrated average is very close to zero implying a low relationship between the output data in each iteration of the AES encryption method. The randomness feature of the output value in the AES may be employed as a solution to tolerate stuck-at faults in PCM cells. However, in the case of raw data (data that are not encrypted), due to the existence of spatial/temporal correlations among the data blocks, the use of manipulating methods (e.g., circular shifting or inversing) may not be appropriate for overcoming the problem of the stuck-at faults. If the encrypted data fail to fully match with the stuck-at faults (the number of "ST-W" is zero), one may use the technique suggested in [12] to regenerate the encrypted data.

Otherwise, a data write failure exception signal is issued to inform, e.g., the processor of the write failure (lines 14–19).

As mentioned before, due to the possibility of having to do a large number of regenerations, this technique is a power-hungry approach. Each mismatch between the writing data and the stuck-at fault values causes to add ten rounds of add-Round-Key, substitute, shift-Rows, and mix-Column in AES-128. Although data shifting approach, as well as the generation of new encrypted data may not completely keep the randomness of the data, it may increase the number of "ST-R" in the case when there are not many stuck-at fault bits in the memory block. Obviously, the former approach is considerably faster and more energy efficient. Since the RandShift approach is applied on the encrypted data whose bits enjoy a high degree of randomness, the disturbance in the randomness in the RandShift approach is similar to that in the regeneration approach. To evaluate the efficacy of the proposed RandShift method compared to the one proposed in [12] (which is denoted ReGen in the rest of this article), probabilities of the stuck-at fault coverages of the two methods should be compared. Because of the randomness property of AES encryption, there is no dependency between the previous and the next data generations at each time in the ReGen method [12]. Because of the data dependency between the shifted bits in the RandShift method, extracting a close-form formula to calculate the fault coverage probability is not possible.

The coverage probabilities of RandShift and ReGen were obtained by applying one million encrypted data as stimuli. In this article, the number of faults in 128 bits of data does not exceed six for the assumed distribution. In Fig, the parameter Diff indicates the average absolute difference between the two cases of RandShift and ReGen. When a data write request arrives from the LLC, the memory controller encrypts the data block (lines 1 and 2). Then, the RowVerifier checks the stuck-at faults value and their positions by storing and reading the pattern of all 1s and 0s in the memory [6] (line 3). Next, the RandShift method iterates until the shifting process hides all stuck-at faults (lines 4–13) or the number of iterations reaches a predefined value. Finally, if all faults are matched, the data write process will be performed.

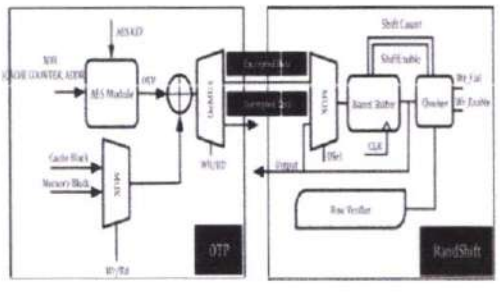


Figure 5. Full architecture of RandShift.

V. CONCLUSION

In this work, we proposed a method employing the randomness feature of AES encryption as well as rotational shift operation to tolerate hard faults in nonvolatile memory cells. This method, which was called RandShift, enjoyed the simple hardware implementation and low energy consumption. It limited the need for exploiting powerful error correction methods, such as ECC and ECP. The results of our comparative study showed up to 82% lower energy consumption for RandShift when obtaining about the same fault coverage as that of the state-of-the-art technique.

VI. FUTURE SCOPE

A FPGA implementation of area-optimized AES algorithm which meets the actual application is proposed in this paper. After being coded with Verilog Hardware Description Language, the waveform simulation of the new algorithm was taken in platform. Ultimately, a synthesis simulation of the new algorithm has been done. The result shows that the design with the pipelining technology and special data transmission mode can optimize the chip area effectively.

REFERENCES

[1]. Madakam, Somayya, R. Ramaswamy, and Siddharth Tripathi. "Internet of Things (IoT): A literature review." Journal of Computer and Communications 3, no. 05 (2015): p.164.

[2]. Wang, Yong, Garhan Attebury, and Byrav Ramamurthy. "A survey of security issues in wireless sensor networks." IEEE Communications Surveys Tutorial (2006).

[3]. Veeramallu, B., S. Sahitya, and Ch LavanyaSusanna. Veeramallu, B., S. Sahitya, and Ch LavanyaSusanna. "Confidentiality in Wireless sensor Networks." International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-2, Issue-6, January 2013.

[4]. Eisenbarth, Thomas, and Sandeep Kumar. "A survey of lightweightcryptography implementations." IEEE Design & Test of Computers 24.6 (2007).

[5]. Banik, Subhadeep, Andrey Bogdanov, and Francesco Regazzoni. "Exploring energy efficiency of lightweight block ciphers." International Conference on Selected Areas in Cryptography. Springer, Cham, 2015.

[6]. Bogdanov, Andrey, et al. "PRESENT: An ultra-lightweight block cipher." CHES. Vol. 4727. 2007.

[7]. Borghoff, Julia, et al. "PRINCEa low-latency block cipher for pervasive computing applications." International Conference on the Theory and Application of Cryptology and Information Security. Springer, Berlin, Heidelberg, 2012.

[8]. Beaulieu, Ray, et al. "The SIMON and SPECK lightweight block ciphers." Design Automation Conference (DAC), 52nd ACM/EDAC/IEEE. IEEE, 2015.

[9]. Suzaki, Tomoyasu, et al. "TWINE: A Lightweight Block Cipher for Multiple Platforms." Selected Areas in Cryptography. Vol. 7707. 2012.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Implementation of SRAM Based Error Correction and Detection in Memory System Using LFSR

M Mounika

MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India. Email: mounika.murari@gmail.com

Dr. S. Kishore Reddy

Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg.&Tech., India. Email: kishorereddy416@gmail.com

V Nagaraju

Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India. Email: vasanthanagayadav@gmail.com

Abstract-**Ternary Content Addressable Memories, or TCAMs, are often used by network devices in order to conduct packet categorization. For example, they are used in the construction of software-defined networks, the management of security, and the transmission of packets (SDNs). TCAMs are often used either as standalone devices or as a component embedded into networking application-specific integrated circuits. TCAMs may also be used in either capacity simultaneously. When working with memory, one of the problems that might arise is the possibility of soft errors destroying the bits that have been saved. The memories might be protected by using an error-correcting code or a parity check to locate any errors; however, doing so would require an increase in the number of memory bits used each word. This approach takes into consideration the need of maintaining the integrity of the memory while simulating TCAMs. This technique gives protection against soft faults and the error correcting strategy that provides rapid response time, inexpensive cost, and excellent search performance in order to deliver an error-free SRAM-Based TCAM Design. In addition, this method offers protection against hard faults.**

Keywords- TCAMs, SRAM, Transmission, Parity Check, Soft Faults.

Manuscript received Dec 10, 2022; Revised Dec 25, 2022; Accepted Dec 31, 2022

1. INTRODUCTION

Very-large-scale integration (VLSI) integration refers to the process of creating an integrated circuit by placing a large number of semiconductors on a single chip (IC). In the 1970s, as more complex semiconductor and communication technologies were being created, very large-scale integration (VLSI) was first introduced. The chip in question is a very large-scale integration device. Before the development of VLSI technology, the bulk of ICs were only capable of carrying out a limited number of functions simultaneously. An electrical circuit may include a central processing unit (CPU), ROM, random access memory (RAM), and several other components. VLSI makes it possible to put all of them into a single chip.

The history of the transistor may be traced back to the middle of the 1920s, when many inventors attempted to change the current that was running through solid-state diodes so that they would become triodes. This was the first step in the development of the transistor. Since the end of the Second World War, the production of radar detectors using silicon or germanium crystals has significantly contributed to the advancement of both practical and theoretical knowledge. Researchers working in the field of radar have started producing solid-state radar systems again. The era of vacuum tubes gave way to that of solid-state devices when the transistor was invented at Bell Labs in 1947. This marked the beginning of the modern technological era.

In the 1950s, mechanical engineers came to the realization that the relatively simple transistor might be employed in the construction of more complex

circuits. However, complications emerged as the level of circuit intricacy grew. The magnitude of the circuit was one of the issues. The dynamic circuit of speed was similar to a machine. The length of the wires that are connected to the modules will be increased due to the fact that they are through. Before the electronic impulses could be sent via the device, the circuit had to first slow down the device. When Jack Kilby and Robert Noyce built the integrated circuit, they solved this issue by combining all of the components of the semiconductor material into a single block. This allowed the integrated circuit to function (monolith). This is necessary in order to complete the loops and make the manufacturing process more efficient. This gave birth to the concept of medium-scale convergence in the beginning of the 1960s, which is when all of the components are placed on a single silicon wafer. (LSI) and VLSI, which incorporate hundreds of millions (109) of transistors on a single chip, were created by (MSI) in the late 1960s and then again in the 1970s and 1980s. (MSI) was a pioneer in the field of integrated circuitry.

Two transistors were included on the first semiconductor devices. Eventually, additional transistors were added, which resulted in the progressive creation of a variety of different features or devices. These developments occurred as a direct result of the steady addition of more transistors. Because the first integrated circuits only required a small number of parts—perhaps 10 diodes, transistors, resistors, and condensers—it was possible to build one or more logic gates on a single component. This was made possible by the fact that integrated circuits only required a small number of components. The advancement of technology has led to the creation of systems that include hundreds of logic gates. These systems are now referred to as medium-scale integration (MSI), while they were formerly known as small-scale integration (SSI). More advancements were made possible as a result of more sophisticated integration (LSI), which refers to devices that have at least one thousand logic gates. The fact that modern microprocessors have hundreds of unique transistors and many millions of gates is indicative of how far technology has progressed since then.

A. Engineering for SSI

The first integrated circuits had a small number of transistors. The term "small-scale integration" (SSI) refers to the use of logic gates in binary circuits with tens-numbering transistors; early linear integrated circuits, such as the Plessey SL201 or Philips TAA320, featured just two transistors. Rolf Landauer, an IBM researcher, was the first to use the terms SSI, MSI, VLSI, and ULSI when formulating the scientific definition.

B. Engineering for MSI

The next phase in the process of building integrated circuits was the invention of "small integration" (MSI) modules in the late 1960s. These modules each included several hundred transistors and were the next step in the process of building integrated circuits. The fact of the matter is that even if the cost of production was comparable to SSI, it would still be preferable to produce more complex devices with smaller circuit boards, less labor-intensive assembly (due to fewer individual components), and a number of other advantages. This is because of the fact that the reality of the situation is as follows.

C. LOW Scale Inclusion

In the middle of the 1970s, a phenomenon known as "wider convergence," which consisted of tens of thousands of transistors on a single chip, evolved as a response to the same economic forces. In the early 1970s, the production of integrated circuits started in small numbers. At that time, the first microprocessors, computer chips, and 1K-bit RAMs were among the integrated circuits that were created. The first true 10,000-transistor LSI circuits for device huge memory and second-generation microprocessors were invented around 1974.

Using very large scale integration (VLSI), an effort was originally made to calibrate and define various degrees of specific integration. developed concepts like as (ULSI). However, the many doors and transistors that can be seen on modern technology serve as a perfect representation of these wonderful distinctions. Conditions that are more stringent than the VLSI convergence requirements are utilized much less often now. 2008 was the year when billion-transistor processors were available on the commercial market. The manufacture of semiconductors progressed, and new 65 nm technologies were discovered, which led to an increase in its popularity. Recent designs make advantage of robust and independent transistor logic synthesis, which contributes to an increase in the complexity of the logic implementation that is produced. In addition, various hand-crafted high-performance logic blocks, such as the static-random access memory (SRAM) cell, have been designed in order to get the greatest possible output.

2.FPGA-BASED TCAM IMPLEMENTATIONS

When working with FPGAs, the implementation of TCAMs may primarily be done in one of two ways. The first thing that has to be done is to build the TCAM cells and match lines by making use of the flip-flops and logic facilities provided by the FPGA. The second option is to make advantage of the block memory that is available on the FPGA.

The bits of the rules are first held by flip-flops since this is the most convenient option. As was mentioned before, there are three distinct values that may be assigned to each bit: 0, 1, and x. For instance, a flip-flop can be used to store whether a bit is 0 or 1, and a second flip-flop, which functions as a mask and is set when the bit is do not care, can be used to record the result of the first flip-operation. flop's Both flip-flops can be used together to record the result of an operation. After then, programmable circuitry may be used in order to carry out the comparison with the key. Because of the significant amount of resources that are needed for each rule, this strategy cannot be utilized to construct enormous TCAMs with tens of thousands of rules that are longer than 100 bits and that function quickly.

The second possibility involves making use of the FPGA's built-in memories, which are known as embedded memories. In order to do this, the key is segmented into more manageable chunks of b bits. After then, a rule might be reproduced by making use of a 1-bit memory that has 2b places for each block. When looking for a key, all of the memory is accessible by utilizing the bits that correspond to the key; a match is found if all of the locations read contain a one. In most cases, k rules can be implemented with the use of a memory that has k bi t locations for each block. An illustration is the most effective method for conveying this point. Consider a key that is comprised of two blocks that are each composed of three bits, bringing the total number of bits to six. Then, a TCAM consisting of four rules might be used, as seen in Figure 1. As can be seen, each memory has a width of 4 bits and a total of 23 places, which equals 8 different storage spots. The three bits at the very top of the key may be used to access the memory that is placed the furthest to the left, while the three bits at the very bottom of the key can be used to access the other memory. When reading data from memory, these bits are necessary for determining the address of the memory location being read from. Figure also demonstrates the rules that are kept in each individual bit's storage space.

1. Let's have a look at the results of a key search for the number 000011. We would go closer and closer to the commencement of the story. The address on the memory on the far left reads 1100, and the address on the memory on the far right reads 011, with the four position reading 1100. Following the AND operation, the only rules that would be satisfied are r1 and r2. When we examine the rules in more detail, we see that the rules (r4) that are not being utilized have zeros in every memory location and location. This is visible when we examine the rules more carefully. The number of ones that are available in a specific memory for the remaining rules is determined by the amount of x bits a rule has on the address bits that are used as the memory's key bits. A one is stored in the one position if there are no x bits; whenever there are one or two x bits, the two locations store a one; whenever there are three or more x bits, the four places store a one; and so on. There will typically be a total of 2n x ones on the memory if there are n x bits that have the value x.

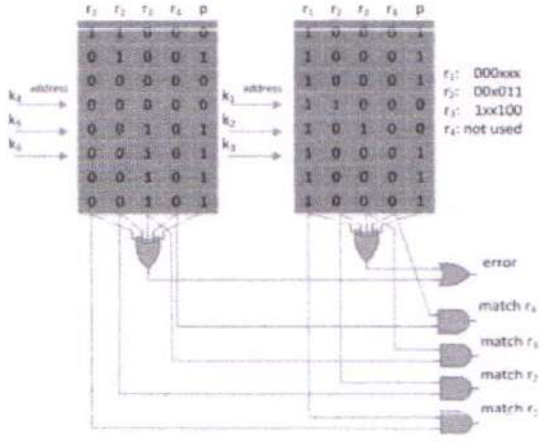


Fig.1 Parity protected TCAM with 6-bit keys and four rules emulated usingtwo SRAMs.

Now take into consideration the expenses associated with the implementation, keeping in mind that each block must have b bits of SRAM memory and includes b bits of a rule. Using this strategy will result in a cost of 2b/b for each SRAM bit required for the TCAM bit [13]. Therefore, it would seem that lower values of b are more effective. However, this is not quite accurate since the amount of mental effort required to piece together the structure grows in proportion to the number of bricks used. Be aware that a significant amount of data stored in a physical memory may be partitioned into a number of blocks, each of which may execute via different components of a rule. At that point, more memory accesses are required to complete a search operation; however, it is possible to prevent this by using multiport memories or running the memory at a quicker speed [16].

Memory resources for Xilinx FPGAs come in the form of either lookup table random access memories (LUTRAMs) or basic random access memories (BRAMs). The early ones are typically compact with 32 or 64 places and are constructed using the same lookup tables (LUTs) that are used to implement the logic. BRAMs, on the other hand, are bigger and can store up to 36 k bits. They are capable of being set up with a variety of word sizes, the greatest of which is 72 bits, which is equivalent to 512 locations. As a direct consequence of this, LUTRAMs have a cost per bit that is much lower (25/5) than BRAMs do (29/9). On the other hand,

compared to LUTRAMs, BRAMs have access to a greater number of total memory bits.

An essential finding for the safety of SRAM-based TCAM implementations is that just a few permutations of all of the potential values are utilized, and the contents of the SRAMs are decided by the rules that have been stated. This would seem to imply that the contents of the SRAM had some kind of built-in redundancy that may be used to safeguard the memories. This concept will be further explored in the next paragraphs of this short text.

An Energy-Efficient SRAM-Based TCAM on FPGA: Ternary content-addressable memory (TCAM) chooses a word from the ternary data it has saved depending on the information contained inside the word. Following completion of one cycle, the address of the matched word is obtained by carrying out a parallel comparison of the search key and each of the TCAM words that have been stored. The circuitry of a TCAM cell is responsible for storing, as well as comparing, three different states. These states are 0, 1, and the don't care state x. A priority encoder and a collection of TCAM cells make up the TCAM architecture (PE). Each TCAM cell has both a comparison circuitry and two SRAM cells, each of which may store a ternary bit. Both of these components are responsible for storing the bit. In the search technique, both search lines (also known as SLs) and match lines are used (MLs).

The SLs give the TCAM words' matching cells with search key bits in order to match them. The MLs are used to illustrate the comparison findings for each each TCAM word. If there is more than one TCAM word that successfully matches the search key, the PE will choose the address that has the greatest priority among the matching addresses. Figure 1 may depict an example 4 3 TCAM design. Native TCAM is a kind of TCAM that was built specifically for an application as an integrated circuit system (ASIC).

TCAM is used in a variety of different systems, including look-up tables in networking routers [1, 2], translations-look-aside buffers (TLB) caches in microprocessors [3, 4], database accelerators in big-data analytics [4,5], filters for storing signature patterns in the Internet of Things [6, 7], and local binary patterns recognition systems in image processing and DNA sequence matching [8, 9].

However, because of the specialized bit comparison circuitry, the memory density of the native TCAM cells is decreased. Additionally, because of the high degree of parallelism in the system, native TCAM is both costly and energy-intensive. In addition, the native TCAMs that are built into ASICs have a restricted number of configurations, which hampers their capacity to adapt to evolving market demands and prospective TCAM application trends that may emerge in the future.

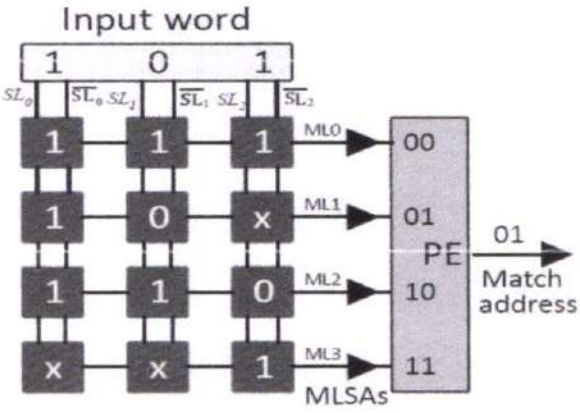


Figure 2 A 4 _ 3 TCAM: (MLSAs: Match line sense amplifiers)

The ability of modern field-programmable gate arrays, often known as FPGAs, to enable massive parallelism in addition to flexibility via on-the-fly reconfiguration makes them an appealing choice for the development of new systems. This is because tremendous progress has been made in CMOS technology, which has led to this outcome. Block RAMs, often known as BRAMs, are a prevalent kind of embedded memory that is used in contemporary SRAM-based FPGA devices such as the 16-nm Xilinx Virtex Ultra SCALE FPGA. These BRAMs can store large amounts of data. BRAMs are built utilizing silicon substrates, and they are capable of high speeds while using just a little amount of power.

Integrated memory BRAMs on current SRAM-based FPGAs are preferred due to the need for rapid, adaptable (reconfigurable), and adaptive (easy for integration) TCAM design. This is because integrated memory BRAMs are easier to integrate. SRAM is used to implement TCAM in FPGAs. This is done by addressing SRAM with the contents of TCAM and storing data for the whole of the TCAM table in SRAM. The existence as well as the address of a single TCAM pattern is stored in each word of SRAM. currently available SRAM-based

TCAMs on FPGAs have a greater energy use than other types of memories because it takes an excessive amount of power to activate all of the SRAM memory that is required for a lookup. For example, the BRAMs on the FPGA were utilized to construct 89 kb and 150 kb TCAM tables via the SRAM-based TCAM design approaches, which required a total of 2.5 Wand and 3.2 Wand, respectively. These table sizes were accomplished by employing the SRAMs. When capacity rises, the already high power consumption of SRAM-based TCAM devices becomes even more problematic.

3. SOFT ERRORS IN SRAM

The sensitivity of semiconductor devices to radiation has significantly grown as a result of the evolution of technology. SRAM arrays are often the most densely packed circuitry on a chip because they make full use of very small cells. Due to the high bit count, there is a greater chance that an ionizing particle would collide with a sensitive node in the array, therefore erasing the data that was previously stored. The lowest layout dimensions reduce the capacitance of the storage nodes and, as a result, the critical charge Qcrit that might be introduced by radiation and cause a disturbance in the SRAM cell.

The Qcrit is reduced even more as a result of the falling supply voltages. Radiation may cause data mistakes, which makes it difficult to construct dependable SRAM arrays using nano scaled technologies. These variables contribute to radiation-induced data errors. Radiation may be the major cause of localized ionization events in semiconductor devices or it may be the outcome of a secondary process. A small number of these radiation-induced events create a enough number of electron-hole pairs to cause damage to the storage nodes of SRAM cells. A "soft" mistake is what we mean when we say anything like this while we're angry. A disturbance of this magnitude might cause a data mistake, although the device structures themselves are not irreparably harmed. Though the voltage disturbance on one of an SRAM cell's storage nodes is lower than the node's noise margin, the SRAM cell will continue to function correctly and will maintain the integrity of the data it stores even if the disturbance occurred.

A "soft" mistake will occur, however, if the noise buffer of a cell is insufficient to survive the disruption induced by ionizing radiation. This might lead to a cell malfunctioning. In the late 1970s, soft errors were identified as a potential issue for dynamic random-access memories (DRAMs) that used planar storage capacitors. The charge that was stored in these capacitors was kept in two-dimensional p-n junctions that covered a huge region. Early DRAM cells were very prone to soft mistakes because of the high radiation-induced charge collection efficiency of the large planar reverse-biased connections. Technology advances and attempts to lower the high soft error rates and poor pause/refresh time ratios of DRAMs (SER) (SER)

As a result, there was an increased need for portable three-dimensional storage capacitors. Because of the decreased volume of the p/n junction, the newly developed 3D capacitors demonstrated a junction collection efficiency that was much lower than that of the older 2D planar capacitors. Despite the fact that a DRAM cell's Qcrit will decrease as a result of VDD scaling, the storage capacitor's aggressive junction volume growth will more than compensate for this loss. Because of this, the SER of a DRAM bit cell drops by about 4 times with each new generation of technical advancement.

This decrease in DRAM SER, however, is being countered by the rapidity with which the system-level DRAM bit count is growing. Because bigger DRAM arrays are statistically more prone to generate soft mistakes, the resultant DRAM SER at the system level has remained impressively consistent over numerous recent technological generations. This is despite the fact that larger DRAM arrays are statistically more likely to create soft errors. The feedback mechanism that safeguards the state of an SRAM cell allowed early SRAMs to be more resistant to the effects of soft faults than their DRAM counterparts. The critical charge of an SRAM cell is impacted in two different ways: first, by the restoring current of the pull-up or driver transistors, and second, by the capacitance of the storage node.

As a result of scaling in technology, the size of the SRAM cell and, therefore, the junction area of the storage nodes are both decreasing (Fig S1). Additionally, the capacitance of the storage node was decreased, and there is a possibility that the leakage at the cell junction was lowered. A more aggressive scaling of the VDD was the outcome of switching from constant voltage scaling to constant electric field scaling. The combined effect of these two elements is to lower the Qcrit, which in turn leads to an increase in the likelihood of soft mistakes, which in turn leads to a rise in SER levels. With each new generation of technology, decreases in cell collecting efficiency brought on by decreases in cell depletion volume were compensated for by improvements in storage node and VDD capacitance. These changes occurred with each new generation of technology.

4. ERROR DETECTION AND CORRECTION INSRAM – BASED TCAMS

The emulated TCAM memory is equipped with a protection system that employs a per-word parity bit in order to identify instances of single-bit mistakes. When an error is found, an attempt is made to fix it by using the built-in redundancy of the memory contents. This is done in the event that the fault cannot be corrected. Figure 2 depicts the implementation of the parity protection, where the letter p stands for the parity bit. It is abundantly clear that in addition to the match signal, an error signal is also produced if there is a discrepancy between the parity that has been saved and the one that has been recomputed. This parity check is the industry standard, and it can detect any and all single-bit

defects [5]. Error detection on each and every access is very necessary in order to avoid producing inaccurate search results.

Let's suppose for the time being that a specific word had a single-bit mistake and that the parity check was able to find it. In the event that a mistake is discovered, we can investigate the matter by looking at the information stored in the memory. A good place to start would be to read every word in the memory and make a note of the number of times each rule occurs in a single area. This would be a nice place to begin. Make use of that number to indicate the significance of the rule associated with that memory. Taking Fig. 2's leftmost memory as an example, r1 would have a weight of 1, r2 would have a weight of 2, and r3 would have a weight of 4. It's possible that this will assist us in locating the incorrect bit, given that the weight of an error-free rule for an 8-position memory can only be 0, 1, 2, 4, or 8. Let's concentrate on the cases of single-bit mistake shown in Fig. 3 so that we can have a more in-depth conversation about the process of error repair. For example, e3 reduces the weight of r3 in the leftmost memory from 4 to 3, making no other modifications. After finding the parity mistake, we would determine that the bit in register 3 (r3) is the one that is incorrect, and then we would correct it since 3 is not a legal value. It is possible that using this method will be beneficial for rules which either have weights greater than two or have two or more "x" bits on the key bits relating to the memory in question. On the other hand, when it comes to regulations that have a smaller weight, it's possible that examining the weight alone won't be sufficient. Now, let's think about a rule that has a weight of two. After then, there will be a blunder that causes a 0 to be changed into a 1.

In order to rectify the situation, the value of the weight is going to be raised to three. It is impossible to repair the mistake when a one is converted to a zero (as in e2) since the new weight would then be a legal integer. This occurs when the error occurs in the calculation for e2. However, the fact that there are only two spots with a one makes the occurrence of this event less probable. If we are going to take the guideline for weight one as our standard, then an error that changes another bit to one will result in a weight of two, which is likewise acceptable. However, not every possible combination of weights two can be implemented. When looking at e4, this is really obvious to see. In this scenario, the key values 000 and 011 would be similar to r2 values of one, which are not equivalent to a legitimate rule. r2 values of one are not equivalent to a valid rule. Most of the time, the search will not be successful until the place in question matches a key value that is one step removed from the initial value. On the other hand, a mistake that resets a weight one rule's position from one to zero may be remedied by confirming that the rule has zero weight on the other memory. This corrects the error that caused the position to be reset.

In this scenario, the rule would be deactivated, and there would be no indication that the bit was incorrect. If this was not the case, the mistake was fixed, and the weight of the rule was increased to 1. Last but not least, an inaccuracy in a rule with a weight of 0 may also be rectified by evaluating the impact of the rule on the other memories in order to determine its relative importance.

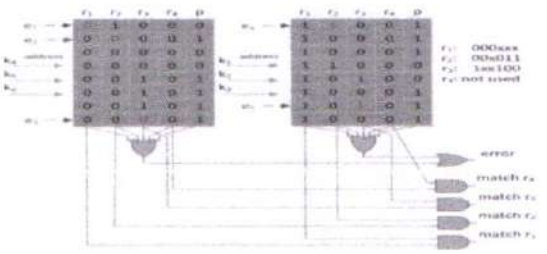


Fig.3. Examples of single-bit errors on a parity protected TCAM with 6-bit keys and four rules emulated using two SRAMs.

The section that came before it demonstrated how several single-bit error patterns may be resolved by making advantage of the redundancy that was already built into the memory contents. Now that we have it figured out, let's calculate out how many single-bit error patterns there are in a memory that has 2b places that can be repaired for each weight.

1. There is no weight; errors in patterns may be corrected.

2. Weight one: Everyone, with the exception of those who set a bit to one for a place that has an address at a distance of one; the sum of these two values is equal to 1 b/2b.

3. The second weight entails that all patterns, with the exception of the two that set a position with a one to a zero, are able to have their values altered. This is the same as 12 divided by 2b.

All patterns may be corrected up to and including level four when using weights four and above.

The vast majority of the erroneous patterns have been, without a doubt, fixed. This idea is made more understandable by referring to Table I, which provides an overview of the proportion of designs that may be modified to accommodate columns with varying weights. The only circumstances in which all mistakes cannot be rectified are those involving weights one and two; in such circumstances, the percentage will be extremely close to 100% when b is big. The only other circumstance is when all faults occur in weights three and four. Table II presents, for each of many possible values of b, the proportion of mistakes that are amenable to correction. Even

ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

with a relatively little amount of memory (b = 5, which equates to 32 locations), the error coverage is rather near to 90%, even in the worst case scenario, as can be shown. The coverage for bigger memories is more than 95% and comes very close to reaching 100%. As an example, the coverage for b = 9 is more than 98% even in the most dire of circumstances. This demonstrates how successful the suggested method is at repairing single-bit mistakes in situations where the parity bit is used to ensure security for the memory.

5. SYNTHESIS AND IMPLEMENTATION OF THE DESIGN

Before the design can be implemented on the prototype board or checked for accuracy using functional simulation, it must first be synthesized and implemented. This may be done at any time throughout the design process. While the top-level VHDL file is accessed (by double-clicking that file in the HDL editor window on the right section of the Project Navigator), the implement design option may become accessible in the process view of the project. This occurs when the project view is in the Module view. In addition, the process view displays the available choices for the Generate Programming File and Design Entry utilities. In the event that there are any user limitations, they might be dealt under the former, while the latter will be considered in a later section.

Double-clicking the option in the Processes box that is titled "Synthesize Design" will cause you to synthesize the design. To get started, double-click the "Implement design" option that is located in the Processes box. There are several steps involved, including Translate, Map, Place & Route, and others. Any of these stages that were either impossible to finish or were done in an unacceptable manner will have a cross superimposed over them. In such case, a check mark will be added after each activity to show that it was completed without any problems. If everything goes according to plan, there will be a check mark shown next to the choice to Implement Design. In the event that there are any cautions, a checkmark will appear in front of the option to indicate whether or not there are any warnings. The Console window, which may be seen at the bottom of the Navigator window, displays any warnings or problems that may have occurred. Because each of these markers is deleted every time the design file is saved, you will need to start the compilation process from scratch.

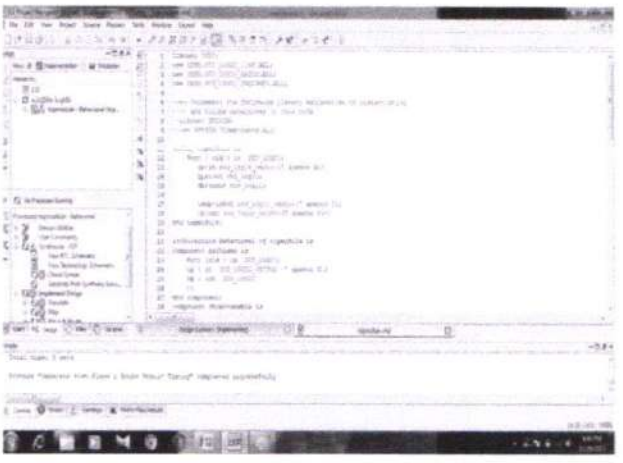


FIG.4 Implementing the Design (snapshot from Xilinx ISE software)

The schematic representation of the synthesized VHDL code may be examined in the Process Window by selecting Synthesize-XST from the menu and then selecting View RTL Schematic by clicking it twice. This is a useful way for troubleshooting the code and would be beneficial in the event that the output on the prototype board did not meet our needs.

When you double click, the top-level module will open, and all it will show you are the module's inputs and outputs, as seen below.

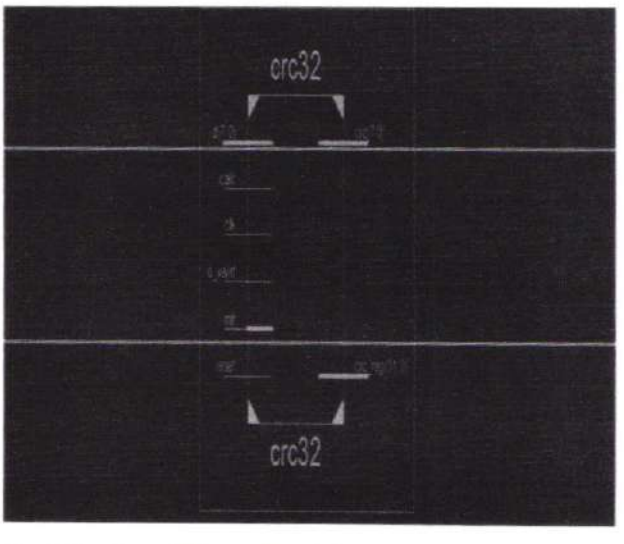


Fig 5 Top Level Hierarchy of the design

When you double click on the rectangle, the underlying logic that has been established is revealed, as demonstrated in the following example. XilinxISE's implementation of the logic included in the VHDL code The ETI simulation has been finished successfully with the help of the model Xilinx simulator.

A. Simulation and synthesis has been carried out with XILINXISE:

Before the design can be implemented on the prototype board or checked for accuracy using functional simulation, it must first be synthesized and implemented. This may be done at any time throughout the design process. The implement design option becomes accessible in the process view when the top-level VHDL file is opened (by double-clicking that file in the HDLeditor window located on the right side of the Project Navigator) and the project is shown in the Module view.

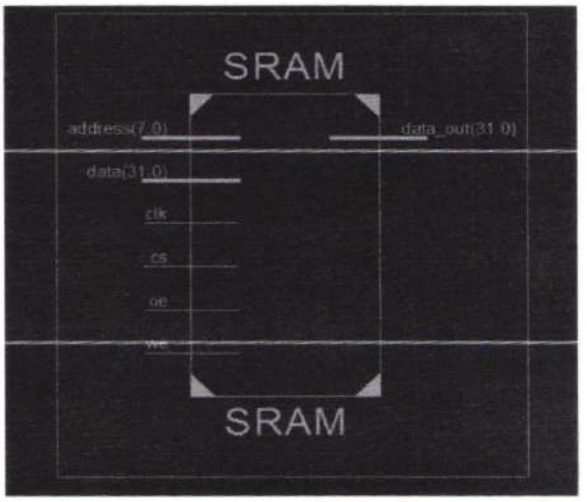
In addition, the process view displays the available choices for the Generate Programming File and Design Entry utilities. In the event that there are any user limitations, they might be dealt under the former, while the latter will be considered in a later section. Double-clicking the option in the Processes box that is titled "Synthesize Design" will cause you to synthesize the design. In order to put the plan into action.

To implement the design, double-click the corresponding option in the Processes pane. There are several steps involved, including Translate, Map, Place & Route, and others. Any of these stages that were either impossible to finish or were done in an unacceptable manner will have a cross superimposed over them. In such case, a check mark will be added after each activity to show that it was completed without any problems. If everything goes according to plan, there will be a check mark shown next to the choice to Implement Design.

One may be able to see the warnings, if there are any! Put a checkmark in front of the choice to let consumers know that there are certain precautions they should take. The Console window, which may be seen at the bottom of the Navigator window, displays any warnings or problems that may have occurred. When the file containing the design is saved, each of these markers is removed, which means that a new compilation will need to be done.

If you double click the View RTL Schematic option in the Synthesize-XST menu in the Process Window, you will be able to view the schematic diagram that corresponds to the VHDL code that was synthesized. If the output on the prototype board did not match our standards, then this would be a helpful approach for debugging the code.

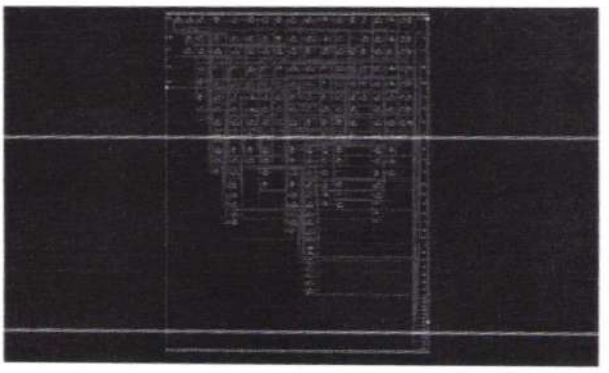
Simply clicking the plus symbol that is located next to the Modelsim simulator Tab in the Processes window will allow you to make it larger (while making sure the test bench file in the Sources window is chosen). You need to click the Simulate Behavioral Model button a total of two times. There is a good chance that you may run across a compiler error. When asked whether you want to quit the simulation, choose "NO" from the drop-down menu. There is nothing to be afraid of in this situation. As a direct result of this, ModelSim ought to begin running. Continue to watch it until it stops moving.

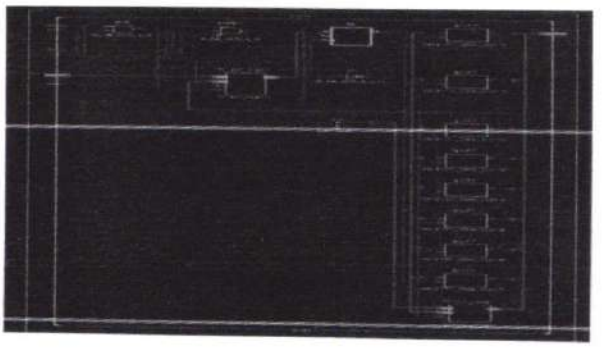


B. Technology schematic of crc Block replaced by XOR gate in ETI architecture

6. EXPERIMENTAL RESULTS

RTL





CONCLUSION

In this paper, a method is proposed for securing the SRAMs that are present on FPGAs and serve the purpose of simulating TCAMs. The technique is founded on the discovery that while not all values may be obtained in those SRAMs, there are certain degrees of duplication in the memory contents. This observation is the foundation for the method. When the memory is secured with a parity bit to detect faults, this redundancy is employed to rectify the majority of single-bit error patterns so that the memory can function properly. Because the suggested method reduces the amount of resources required to safeguard memory by a large margin, it is an attractive choice for implementation in systems in which dependability is essential but resources are in short supply.

This condensed description of the underlying idea may be used for a variety of memory architectures. For example, by routinely evaluating the accuracy of an unprotected memory, it might be used to locate problems in the memory and determine how to fix them. It is possible to utilize it to rectify numerous bit mistakes in the memory when it is protected by a more robust code that is able to notice a string of faults in succession. For instance, double-bit error patterns for a memory that is guarded by an SEC code may be identified and corrected by the use of the built-in redundancy of the memory's contents.

REFERENCES

1. N. Kanekawa, E. H. Ibe, T. Suga, and Y. Uematsu, Dependability in Electronic Systems: Mitigation of Hardware Failures, Soft Errors, and Electro-Magnetic Disturbances. New York, NY, USA: Springer-Verlag, 2010.

2. J. L. Autran et al., "Soft-errors induced by terrestrial neutrons and natural alpha-particle emitters in advanced memory circuits at ground level," Microelectron. Rel., vol. 50, no. 9, pp. 1822–1831, Sep. 2010.

3. L. Silburt, A. Evans, I. Perryman, S. J. Wen, and D. Alexandrescu, "Design for soft error resiliency in Internet core routers," IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3551–3555, Dec. 2009.

4. Evans, S.-J. Wen, and M. Nicolaidis, "Case study of SEU effects in a network processor," in Proc. IEEE Workshop Silicon Errors Logic-Syst. Effects (SELSE), Mar. 2012, pp. 1–7.

5. L. Chen and M. Y. Hsiao, "Error-correcting codes for semiconductor memory applications: A state-of-the-art review," IBM J. Res. Develop., vol. 28, no. 2, pp. 124–134, Mar. 1984.

6. K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey," IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.

7. F. Yu, R. H. Katz, and T. V. Lakshman, "Efficient multimatch packet classification and lookup withTCAM," IEEE Micro, vol. 25, no. 1, pp. 50–59, Jan./Feb. 2005.

8. P. Bosshart et al., "Forwarding metamorphosis: Fast programmable match-action processing in hardware for SDN," in Proc. ACM SIGCOMM, 2013, pp. 99–110.

9. Syafalni, T. Sasao, and X. Wen, "A method to detect bit flips in a soft-error resilient TCAM," IEEETrans. Comput.-Aided Design Integr. Circuits Syst., vol. 37, no. 6, pp. 1185–1196, Jun. 2018.

10. S. Pontarelli, M. Ottavi, A. Evans, and S. Wen, "Error detection in ternary CAMs using Bloom filters,"in Proc. Design, Automat. Test Eur. Conf. Exhib. (DATE), Mar. 2013, pp. 1474–1479.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Implementation Of Turbo Decoder For Completing Communication System In IVS

CH. Baby Shalini
MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: babyshalini.chanchala99@gmail.com

Dr.S. Kishore Reddy
Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

Abstract- **The most popular communications encoding algorithm, the iterative decodin requires an exponential increase in hardware project focuses on the Keywords- encoding, decoder trellis o technique.The turbo codes are designed with the help of Recursive Systematic Convolutional and are separated by inter leaver, which (component used to rearrange the bit sequence) plays a vital role in the encoding process. This the design paper provides of a Turbo E**

Keywords- **Turbo E, decoding, Recursive Systematic**

I. INTRODUCTION

Error could be a condition once the output information doesn't match with the input information. Throughout transmission, digital signals suffer from noise which will introduce errors within the binary bits movement from one system to another. That means a 0 bit might change to 1 or a 1 bit might change to 0. a codes which are additional data added to a given digital message to help us detect if an error occurred throughout transmission of the m A are able to pass some data tsy way to detect errors along with a sophisticated mechanism to work out the corrupt bit location. tozero) to urge the original message. To detect and correct the errors, extra bits are super imposed to the data bits at the time of transmission. The extra bits are referred to as parity bits . They permit detection or correction of the errors. The data bits in conjunction with the parity bits form a code word. Parity checking is employed detection. It is the best technique for detecting and c for parity and the remaining 7 bits are employed as data or message bits. The parity of 8-bits transmitted word is either even parity or odd parity. Even parity suggests that the amount of 1's within the given word as well as the parity bit should be even (2, 4, 6 ...). Odd parity means the number of 1's in the given word including the parity bit should be odd (1, 3, 5 ...). The parity bit is set to zero and one depending on the type of the parity needed [10]. For even parity, this bit is set to one or zero such that the no. of "1 bits" in the entire word is even. For odd parity, this bit is set to one or zero such that the no. of "1 bits" in the entire word is odd.

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

II. TURBOS CODES

The theory of error correcting codes has presented a large number of code constructions with corresponding decoding algorithms. However, for applications where very strong error correcting capabilities are required these constructions all result in far too complex decoder solutions. The way to combat this is to use concatenated coding, where two (or more) constituent codes are used after each other or in parallel - usually with some kind of interleaving. The constituent codes are decoded with their respective decoders, but the final decoded result is usually sub-optimal. This means that better results might be achieved with a more complicated decoding algorithm - like the brute-force trying of all possible codewords. However, concatenated coding offers a nice trade of between error correcting capabilities and decoder complexity. Concatenated coding is illustrated in Figure 1. Here we see the information frame illustrated as a square - assuming block interleaving - and we see the parity from the vertical encoding and the parity from the horizontal encoding. For serial concatenation the parity bits from one of the constituent codes are encoded with the second code and we have parity of parity. If the codes are working in parallel, we do not have this additional parity. The idea of concatenated coding fits well with Shannon's channel coding theorem, stating that as long as we stay on the right side of the channel capacity we can correct everything - if the code is long enough. This also means that if the code is very long, it does not have to be optimal. The length in itself gives good error correcting capabilities, and concatenated coding is just a way of constructing - and especially decoding - very long codes

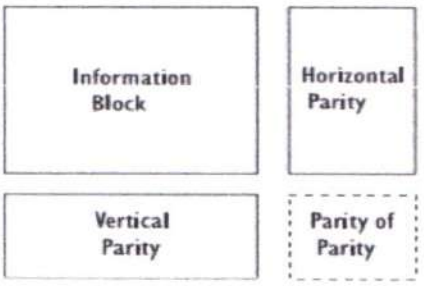


Figure 1 Concatenated coding

A generic Turbo encoder (Barbulescu et al 1999) has been shown in BELOW Figure. The input sequence of the information bits is organized in blocks of length N. The first block of data will be encoded by the Recursive Systematic Convolutional codes RSC ENCODER1 block, which is recursive systematic encoder. The same block of information bits is interleaved by the interleaver, and encoded by RSC ENCODER2, which is also systematic recursive encoder. The code word is framed by concatenating out put codc words Xk, Y1k, and Y2k

Due to similarities with product codes (OrhanGazi and Ali Ozgur Yilmaz 2006), it can be called the RSC ENCODER1 block as the encoder in the horizontal dimension and the RSC ENCODER2 block as the encoder in the vertical dimension. The interleaver block, rearranges the order of the information bits of input to the second encoder. The main purpose of the Interleaver (Sadjadpour et al 2000) is to increase the minimum distance of the Turbo code such that after correction in one dimension the remaining errors should become correctable error patterns in the second dimension. Ignoring for the moment the delay for each block, we assume both encoders output data simultaneously. This is rate 1/3 Turbo code, the output of the Turbo encoder being the triplet (Xk, Y1k, and Y2k). This triplet is then

modulated for transmission across the communication channel, which is Additive White Gaussian Noise channel. Since the code is systematic, Xk is the input data at time k. Y1k, and Y2k are the two parity bits at time k. The two encoders do not have to be identical.

The basic idea of turbo codes is to use two convolutional codes in parallel with some kind of interleaving in between. Convolutional codes can be used to encode a continuous stream of data, but in this case we assume that data is configured in finite blocks - corresponding to the interleaver size. The frames can be terminated - i.e. the encoders are forced to a known state after the information block. The termination tail is then appended to the encoded information and used in the decoder. The system is illustrated in below Figure .

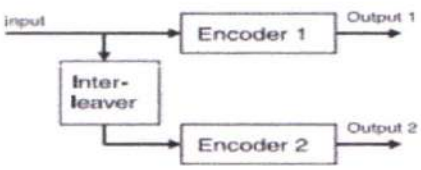


Figure 2 turbo encoder

We can regard the turbo code as a large block code. The performance depends on the weight distribution - not only the minimum distance but the number of words with low weight. Therefore, we want input patterns giving low weight words from the first encoder to be interleaved to patterns giving words with high weight for the second encoder. Convolutional codes have usually been encoded in their feed-forward form, like (G1,G2)=(1+D ,1+D+D). However, for these codes a single 1, i.e. the sequence 2 2 ...0001000..., will give a codeword which is exactly the generator vectors and the weight of this codeword will in general be very low. It is clear that a single 1 will propagate through any interleaver as a single 1, so the conclusion is that if we use the codes in the feed-forward form in the turbo scheme the resulting code will have a large number of codewords with very low weight. The trick is to use the codes in their recursive systematic form where we divide with one of the generator vectors. Our example gives (1,G2/G1)=(1,(1+D+D /(1+D)). This operation 2) 2 does not change the set of encoded sequences, but the mapping of input sequences to out-put sequences is different. We say that the code is the same, meaning that the distance properties are unchanged, but the encoding is different. In Figure 3 we have shown an encoder on the recursive systematic form. The output sequence we got from the feed-forward encoder with a single 1 is now obtained with the input 1+D =G1. More important is the fact that a single 1 gives a codeword of semi-infinite 2 weight, so with the recursive systematic encoders we may have a chance to find an interleaver where information patterns giving low weight words from the first encoder are interleaved to patterns giving words with high weight from the second encoder. The most critical input patterns are now patterns of weight 2.

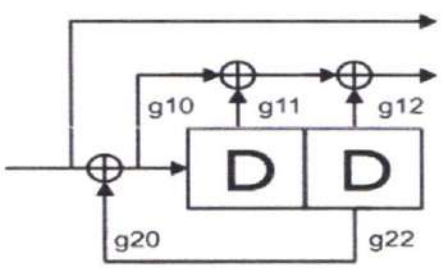


Figure 3 Recursive systematic encoder

For the example code the information sequence ...01010... will give an output of weight 5. Notice that the fact that the codes are systematic is just a coincidence, although it turns out to be very

convenient for several reasons. One of these is that the bit error rate (BER) after decoding of a systematic code can not exceed the BER on the channel. Imagine that the received parity symbols were completely random, then the decoder would of course stick to the received version of the information. If the parity symbols at least make some sense we would gain information on the average and the BER after decoding will be below the BER on the channel. One thing is important concerning the systematic property, though. If we transmit the systematic part from both encoders, this would just be a repetition, and we know that we can construct better codes than repetition codes. The information part should only be transmitted from one of the constituent codes, so if we use constituent codes with rate 1/2 the final rate of the turbo code becomes 1/3. If more redundancy is needed, we must select constituent codes with lower rates. Likewise we can use puncturing after the constituent encoders to increase the rate of the turbo codes. Now comes the question of the interleaving. A first choice would be a simple block interleaver, i.e. to write by row and read by column. However, two input words of low 6 . . . . . 0 0 0 0 0 . . . . . 0 1 0 1 0 . . . . . 0 0 0 0 0 . . . . . 0 1 0 1 0 . . . . . 0 0 0 0 0 . . . . . Figure 4 Critical pattern in block interleaver weight would give some very unfortunate patterns in this interleaver. The pattern is shown in Figure 4 for our example code. We see that this is exactly two times the critical twoinput word for the horizontal encoder and two times the critical two-input pattern for the vertical encoder as well. The result is a code word of low weight (16 for the example code) - not the lowest possible, but since the pattern appears at every position in the interleaver we would have a large number of these words.

Turbo Encoder is a parallel concatenation of Two Recursive Systematic Convolutional (RSC) Encoders and is separated by interleaver. RSC Encoders generates twodifferent codes one is systematic output and the second one is parity bits. But each RSC encoders takes different bit stream as an input. The first one will take original data as input and second will take interleaved data as input. Interleaving is a process in which bits are rearranged by using the desired algorithm. The Turbo Encoder gives output of 28 bits which is a combination of input data and an output of two RSC encoders which is thrice the length of the input bits as it shown in below Fig

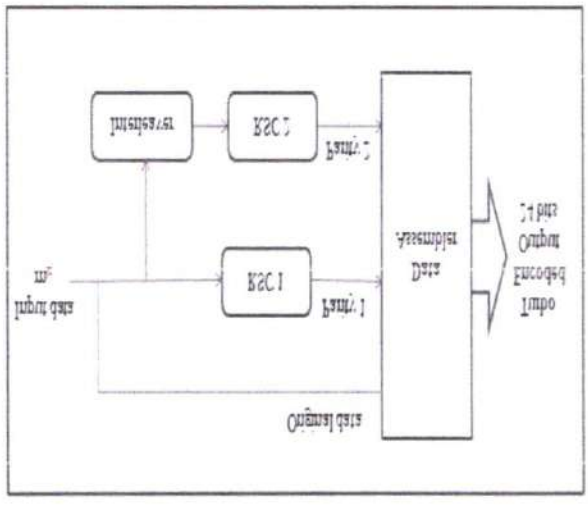
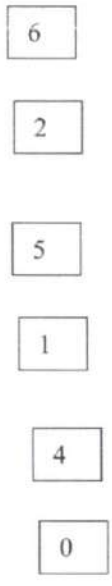


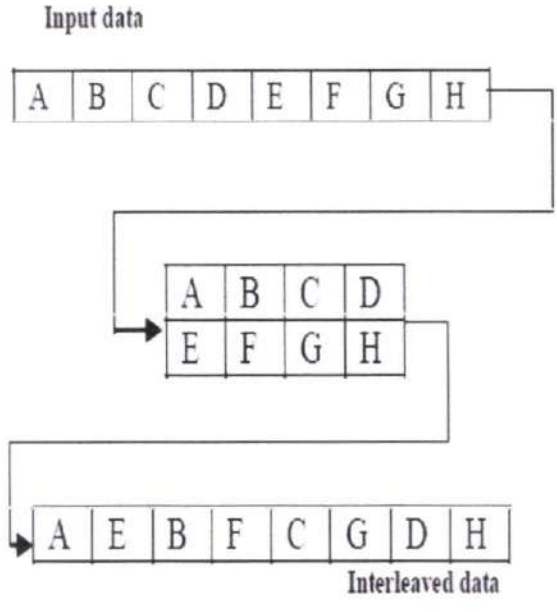
Figure 4 Turbo Encoder Block Diagram

III. INTERLEAVER

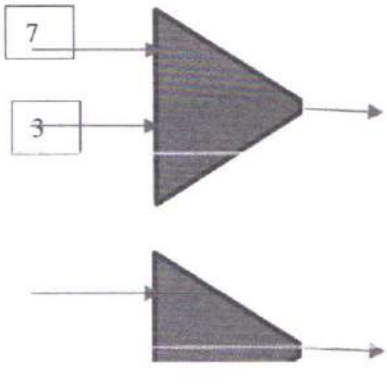
The interleaver design (Khandani 1998) is a key factor, which determines the good performance of a Turbo code. Shannon (1948, 1949) showed that large

block-length random codes achieve channel capacity. The 23 pseudo-random interleaver makes the code appear random. In this work the pseudo Random Interleaver has been used. Block interleaver or Matrix interleaver is a most popular interleaver used in digital data transmission that is illustrated in Fig 6. When compared with the other interleavers, it is very simple and easy to design and implement. A block interleaver writes data in a matrix row wise from left to right and top to bottom. After all the information bits are writing into a matrix. it reads the data in column wise from top to bottom and left to right. The output of the interleaver is applied to the RSC 2.





A. Modified Interleaver Dsign:

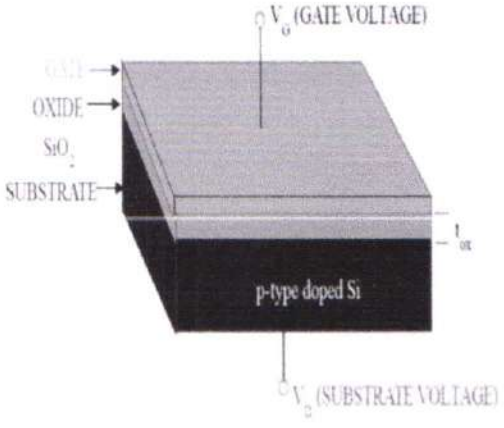


B. Basic Vlsi Design

Complementary MOSFET (CMOS) technology is widely used today to form circuits in numerous and varied applications. Today's computers, CPUs and cell phones make use of CMOS due to several key advantages. CMOS offers low power dissipation, relatively high speed, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed)

For the processes we will discuss, the type of transistor available is the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). These transistors are formed **as a 'sandwich'**consisting of a semiconductor layer, usually a slice, or wafer, from a single crystal of silicon; a layer of silicon dioxide (the oxide) and a layer of metal.

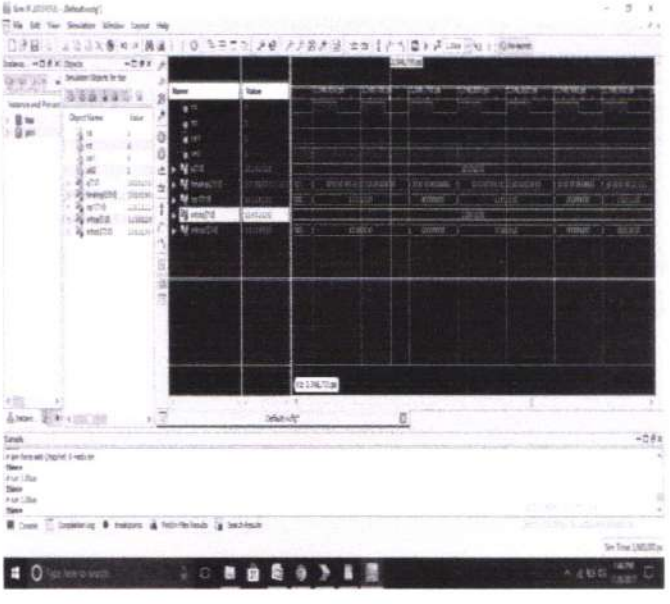
C. *Structure of a MOSFET*



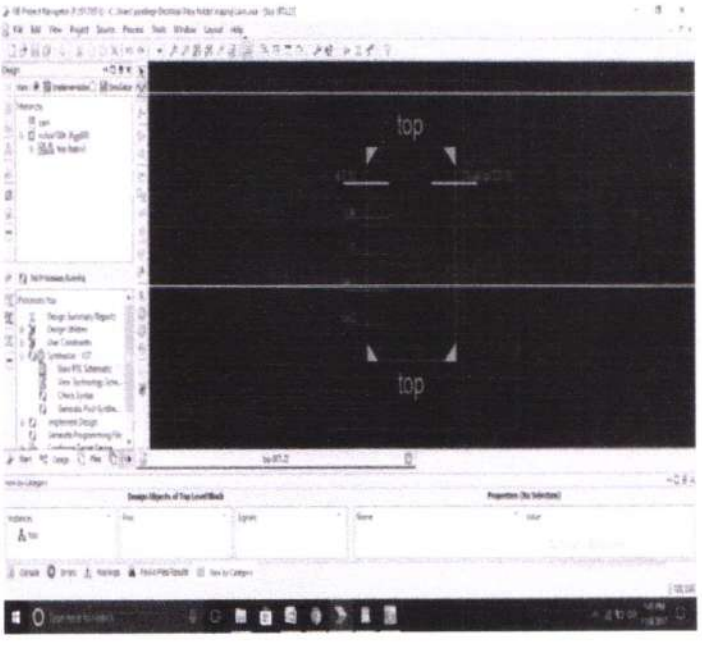
As shown in the figure, MOS structure contains three layers –

- The Metal Gate Electrode
- The Insulating Oxide Layer (SiO_2)
- P – type Semiconductor (Substrate)

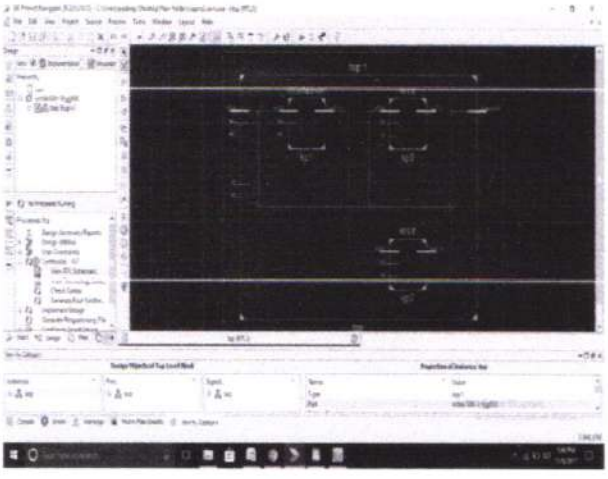
MOS structure forms a capacitor, with gate and substrate are as two plates and oxide layer as the dielectric material. The thickness of dielectric material (SiO_2) is usually between 10 nm and 50 nm. Carrier concentration and distribution within the substrate can be manipulated by external voltage applied to gate and substrate terminal. Now, to understand the structure of MOS, first consider the basic electric properties of P – Type semiconductor substrate.



A. *RTL*



IV. SIMULATION RESULT



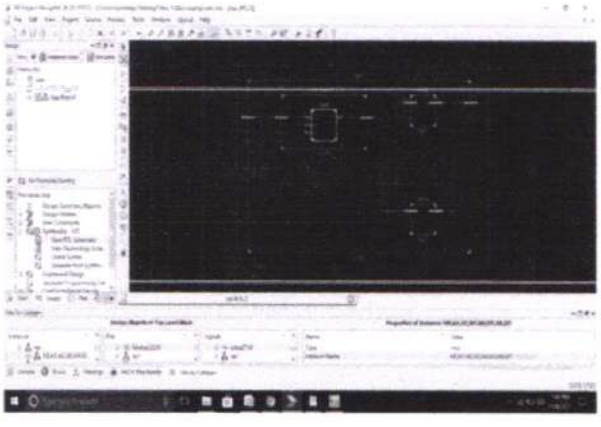


Figure 5 Modified interleaver block

V. CONCLUSION

The Turbo Encoder is designed using Verilog-HDL and simulated using Xilinx ISE 14.7, by considering 8-bit input stream and 16-bit input stream. It is observed through the simulation results that the Turbo Encoder with 8-bit input is more efficient when compare with existing methodologies. These parameters can have negative effects when very low BERs are simulated. Another cause for the limitation in BER performance is a poor interleaver design. Due to highly correlated sequences, the BER decreases to a certain level from the decoding process. SO, interleaver is designed in efficient manner.

REFERENCES

[1] Jakob Dahl Andersen, "Turbo Codes Extended with Outer BCH Code", Electronics Letters, vol. 32 No. 22, Oct. 1996.

[2] J. Dahl Andersen and V. V. Zyablov, "Interleaver Design for Turbo Coding", Proc. Int. Symposium on Turbo Codes, Brest, Sept. 1997.

[3] Jakob Dahl Andersen, "Selection of Component Codes for Turbo Coding based on Convergence Properties", Annales des Telecommunication, Special issue on iterated decoding, June 1999.

[4] L. R. Bahl, J. Cocke, F. Jelinek and R. Raviv, " Optimal Decoding of Linear Codes for Minimizing Symbol Error Rate," IEEE Trans. Inform. Theory, vol IT- 20, pp 284-287, March 1974.

[5] S. Benedetto and G. Montorsi, "Performance Evaluation of Turbo-codes", Electronics Letters, vol. 31, No. 3, Feb. 1995.

[6] S. Benedetto and G. Montorsi, "Serial Concatenation of Block And Convolutional Codes", Electronics Letters, Vol. 32, No. 10, May 1996.

[7] C. Berrou, A. Glavieux and P. Thitimajshima, "Near Shannon Limit Error-correcting Coding and

Decoding : Turbo-codes(1)", Proc. ICC 93, pp. 1064-1070, May 1993.

[8] C. Berrou and A. Glavieux, "Near Optimum Error Correcting Coding and Decoding: Turbo Codes", IEEE trans. on Communications, Vol. 44, No. 10, Oct. 1996.

[9] R. J. McEliece, E. R. Rodemich and J.-F. Cheng, "The Turbo Decision Algorithm", Presented at the 33rd Allerton Conference on Communication, Control and Computing, Oct. 1995. 21

[10] L. C. Perez, J. Seghers and D. J. Costello, Jr, "A Distance Spectrum Interpretation of Turbo Codes", IEEE Trans. on Inform. Theory, Vol. 42, No. 6, Nov. 1996.

[11] Steven S. Pietrobon, "Implementation and Performance of a Serial MAP Decoder for use in an Iterative Turbo Decoder", Proc. Int. Symposium on Information Theory, Whistler, Canada, Sept. 1995.

International Journal of Engineering Innovations in Advanced Technology
ISSN: 2582-1431 (Online), Volume-4 Issue-4, December 2022

Improvement Of Memory Data Corrections By Using CRC Technique For Fault Torrent Applications

Kethan Tingilkar

MTech Student, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kethan1510@gmail.com

Dr.S. Kishore Reddy
Associate professor, HOD, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: kishorereddy416@gmail.com

B Dasharadha
Assistant professor, Department Of ECE, VLSI System Design, Avanthi Institute of Engg. & Tech., India.
Email: banothudasharadha@gmail.com

Abstract- **A Bose-Chaudhuri-Hocquenghem (BCH) code decoder with high decoding efficiency and low power for error correction in developing memories is provided in this research as DEC-TED, or double-error-correcting and triple error-detecting. We suggest an adaptive error correction method for the DEC-TED BCH code to improve decoding efficiency. This method counts the number of mistakes in a codeword right after syndrome creation and uses a different error correction algorithm based on the error conditions the syndrome vectors in the error-finding block in order to further reduce the power consumption. The suggested decoders for the (79, 64, 6) BCH code achieve more than 70% power reduction compared to the standard fully parallel decoder under the 104-102 raw bit-error rate, according to synthesis findings with an industry-compatible 65-nm technology library.**

Index Terms- **DEC-TED, BCH code, synthesis, decoding**

I. INTRODUCTION

Digital networks and storage devices typically utilize error-detection codes known as cyclic redundancy checks (CRCs). Short check values are applied to data blocks entering these systems, depending on the remainder of polynomial division of the contents. It is possible to take remedial action against data corruption if the check values do not match after retrieval. A cyclic code is used to generate the check (data verification) value, which gives CRCs their name since it doubles the message's size without adding any new information. Popularity of CRCs is due to the fact that they are simple to build in binary hardware and straightforward to evaluate mathematically, and they are especially excellent at identifying typical mistakes caused by transmission channel noise. Using a function to create the check value is common since it has a defined length. When W. Wesley Peterson first came up with the CRC in 1961, the 32-bit CRC function of Ethernet and many other standards was developed and released in 1975 by a group of researchers from across the world.

Manuscript received Oct 10, 2022; Revised Oct 25, 2022; Accepted Nov 4, 2022

II. CRC AND ITS WORKING

the theory of cyclic error-correcting codes underpins CRCs. In 1961, W. Wesley Peterson suggested the

use of systematic cyclic codes, which encrypt messages by adding a fixed-length check value, for error detection in communication networks.[1] Although cyclic codes are easy to design, they are especially well-suited for detecting burst mistakes,

which are continuous sequences of incorrect data symbols in messages. Cyclic codes offer both of these advantages. These mistakes are widespread in many communication channels, such as magnetic and optical storage systems, thus it's critical to prevent them. A single error burst of length n bits or less will be detected by an n-bit CRC applied to a data block of any length, and a percentage of all larger error bursts will be detected by an n-bit CRC.

The so-called generator polynomial must be defined in order to provide a CRC code. If we divide the message by this polynomial, we get the quotient, which is then multiplied by this polynomial to get the remainder. To be clear, because a finite field is used to generate the polynomial coefficients, the addition may always be done bitwise-parallel (there is no carry between digits). The generator polynomial's length is never more than the length of the remainder. GF is a Galois field with two elements, and it is utilised in almost all standard CRCs nowadays (2). 0 and 1 are often referred to as the two elements, which is a good fit for computer architecture.

An n-bit CRC is one that has a check value of n bits. It is feasible to have many CRCs with different polynomials for the same n. The greatest degree n of this polynomial is 1, indicating that it has n + 1 terms. That is to say, the polynomial has a length of n + 1 and needs n + 1 bits for encoding. Because the MSB and MSB are always one, most polynomial specifications either omit the MSB or MSB. As shown in the table below, the CRC and its related polynomial often have a name of the form CRC-n-XXX Using the generator polynomial x + 1 (two terms) and the label CRC-1, the parity bit is in reality a straightforward 1-bit CRC.

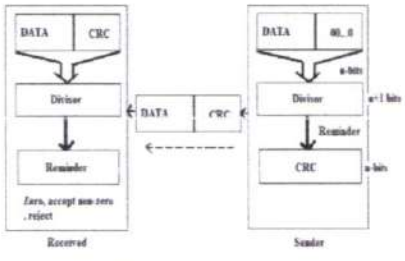


Figure 1 Operation of CRC performed at sender and receiver Side.

Using cyclic redundancy check is a standard way for dealing with data mistakes in data transmission and other domains such as data storage, data compression. A common approach to real-time CRC calculation is to use the serial data-handling devices known as linear feedback shift registers (LFSRs). Serial CRC code computation, on the other hand, has a low throughput. Using concurrent CRC calculations, on the other hand, may considerably boost the computational throughput. However, the 32-bit parallel computation of CRC-32 may accomplish many gigabits per second, but this is not adequate for high-speed applications like Ethernet networks, for example. For example, CRC-CCITT in the X-25 protocol, disc storage, SDLC, and XMODEM all employ CRC-CCITT variants to identify errors in their data transmissions; this might be an alternative solution to the problem at hand. The theory of cyclic error-correcting codes underpins CRCs. To help identify errors in communication networks, W. Wesley Peterson originally advocated the use of systematic cyclic codes, which encrypt messages by adding a fixed-length check value. Binary polynomial division is used to generate a CRC (Cyclic Redundancy Check), a widely used error-detection code. The sender treats binary data as a binary polynomial and divides the polynomial by a standard generator to obtain a CRC (e.g., CRC-32). The remainder of this division is used as the data's CRC, which is then sent together with the original data to the recipient. The receiver executes modulo-2 division on the received data and the same generating polynomial after receiving the data and the CRC checksum. Even if the original data is long, the CRC method only adds 32 bits (in the case of CRC-32) to the message, and it performs well in detecting a single mistake as well as a burst of errors.

A. Design of polynomials

The generator polynomial is the most critical aspect of the CRC method implementation. Polynomials must be selected to optimise error detection while reducing total collision probability.

Polynomial length is critical because it directly affects the length of the calculated check value (i.e., the greatest degree (exponent) +1 of any one term in a polynomial).

• 9 bits (CRC-8); • 17 bits (CRC-16); • 33 bits (CRC-32); • 65 bits are the most widely utilised polynomial lengths (CRC-64)

When the check value of a CRC is n-bits, it is known as an n-bit CRC. It is feasible to have many CRCs with different polynomials for the same n. If the polynomial has the greatest number of terms (n+1),

then it has the greatest number of terms (n+1). n is the length of the remainder. To remember its value, the CRC uses a number formatted as CRC-n-XXX.

As a result of these factors, the CRC polynomial's design is determined by its maximum total length, the intended error prevention features, the kind of resources needed to implement it, and its performance requirements. Irreducible polynomials and irreducible polynomials are two frequent misconceptions about CRC polynomials.

All faults affecting an odd number of bits may be detected by multiplying the polynomial by the quantity 1 + x. A polynomial that incorporates all of the aforementioned criteria is more likely to be a reducible polynomial. However, the quotient ring has zero divisors, therefore picking a reducible polynomial will result in a certain percentage of missed mistakes.

Using a primitive polynomial to generate a CRC code has the advantage of providing the maximum possible total block length because all 1-bit errors within that block length have different remainders (also referred to as syndromes), and because the remainder is a linear function of the block, the code can detect all 2-bit errors within that block length. A primitive generator polynomial of degree r may have a maximum block length of 2r-1, and the corresponding code can identify any single-bit or double-bit faults. [6] This condition can be improved. Code that can detect single, double, triple, or odd number of mistakes may be generated by using the generator polynomial (x)=p(x)(1+x) g(x)=p(x)(1+x). The maximum total block length is 2r-1-1s.

A polynomial that can be factored into additional polynomials may then be selected to balance the maximum overall block length with a desired error detection power. A class of polynomials known as BCH codes is a powerful one. These two samples are merged into one. A generator polynomial that contains the "+1" term will be able to identify error patterns restricted to a window of r contiguous bits, regardless of the reducibility features of the polynomial. "Error bursts" are the term for these patterns.

Specifications

When a share of services or standards committee utilises the CRC to construct a realistic system, the idea of the CRC as an error-detection code becomes more sophisticated. The following are a few of the difficulties:

A predetermined bit pattern may be prefixed to the bit stream to be examined in certain implementations. For example, if a clock fault inserts zero-bits in front of a message, the check value will remain unaltered.

Before performing polynomial division, an implementation would typically add n 0-bits (n being the size of the CRC) to a bit stream. In the Computation of CRC article, such appending is clearly proved. Since the check value is added to the original bit stream, the rest of the bit stream may be divided by the polynomial division function and the result compared to zero to determine if the CRC has been correctly generated. It is possible to achieve a result equivalent to zero appending without explicitly adding zeroes, because of the associative and commutative properties of the exclusive-or operation in practical table driven implementations, by using an equivalent, faster algorithm that combines the message and CRC data streams.

The residue of the polynomial division is sometimes exclusive-ORed using a predetermined bit pattern.

Order of bits: "Low order" refers to the first low-order bit of each byte, however other systems see this as the "first" bit, which denotes "leftmost" in polynomial division. Because many serial-port transmission conventions send the least significant bit (LSB) first, this convention makes sense when CRC-checked in hardware. Byte order: With multi-byte CRCs, it can be confusing whether the byte transmitted first (or stored in the smallest byte of memory) is the least major byte (LSB) or the most significant byte (MSB). In certain 16-bit CRC systems, for example, the check value is swapped.

The divisor polynomial's high-order bit was omitted. If an n-bit CRC must be defined by a (n + 1)-bit divisor, some publications think that it is unnecessary to provide the divisor's high-order bit because the high-order bit always equals 1.

The divisor polynomial's low-order bit was omitted: In order to express polynomials with their high-order bits intact, writers such as Philip Koop may do so without the low-order bit (the x0 or 1 term). The degree of a polynomial is encoded in one number in this convention.

There are three typical methods to represent a polynomial as an integer due to these complications: the first two are mirror copies of binary constants seen in code, and the third is the integer found in Koopmans' publications. One phrase is missing in each example. There are a number of ways to express this polynomial, and the following is one example: (MSB-first code)

• 0xC is equal to 0b1100, which represents (LSB-first code)

• 0x9 is 0b1001, (1x4+0x3+0x2+1x1)+x0, which is the hexadecimal representation of 0x9 (Koop man notation)

B. FAST CRC

From the parallel CRC computation, we developed a technique that can handle any amount of bits being processed in parallel. The CRC calculation unit's power consumption and data traffic may be reduced by using this approach, as well as the correction process itself.

It is known as "channel coding" or "forward error correction" in the field of telecommunications and computer science for its usage in reducing transmission mistakes while using unstable or noisy channels of communication. The key principle is that the sender uses an error-correcting code to encode the information in a redundant manner (ECC). It all began in the 1940s, when American mathematician Richard Hamming set out to discover the first error-correcting code.

In the event of a mistake occurring anywhere else in the message, the receiver may catch it and fix it without having to retransmit. FEC eliminates the requirement for a reverse channel to seek retransmission of data by allowing the receiver to repair mistakes, albeit at the expense of a fixed, greater forward channel capacity. Retransmissions are prohibitively expensive or impossible in FEC scenarios, such as one-way communications systems and multicast broadcasts to a large number of recipients. Mass storage devices sometimes include FEC information to help restore damaged data, and modems utilise it extensively.

When a channel's noise level is high enough, the noisy-channel coding theorem limits the channel's theoretical maximum information transmission rate. The theoretical maximum performance of several modern FEC systems is extremely close to being reached.

Various forward error correcting codes are acceptable for different scenarios based on the maximum percentages of mistakes or missing bits that can be rectified by the FEC code design.

Using an algorithm, FEC makes data transmissions more secure by providing more redundancy. It is possible that a redundant bit is a multi-bit function of several original bits of information in the original data. Some codes contain the original data in their output exactly, while others do not; codes that include the original data are called systematic, while those that do not are called non-systemic.

Due to the fact that each data bit impacts several sent symbols, the noise corruption of certain symbols generally permits the original user data to be retrieved from the other, uncorrupted received symbols that also rely on the same user data. FEC works by "averaging noise"

In the case of NAND flash memory, Hamming ECC is a popular remedy. Single-bit error correction and two-bit error detection are provided by this method. Only SLC NAND can benefit from hamming codes because of their higher degree of reliability.

C. simulation

The design was simulated utilizing ModelSim and Xilinx ISE 145i was used to calculate the area delay, which is necessary for the design, in VHDL. As a result, the updated ETI design with XOR gate takes up more circuit space and causes a delay in implementation.

The purpose of a simulation is to ensure that your design works as expected. After you've completed your design and code, this is the first stage. ModelSim and other simulators like it are used to test your idea. Functional simulation is another name for this process. To put it another way, simulation is nothing more than a technique to test hardware for predicted logical capability without taking into account real timing concerns, such as network and circuit delays.

A. synthesis

A VHDL register-transfer level model of a circuit is used to create a net list at the gate level, which is known as synthesis. At the net list generation stage, there is a process known as synthesis, when register transfer level blocks such as arithmetic logic units and multiplexers are joined through wires to create a net list. Implementing a design into physical hardware is what we mean by synthesis.

If your functional design has been confirmed, rather than only intellectually, then Synthesis is what you're looking for. After we've confirmed your design, we'll move on to hardware implementation. Because of this, you must change the design from RTL to gate level design.

In order to synthesise, there are three steps:

- Translating and optimising content, as well as mapping technology.
- RTL translation to net-lists at the gate level.
- The third degree of optimization is non-optimization-technological logic.

A reduction in the number of components necessary to provide the desired functionality is achieved via optimization. In addition to it, there's a "timing simulation."

III. EXPERIMENTAL RESULTS

A. Simulation Results for 32 bit CRC:

Figure 1simulation results of 32 bit crc

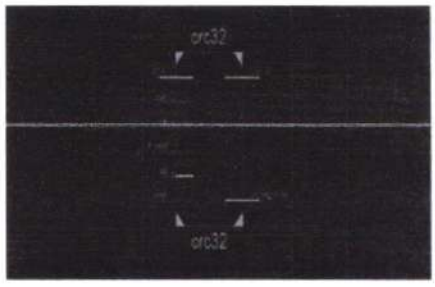


Figure 2 RTL schematic diagram for CRC

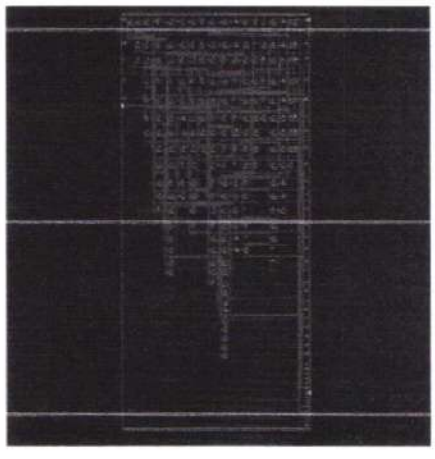


Figure 3 internal schematic diagram for CRC

IV. FUTURE WORK

To eliminate data mistakes in high-speed DSP communications, CRC will be used primarily in the future, as well as in all network streams to prevent data mistakes from transmitter to the receiver in all network-related devices.

V. CONCLUSION

Because of its poor throughput, serial implementation is seldom used for high-speed data transfer. Parallel implementation is preferable since it is faster. To send 64 bytes of data using CRC-32, you'll need 17 clock cycles. When compared to CRC-64, this data is sent in 9 clock cycles. In other words, it dramatically cuts down on processing time by half while also boosting throughput.

REFERENCES

[1] Walma, M., "Pipelined Cyclic Redundancy Check (CRC) Calculation," Computer Communications and Networks, 2007. ICCCN 2007. Proceedings of 16th International Conference on , pp.365,370, 13-16 Aug. 2007

[2] Akagic, A.; Amano, H., "Performance evaluation of multiple lookup tables algorithms for generating CRC on an FPGA," Access Spaces (ISAS), 2011 1st International Symposium on , pp.164,169, 17-19 June 2011

[3] Shukla, S.; Bergmann, N.W., "Single bit error correction implementation in CRC-16 on FPGA," Field-Programmable Technology, 2004. Proceedings. 2004 IEEE International Conference on , pp.319,322, 6-8 Dec. 2004

[4] Toal, C.; McLaughlin, K.; Sezer, S.; Xin Yang, "Design and Implementation of a Field Programmable CRC Circuit Architecture," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.17, no.8, pp.1142,1147, Aug. 2009

[5] Grymel, M.; Furber, S.B., "A Novel Programmable Parallel CRC Circuit," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.19, no.10, pp.1898,1902, Oct. 2011

[6] Akagic, A.; Amano, H., "Performance analysis of fully-adaptable CRC accelerators on an FPGA," Field Programmable Logic and Applications (FPL), 2012 22nd International Conference on , pp.575,578, 29-31 Aug. 2012

[7] Ramabadran, T.V.; Gaitonde, S.S., "A tutorial on CRC computations," Micro, IEEE , vol.8, no.4, pp.62,75, Aug. 1988

[8] Campobello, G.; Patane, G.; Russo, M., "Parallel CRC realization," Computers, IEEE Transactions on , vol.52, no.10, pp.1312,1319, Oct. 2003

[9] Albertengo, G.; Sisto, R., "Parallel CRC generation," Micro, IEEE , vol.10, no.5, pp.63,71, Oct. 1990

[10] Yan Sun; Min Sik Kim, "A Table-Based Algorithm for Pipelined CRC Calculation," Communications (ICC), 2010 IEEE International Conference on , pp.1,5, 23-27 May 2010

[11] http://www.xilinx.com/support/documentation/user_guides/ug384.pdf (last visited on 18.08.2013)

[12] http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/spartan6_hdl.pdf (last visited on 18.08.2013)

[13] Joglekar, A.; Kounavis, M.E.; Berry, F.L., "A Scalable and High Performance Software iSCSI Implementation," File and Storage Technologies (FAST'05) , Proceedings of 4th USENIX Conference on , Vol.4. USENIX Dec, 2005

International Journal of Research in Engineering and Applied Sciences(IJREAS)
Available online at http://euroasiapub.org/journals.php
Vol. 12 Issue 10, October- 2022
ISSN(O): 2249-3905, ISSN(P) : 2349-6525 | Impact Factor: 8.202 |
Thomson Reuters ID: L-5236-2015

INVESTIGATION AND CHARACTERIZATION OF GRAPHITE BASED CARBON REINFORCED LAMINATES

Dr. RAMESH BABU YELURI [1],
Associate Professor,
Avanthi Institute of Engineering and Technology, Telangana, India

MALLIKANTI VENKATESWARLU [2],
Assistant Professor,
Avanthi Institute of Engineering and Technology, Telangana, India

G.VINOD KUMAR[3],
Assistant Professor,
Avanthi Institute of Engineering and Technology, Telangana, India

Abstract

The main objective of this work is to investigate the effect of additives on Tensile and flexural behavior of Carbon Fiber fabric at laminate level to explore an alternative skin material for the outer body of aerospace applications and machines. This experimental work investigates the effect of Graphite concentration in epoxy resin on the Tensile and flexural properties of Carbon fiber laminate of 4 mm thickness. The laminate had been prepared by using hand lay-up method and test has been conducted on it. Various Tensile and Flexural properties values obtained from experimentation have been compared for Carbon fiber laminate composites of three different concentrations were fabricated by adding the Graphite powder to resin bath. The effect of Graphite concentration variation (3%, 6% and 9%) weight on the prepared material. Mechanical properties can be studied by universal testing machine (UTM) according to ASTM standards, and the Experimental results were Tabulated and characterized.

Keywords: composites, fiber reinforced composites, mechanical properties, and laminates preparation.

INTRODUCTION

A composite material is made by combining two or more dissimilar materials. They are combined in such a way that the resulting composite material or composite possesses superior properties which are not obtainable with a single constituent material. So, in technical terms, we can define composite as a multiphase material from a combination of materials, differing in composition or form, which remain bonded together, but retain their identities and properties, without going into any chemical reactions. The components do not dissolve or completely merge. They maintain an interface between each other and act in correct to provide improved, specific or synergistic characteristics not obtainable by any of the original components acting singly. Composite materials are generally costlier as compared to conventional materials but still their use is becoming increasingly popular because of their significant properties like lightness, high specific properties, design and processing flexibility, cost effectiveness, functional superiority, durability.

COMPOSITE MATERIAL CLASSIFICATION:

Composite materials may be broadly classified into natural and synthetic composite materials. Synthetic composite materials are generally prepared by taking the ingredients/ constituents separately and physically combining them by different techniques either random or oriented arranged fibers.

Two ingredients may be composed together as (i) layered composition in which layers of ingredient materials are bonded to one another, and (ii) phase composition in which one ingredient is inserted into the other ingredient. The phase that receives the insert in the phase composition is the continuous phase and is called matrix. The purpose of adding the insert is generally to improve the mechanical properties of the matrix. Presently the most common man-made composites are divided into three main groups they are polymer matrix composites (PMC's), metal matrix composites (MMC's), ceramic matrix composites (CMC's), polymer matrix composites (PMC's). Overall, the properties of the composite materials are determined by the properties of the fiber, properties of the resin, ratio of fiber to resin in the composite (Fibre Volume Fraction), geometry and orientation of the fibers in the composite.

MECHANICAL CHARACTERISTICS TESTING:

Tensile Test: Tensile properties, such as tensile strength, tensile modulus, and Poisson's ratio of flat composite laminate, are determined by static tension tests in accordance with ASTM D 638. The tensile specimen is straight-sided and has a constant cross section with beveled tabs adhesively bonded at its ends. A compliant and strain-compatible material is used for the end tabs to reduce stress concentrations in the gripped area and thereby promote tensile failure in the gage section. Balanced [0=90] cross-ply tabs of non woven Carbon -epoxy have shown satisfactory results. Any high-elongation (tough) adhesive system can be used for mounting the end tabs to the test Specimen.

The tensile specimen is held in a testing machine (UTM) by wedge action grips and pulled at a recommended cross-head speed of 5mm/min. Longitudinal and transverse strains are measured employing electrical resistance strain gages that are bonded in the gage section of the specimen.

ASTM D 638 Standards

- Length- 165mm
- Width- 19mm
- Thickness- 3mm

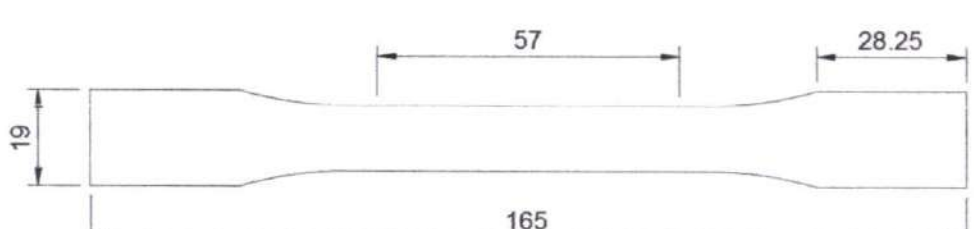


Fig. 01 Tensile Specimen drawing

Flexural Test: Flexural properties, such as Flexural strength, Flexural modulus, and Poisson's ratio of flat composite laminate, are determined by static Flexural tests in accordance with ASTM D 256. The

Flexural specimen is straight-sided and has a constant cross section with beveled tabs adhesively bonded at its ends. A compliant and strain-compatible material is used for the end tabs to reduce stress concentrations in the gripped area and thereby promote Flexural failure in the gage section. Balanced [0=90] cross-ply tabs of non woven Carbon-epoxy have shown satisfactory results. Any high-elongation (tough) adhesive system can be used for mounting the end tabs to the test Specimen.

The Flexural specimen is held in a testing machine (UTM) by wedge action grips and pulled at a recommended cross-head speed of 5mm/min. Longitudinal and transverse strains are measured employing electrical resistance strain gages that are bonded in the gage section of the specimen.

$$\sigma_f = \frac{3FL}{2WT^2}$$

where F is applied load (N), L is support span (mm), w and t are width and thickness of the specimen (mm), respectively.

ASTM D 790 Standards:

- Length- 127mm
- Width- 12.7mm
- Thickness-4mm

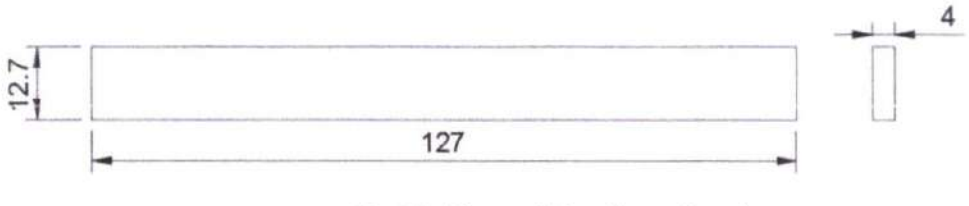


Fig 02 : Flexural Specimen drawing

FABRICATION:

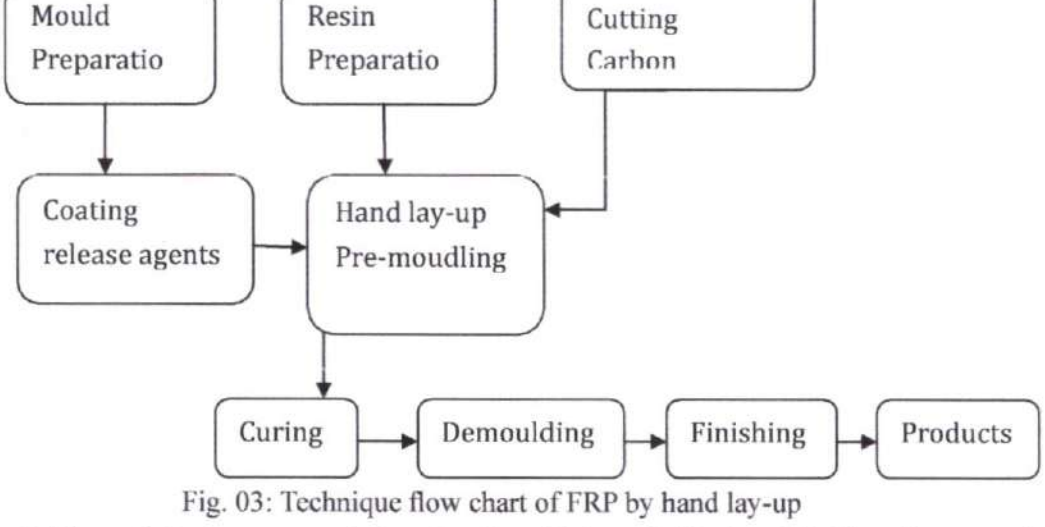


Fig. 03: Technique flow chart of FRP by hand lay-up

Tensile and Flexural test were carried out using Universal Testing Machine for samples of bidirectional oriented Carbon fiber reinforced epoxy resin based polymer composite laminates of different Graphite concentrations and results were discussed.

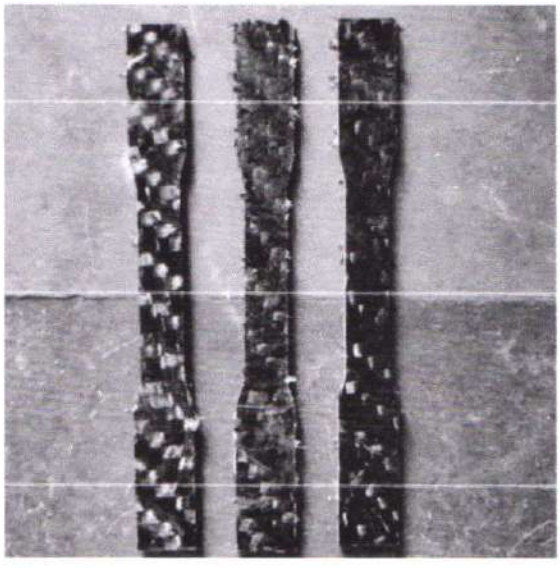


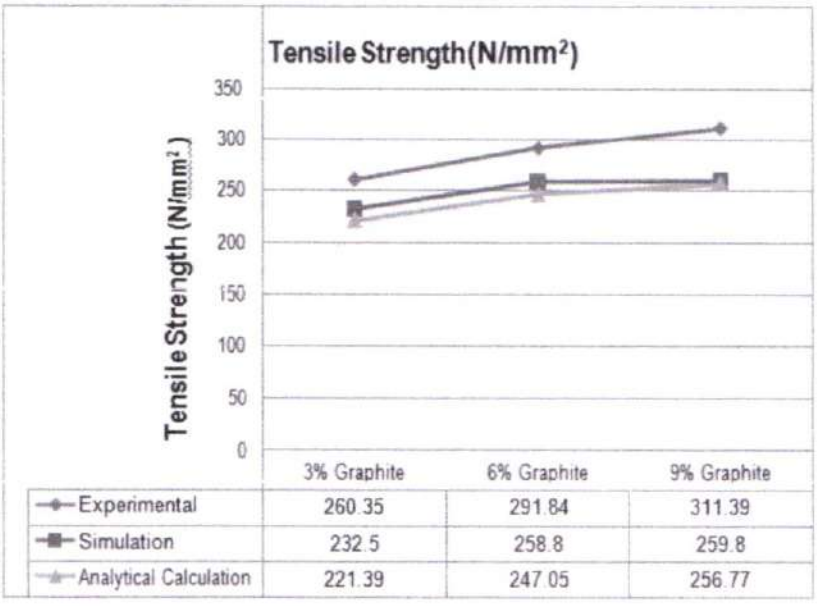
Fig. 04: Final Tensile Specimens from laminates.

RESUTS AND DISCUSSIONS:

The tensile & Flexural specimens from the laminates are subjected to uni-axial load using 20KN capacity Universal Testing machine with the surrounding room temperature of 320C. The load was applied till fracture with a grip displacement rate was maintained at 5 mm/min. Test was done 3 times for each Graphite concentration and the tensile& Impact properties of composite laminates with varying Graphite concentration are calculated and tabulated respectively.

Tensile Test (Carbon+ Graphite)									
	3% Graphite Specimen			6% Graphite Specimen			9% Graphite Specimen		
	n 1	n 2	n 3	n 1	n 2	n 3	n 1	n 2	n 3
Yield Force (N)	11248.23	10173.63	9916.85	9425.37	11136.10	9494.82	10302.49	8921.62	11843.71
Yield Elongation (mm)	11.48	10.32	10.63	11.85	13.56	12.46	13.87	11.84	14.62
Break Force (N)	11512.7	11062.7	10964.7	12150.4	12080.0	12846.7	13352.4	11852.1	12787.9
Break Elongation (mm)	11.81	11.10	11.47	14.55	14.52	16.29	16.75	14.72	15.82
Tensile Strength@ Yield (N/mm^2)	254.37	230.07	224.26	214.12	252.98	215.69	240.26	208.06	276.21
Tensile Strength @ Break (N/mm^2)	260.35	250.17	247.94	276.02	274.42	291.84	311.39	276.40	298.22
Max. Force (N)	11542.43	11087.43	10963.83	12150.44	12121.02	12846.71	13307.62	11852.08	12787.87
Modulus of Elasticity (N/mm^2)	1505.65	1659.13	1457.79	1251.16	1331.06	1296.85	1236.78	1217.27	1227.70

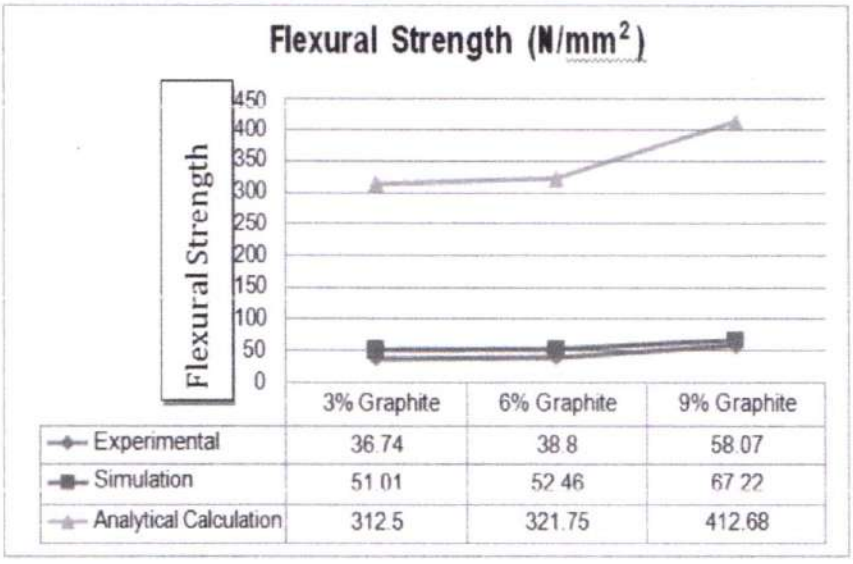
Table 01: Tensile Test results (Carbon + Graphite)



Graph 4: Comparison of Experimental, simulation and Mathematical relations (Tensile Test)

Flexural Test (Carbon+ Graphite)									
	3% Graphite Specimen			6% Graphite Specimen			9% Graphite Specimen		
	n 1	n 2	n 3	n 1	n 2	n 3	n 1	n 2	n 3
Yield Force (N)	311.71	304.02	324.51	333.4	299.94	339.40	373.08	343.59	440.31
Yield Deflection (mm)	3.10	2.93	2.95	2.87	2.76	3.7	3.41	3.42	4.34
Max. Force (N)	312.3	313.0	333.4	333.4	304.0	343.2	382.5	353.0	440.2
Max. Deflection (mm)	15.2	11.1	15.6	3.4	3.1	4.6	6.6	6.6	6.1
Flexural Strength @ Yield (N/mm^2)	35.29	34.42	36.74	37.75	34.29	38.80	49.20	45.31	58.07
Flexural Strength @ Max (Mpa)	171.59	171.98	183.20	183.20	167.84	189.500	226.81	209.36	261.02
Flexural Strain	0.119	0.086	0.12	0.026	0.024	0.035	0.051	0.05	0.04
Flexural Modulus of Elasticity (N/mm^2)	6584.33	4716.20	6682.45	8928.50	7653.62	7560.58	9695.84	8472.46	11336.74

Table 02: Flexural Test results (Carbon + Graphite)



	3% Graphite	6% Graphite	9% Graphite
Experimental	36.74	38.8	58.07
Simulation	51.01	52.46	67.22
Analytical Calculation	312.5	321.75	412.68

Graph 02: Comparison of Experimental, simulation and Mathematical relations (Flexural Test)

CONCLUSION:

Based on the experimental results the effect of additives on Tensile and flexural properties ans behavior of Carbon Fiber at laminates were studied and presented here. And tried to explore an alternative skin material for the outer body of aerospace applications and machines.

The different Graphite concentration processes different properties, and following conclusions are drawn from the above results

- The Tensile Strength of Carbon with 9% Graphite has increased by 19.63% and Carbon with 6% Graphite has increased by 12.11% than Carbon 3% Graphite.
- The Flexural Strength of Carbon with 9% Graphite has increased by 59.25% and Carbon with 6% Graphite has increased by 5.7% and then Carbon 3% Graphite.

With this work Carbon with 9% Graphite is recommended for Tensile and Flexural application. Hence the present study not only discloses that different proportions of Graphite, it also promotes the performance of composites. But those unique tailored properties are improved by changing the proportions of the Graphite filler on the matrix. This indicates that the mechanical properties are mainly dependent on the fiber Filler (Graphite) and orientation of polymer composites.

ACKNOWLEDGEMENT

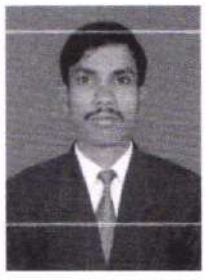
Authors are grateful to Principal Kalyan P. G. College, Bhilainagar for providing laboratory facilities for identification of fungal species and Superintending Archaeologist, Srinagar Circle, Jammu for his support for providing historical and archeological information related to the monument under study.

REFERENCE

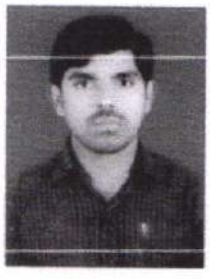
1. M.M. MOHAIDEEN, D.RAVINDRAN,EFFECT OF NANOMATERIALS ON MECHANICAL PROPERTIES OF CARBON COMPOSITES Digest Journal of Nanomaterials and Biostructures 2018

2. S Manigandan, P Gunasekar, S Nithya, G Durga Revanth, EXPERIMENTAL ANALYSIS OF GRAPHENE NANOCOMPOSITE ON CARBON, ICMAEM-2017, IOP Conf. Series: Materials Science and Engineering 2017
3. Prashanth Banakar, H.K Shivananda , Preparation and characterization of the carbon fiber Reinforced epoxy Resin composites, IOSR Journal of Mechanical Engineering, Volume 1, Issue 2(May –June 2012), PP 15-18.
4. Karthik Saravanan.S. Vetrivel.R, Experimental Analysis of Carbon/Glass Fiber Reinforced Epoxy Hybrid Composites with different carbon/Glass Fiber ratios, International Journal of Innovative Research in Science, Engineering and Technology, Volume 5, Issue 5, May 2016, ISSN: 2347-6710.
5. Anoop Anand and Makarandh joshi. Structural composites Hybridized with Nanofillers, Journal of Indian Institute of science, volume 95(2015), ISSN:0970-4140.
6. Abdellatif selmi,Void Effect on Carbon fiber Epoxy Composites,2nd International conference on Emerging Trends in Engineering and Technology(ICETET'2014),May 30- 31,2014 London(UK).
7. T D Jagannatha, and G Harish, Mechanical Properties of carbon/Glass fiber reinforced epoxy Hybrid polymer composites,International Journal of Mechanical Engineering and Robotic Research, vol.4,No.2,April 2015, ISSN 2278-0149.
8. Jyothi Prakash Dhal and S.C Mishra, Processing and Properties of Natural fiber –Reinforced Polymer Composite, Journal of Materials , volume 2013, Article ID 297213,6 pages.
9. Alfred Tcherbi-Narteh, Mahesh V. Hosur, Eldon Triggs, Effects of surface Treatments of Montmorillonite Nanoclay on cure Behavior of Diglycidyl Ether of Bisphenol A Epoxy Resin, Journal of Nano science, volume 2013, Article ID 864141, Hindawi Publishing Corporation.
10. H.B Vinay, H.K Govindaraju and Pranshanth Banakar, Evaluation of Glass/carbon Reinforced Polymer composites, SAGE journals, vol.24, No.7,2016.
11. J.Njuguna, K.Pielichowski, and J.R. Alcock, Epoxy-Based fiber Reinforced Nanocomposites,journal of Research Gate, volume 9, pages 835-847.2017.
12. Muhammad Shahid Nazir, Mohammad Haafiz, Mohammad Kassim, Mazhar Amjad Gilani, Characteristic Properties of Nanoclays and Characterization of Nanoparticles and Nanocomposites, springer Singapore, Journal of Reinforced polymer composites.2016.
13. P.M. Bhagvat, M.Ramachandran, and Pramod Raichurkar, Mechanical Properties of Hybrid Glass/carbon fiber Reinforced epoxy composites,ICAAMM-2016, Materials Today Proceedings 4(2017) 7375-7380.
14. IfeOlorun Olofin, Ronggui Liu,The Application of carbon fiber Reinforced Polymer (CFRP) cables in engineering structures,SSRG International journal(ssrg-ijce), volume 2, Issue 7, July 2015, ISSN:2348-8352.
15. Mr.Chavan V.B, Prof.Gaikwad M.U ,Review on Development of Glass fiber/Epoxy composite Material and its characterizations, International Journal of science, engineering and technology Research (IJSETR), volume 5, Issue 6, June 2016.
16. A.Vikram, V.Nikhil Murthy, C.B.N Murthy, Mechanical & Thermal Properties of carbon fiber/Epoxy composites with Different fiber Orientation, International Journal& Magazine of Engineering, Technology, Management and Research, Volume .2 (2015), Issue no:7(july), ISSN No:2348-4845.

17. R.sreenivasulu, s.Madhusudhan, M.Ashok kumar, V.Nikhil murthy, N.kartikeyan, Synthesis and characterization of Polymer Nanocomposites Filled with Nanoclay/Aerosil on Mechanical and Thermal Properties,International journal of Nanomaterials and Biostructures, volume 3, Issue 4, Pages 51-56.
18. M.Mohith, C.B.N Murthy, V.Nikhil murthy, Chacterization of Epoxy Hybrid composition: Effect of Glass/carbon fiber on Mechanical & Thermal Properties, International Journal & Management Engineering, Technology,Management and Research, volume no. 2(2015), Issue No:7 (july).
19. A.Shirish kumar, V.Nikhil murthy, C.B.N Murthy, Development and Behavior of Mechanical, chemical resistance and Morphology properties of Silicon/Coir Reinforced Epoxy Hybrid composites, International letters of physics and Astronomy, vol 59(2015), pp 124-136, SciPress Ltd.
20. V.Nikhil murthy, B.Suresh kumar Reddy, R.Haranath, Characterization of Epoxy Hybrid composition: Effect of Glass/ Sansevieria cylindrical fiber on Mechanical and Thermal Properties, International journal of Engineering Research, vol.5, Issue: 2, PP: 329-334, ISSN:2319-6890. 11-12 Feb. 2016.



Dr. RAMESH BABU YELURI
Associate Professor,
Avanthi Institute of Engineering and Technology, Telangana, India
E-mail: yrameshbabu321@gmail.com
Published more than 09 papers in the areas of Advanced Manufacturing and its applications. Guided more tan 30 UG_major projects.



MALLIKANTI VENKATESWARLU
Assistant Professor,
Avanthi Institute of Engineering and Technology, Telangana, India
Published 02 papers in the areas of Design Engineerting.

G.VINOD KUMAR,
Assistant Professor,
Avanthi Institute of Engineering and Technology, Telangana, India
Research Scholar: Kakatiya University, Warangal
Pursuing the research in the area of solar energy and its applications. Published more than 20 papers in the areas of Thermal Engineering, Energy Systems and Engineering design.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

OPTIMIZED ROBOT PROCESS AUTOMATED PATH NAVIGATION IN TIME VARYING NETWORKS

[1]Dr.SYED KHASIM and [2]Dr.SHAIK SHAKEER BASHA

[1]Department of Computer Science & Engineering, Dr.Samuel George Institute of Engineering & Technology, Markapur, Prakasam.
[2]Department of Computer Science & Engineering, Avanthi Institute of Engineering & Technology, Gunthapalli, Abdullahpurment Mandal, Hyderabad.

ABSTRACT
The interaction between many empty vehicles is a very challenging topic from a theoretical and material point of view, with far-reaching indicators of scientific and commercial mechanical conditions. The difficulty of connecting the fastest time of multirotor UAVs includes pre-defined local routes depending on the equipment requirements. With the proposed solution, collaborative control is performed in the presence of time-varying communication networks, as well as strong temporary issues, such as simultaneous arrival at the desired terminals. The proposed definition solves the problem of time consolidation under the acceptance that trajectory generation and subsequent assembly of algorithms is provided for guaranteed integration conditions. Communication is processed in unexpected ways using the following method and targeted graph. Optimized Robot Process Automation is an algorithm for detecting very short routes, which is used to avoid / detect collisions / congestion in unexpected ways. Without the discovery of a collision, it does not seem to be compatible to avoid a collision because there would not be everything to avoid. The Dijikloyd algorithm is used to find shortcuts in a targeted graph with a positive or negative margin. The Primloyd algorithm is used to find shortcuts in a weighted non-target graph to overcome complexity in matrix coding. In case of overcrowding or collision the whole network is read about to all its contacts. Therefore, communication occurs unexpectedly in a secure way.

Index Terms
Optimization, Path Navigation, Time Varying Networks, Robot Process Automation, Collision.

1. INTRODUCTION

With the proliferation of communication technology and embedded systems, space communications have greatly improved technology. Especially without human intervention, the planes are designed to fly high in space for commercial and surveillance purposes. The Unmanned Aerial Vehicle (UAV) is a type of aircraft with no pilot. Based on systematic data, the UAV can be remotely controlled [1]. In recent times, the automotive autonomous field has a wide range of research programs in the field of Sensor fusion, Multi-agent Liaison, Traffic Planning, Trajectory Production, Task Allocation and Planning and Collaborative Strategies.

The main goal is to completely avoid the pilot from using the UAV and to stay away from plane crashes. When a UAV is moved and controlled by systems built by the Air Traffic Controller (ATR), there are some difficult tasks that need to be done to reduce the distance between the first stop and the last stop. The number of available modes of flexibility may change the direction of the UAV during its boarding time from the normal route is a significant problem [2].This paper focuses on controlling the existence of time-varying communication networks, as well as strong temporary issues, such as simultaneous arrival at the required final destinations.

The proposed solution solves the problem of time communication under acceptance

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

that the trajectory generation and subsequent algorithms meet certain stability conditions [3] .The Coordinated Path Following and Vehicle Coordination algorithm, solving the problem of temporary communication failure under Lyapunov-based theory [4] .In their presented work, development algorithms are developed in an extended area where sub-systems are different. The design action is based on the successive use of convex development tools. The proposed solution solves the problem of time communication under the assumption that the algorithm followed meets certain stability conditions [5][6].

POMDP and portable algorithms compared to large groups of flexible robots. Separating the Partially Observable Markov Decision Process (POMDPs) as long as the interdependence of multiple robots is maintained through the POMDP policy auction [7][8]. The task of avoiding obstacles, the ability of a method to avoid structural collisions with standing and flexible obstacles during its movement in the desired target area using the Hawk-eye method [9], while a strong and flexible control scheme. to deal with the indirect system and external disturbances due to the closed structure.

2. RELATED WORKS

Kalman's direct filter is introduced [10] to integrate local quadrotor measurements. The control strategy controls the flexible pay-out of the desired position while also controlling the aging to zero, the main idea behind the method is based on common strategies guaranteed by managing the flexible ring. Suitability of this method Communication is easy in the defined method [11]. Model-based and independent control methods are introduced in [12] to design independent quadrotors.

The parallel work includes Sliding Mode control theory [14], Model Independent Linking Strategy [13], stability structures for a group of mobile agents [15], a repetitive algorithm with local integration behavior using a vague programming solution in each recurring area. step and line matrix [LMI] imbalance combined with logic-based changes reflect light on various control strategies [16].This limit has prompted us to change the approach to problem tracking in a different way.

The purpose of this paper is to provide a new solution to every defined or unspecified method using a tracking method and a targeted communication graph. Route can be accessed and communication is processed in unexpected ways using the following method and targeted graph. Optimized Robot Process Automation is an algorithm for detecting very short routes, which is used to avoid / detect collisions / congestion in unexpected ways. The Dijikloyd algorithm is used to find shortcuts in a targeted graph with positive or negative margins.

The Primloyd algorithm is used to find shortcuts in the indirect graph that weigh complexity over matrix coding. In case of overcrowding or conflict the whole network will be read so to all contacts. Therefore, communication takes place in unexpected ways in a given way. The purpose of this paper is to provide the best route conditions for all types of routes. Find a shortcut to both defined and unspecified routes. Avoidance / getting congestion / collisions in unexpected ways. This paper is structured as follows. In Phase II, we present the proposed project. In Section III, we describe the following problem by providing the appropriate set of algorithms. In Section IV, we construct a flow diagram; simulation results are described in Section V.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

Finally, in Section VI, the main conclusions are presented..

3. PROPOSED WORK

At this stage, the proposed operation of the control algorithm that follows the UAV interoperability method is introduced. To overcome the problems that exist, here is a suggestion method of the Optimized Robot Process Automation algorithm used to find short free routes to the destination in unexpected ways.

3.1 Overview of the Proposed UAV Environment

In this section, we propose the Optimized Robot Process Automation method for obtaining free short collisions on the weighted graph and the indirect weighted graph. Figure 1 shows a block diagram of the proposed system. A communication network is used to exchange information between vehicles. Once the connection is complete, the UAV will select Robert's algorithm to avoid collisions / congestion in unexpected ways.

After that the algorithm Dijikloyd and Primloyd were transferred by UAV which is the way it should go. If the path is clear the UAV will select the Dijikloyd algorithm and pass through the path we have already given which is the predefined path. If the path is unclear the UAV will select the Primloyd algorithm and pass the unspecified route. The unspecified route is identified by the path / node closest to the original / predefined path.

The following route allows each car to follow the route assigned to the desired speed profile. Once the route has been identified you will check the time alignment if it is clear that it will adhere to the route. If the timeline is not clear it will wait until clear ways are found. Time management controls a car in a time when one car will not collide. Time communication will check the reference generation whether there are cars on the road or not. If all is clear the car will move in the next direction.

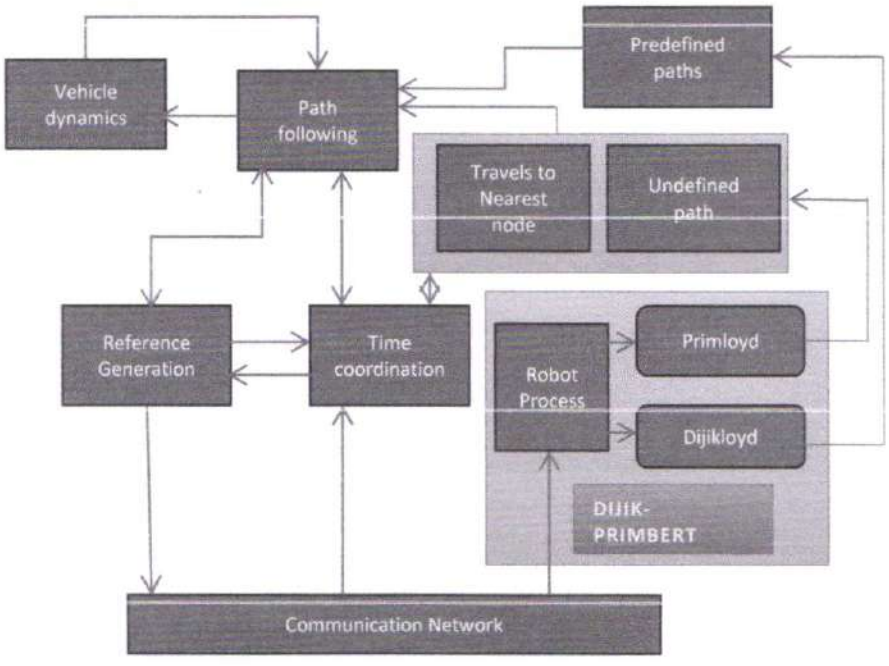


Fig. 1 Block diagram of proposed UAV environment and interactions between them.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

4. PATH-FOLLOWING: PROBLEM FORMULATION

We are now dealing with the next issue of multirotor UAVs. As mentioned earlier, the method can be found and communication is widely used and information across the network increases network topology. The Optimized Robot Process Automation Algorithm is used to find free shortcuts to source on unexpected routes.

4.1 Optimized Robot Process Automation method algorithm for unpredictable paths

The Optimized Robot Process Automation method algorithm is a combination of Dijikloyd algorithm, Primloyd algorithm and Robert algorithm. Optimized Robot Process Automation is an algorithm for detecting very short routes, which is used to avoid / detect collisions / congestion in unexpected ways. Collision detection is simply the act of exploring a known area and identifying possible collisions. Without the discovery of a collision, it does not seem acceptable to avoid a collision because there would be no avoidance.

Collision avoidance is a system of action taken by the robot algorithm to avoid future collisions. As previously announced, there is no need for a collision avoidance algorithm if no conflict should be avoided. A node diagram for finding unpredictable route using the Optimized Robot Process Automation algorithm method is shown in Fig.2. Avoiding collisions, as opposed to colliding with a collision, is what is done after a detection that may be a collision. When making an effort to avoid a hindrance, there are many choices you have to make. The choices that are made will depend on the options available to the robot to prevent it. Finding the right method can be frustrating depending on which algorithm is used and the granularity associated with it.

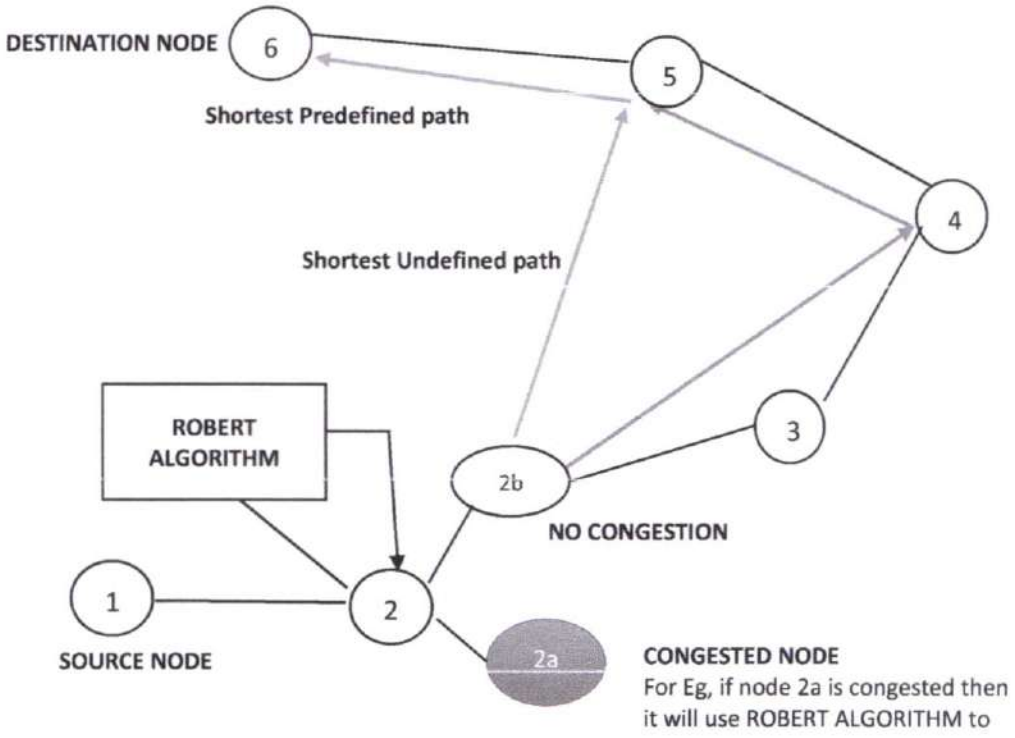


Fig. 2 Node diagram of the Optimized Robot Process Automation method algorithm for unpredictable paths.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

4.2 Dijikloyd algorithm for defined path

The Dijikloyd algorithm is a combination of a Dijkstra algorithm and a Floyd-warshall algorithm. The Dijkstra algorithm is a graph search method that finds a cost-effective method within the vertex and resolves the short-term conflict of a single source graph with the cost of the edge on a non-negative edge, producing a very short path to the local vertex. This algorithm is commonly used on the route and in the path below the other graph algorithms on the targeted graphs which are not negative. The Floyd-Warshall algorithm is a graph analysis method for finding shortcuts on a graph with a positive or negative weight. The Floyd algorithm is an example of flexible planning. The Dijikloyd algorithm is a graph search algorithm for finding shortcuts on a targeted graph with a straight and negative edge. The convenience of this algorithm is that it is easy to encrypt and quickly calculate finder networks.

4.3 Primloyd algorithm for undefined path

The Primloyd algorithm is a combination of the Prims algorithm and the Floyd-warshall algorithm. Prims algorithm is a fast-paced algorithm that finds a small stretchable tree and arranges the edges with the weight of a non-targeted graph. This means that it acquires an existing subset that forms a tree that contains the entire vertex using a key line, where the total weight of all the corners of the tree is reduced. The Floyd-Warshall method analyses all possible graphs to determine. an easy way between each pair of tweets. If there are negative times, the Floyd-Warshall algorithm can be used to identify them. The Floyd-Warshall algorithm usually only supports the length of the lines between all pairs of vertices. When a very short new path is found between two tweaks, a matrix that combines paths with high flow between vertices is updated. The Primloyd algorithm is used to overcome difficulties in matrix writing. The validity of this algorithm is simple and easy to code.

5. ALGORITHM AND COMMUNICATION FLOW DIAGRAM

Let the node at which the UAV is starting called the **initial node**. The **distance** from initial node to destination node is taken as **Y**.

Algorithm for finding unpredictable paths using Optimized Robot Process Automation method algorithm

Let the Optimized Robot Process Automation method algorithm is a decent version of one simple line and works well on simpler methods. The Optimized Robot Process Automation Algorithm will also provide initial node values and will try to find a short free step-by-step collision method.

Announce input to social networks.

Check that the congestion / collision condition is y <= n.

If the above condition is satisfactory then it will detect and correct the congestion / collision using the Robert algorithm.

The Primloyd algorithm is then used to track potential unexplained pathways and to obtain a shorter distance between tracked paths.

If the situation is not satisfactory then it will pass through the Dijikloyd algorithm.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

The Dijikloyd algorithm is used to find the shortest method previously described.

Algorithm for finding defined path using Dijikloyd algorithm

Let the starting point of the UAV be called the first node. Let the Y-node distance be the interval from the starting point to Y. The Dijikloyd algorithm will provide initial length values and will try to improve them step by step.

Assign a conditional range value for each node: set zero on the first node and infinity for all other nodes.

Mark all node intervals from the starting point and line.

Subtract an important distance from the line.

If any line is empty or has a long distance, get acquainted with the current location.

In the absence of a neighbor add a new neighboring distance range + current node distance.

If there is a neighbor calculate the negative aspect of the node i.e. the value of the threshold is greater than the negative value.

The new distance value must be less than the old in both case 5 and step 6.

If step 7 is satisfactory proceed to the next step, otherwise discard.

An undefined discovery algorithm using the Primloyd algorithm

Let the node we choose be called the first node. The Primloyd algorithm will also select the first range values and will try to find the unstructured method step by step.

Start a tree with one vertex, allow a minimum distance in each area.

Focus on variables n, X, Y, number = 1. Set the input number of rows and start X = 1 and Y = 1.

Follow the possible routes and find the shortest distance between the trails.

If X is less than or equal to n and Y is less than or equal to n Print the numerical value and the increment number, Y.

If they see a candidate model and find the neighbor of the current node.

If X is less than or equal to n and y is not equal to n print n then increase the value of X.

If X is not less than n stop.

5.1 Communication flow of Optimized Robot Process Automation method algorithm

A flow diagram of finding a method described using the Dijikloyd algorithm is shown below in Fig. 3. Figure 4 below shows the flow diagram of the indeterminate path using the Primloyd algorithm. A flow diagram of finding an unpredictable route using the Optimized Robot Process Automation algorithm method is shown below in Fig. 5. The Optimized Robot Process Automation method algorithm is a decent version of one simple line and works well on simpler methods. The Optimized Robot Process

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

Automation Algorithm will also provide initial location values and will try to find the shortest free collision method. In the Dijikloyd algorithm, start with the first vertex with a zero distance. Trace the possible paths from the beginning of the vertex and get the shortest distance. Mark it as the next first term to add current and past grades. Repeat the steps above. In the Primloyd algorithm, start with the first vertex and follow the possible paths. Find the shortest distance between trails and adjust the shortest route. From the new vertex repeat the steps above and finally check all the vertices along the trail.

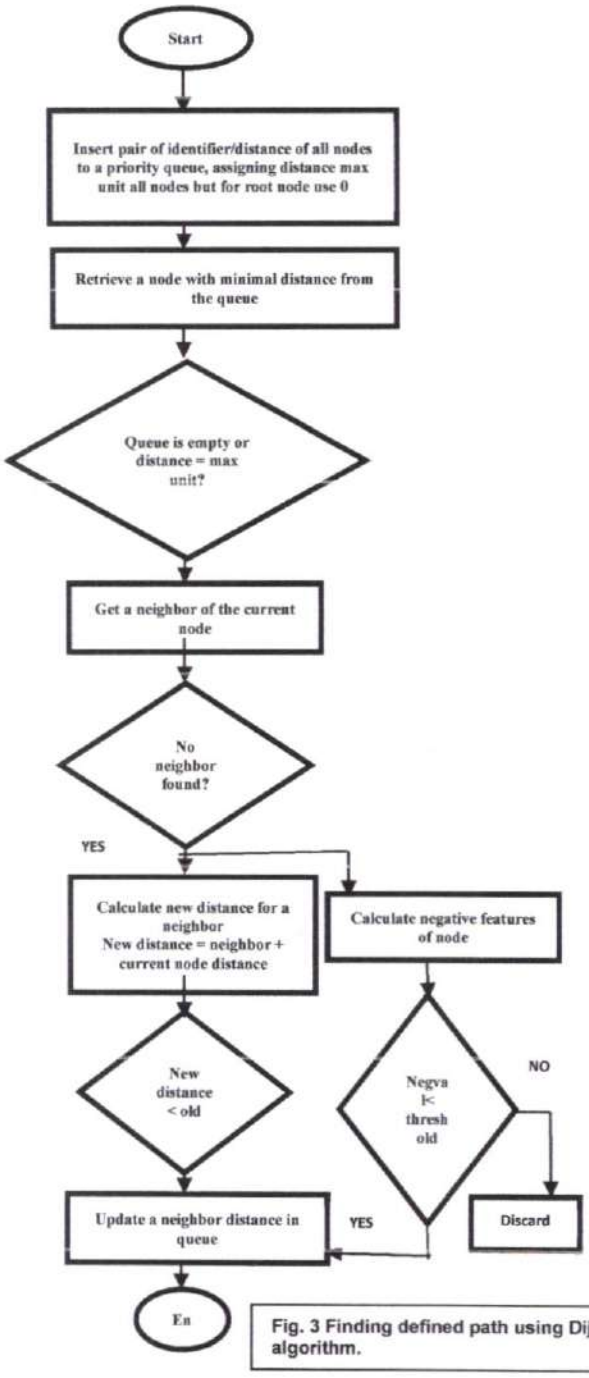


Fig. 3 Finding defined path using Dijikloyd algorithm.

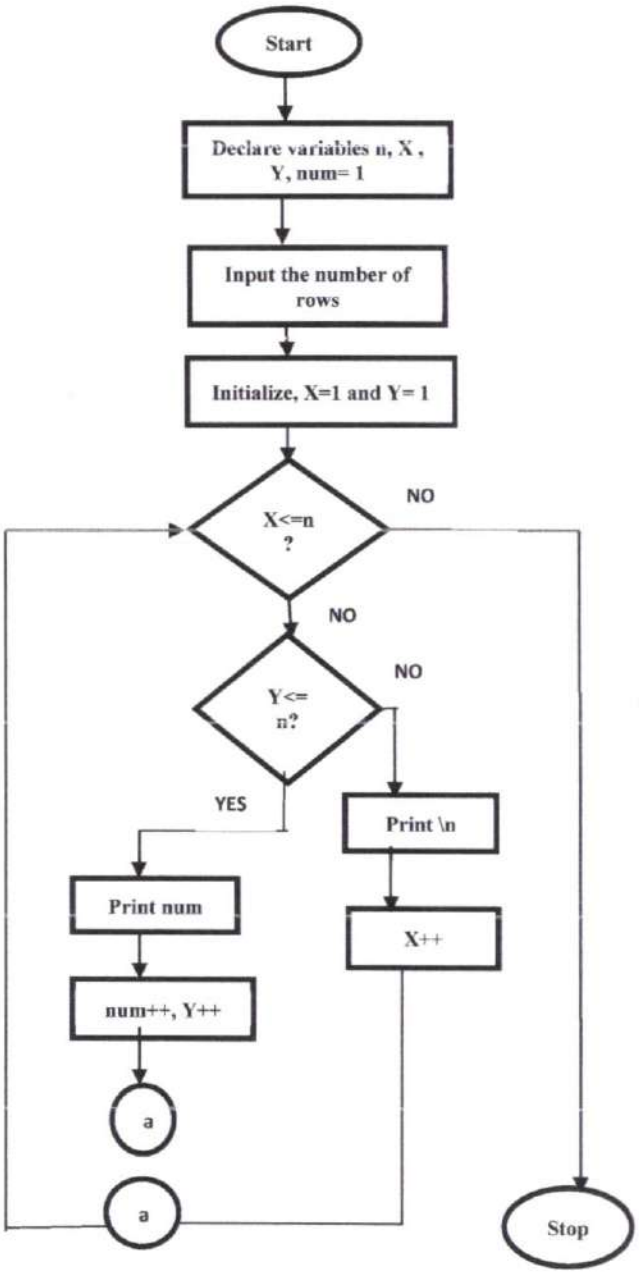


Fig. 4 Finding undefined path using Primloyd algorithm.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

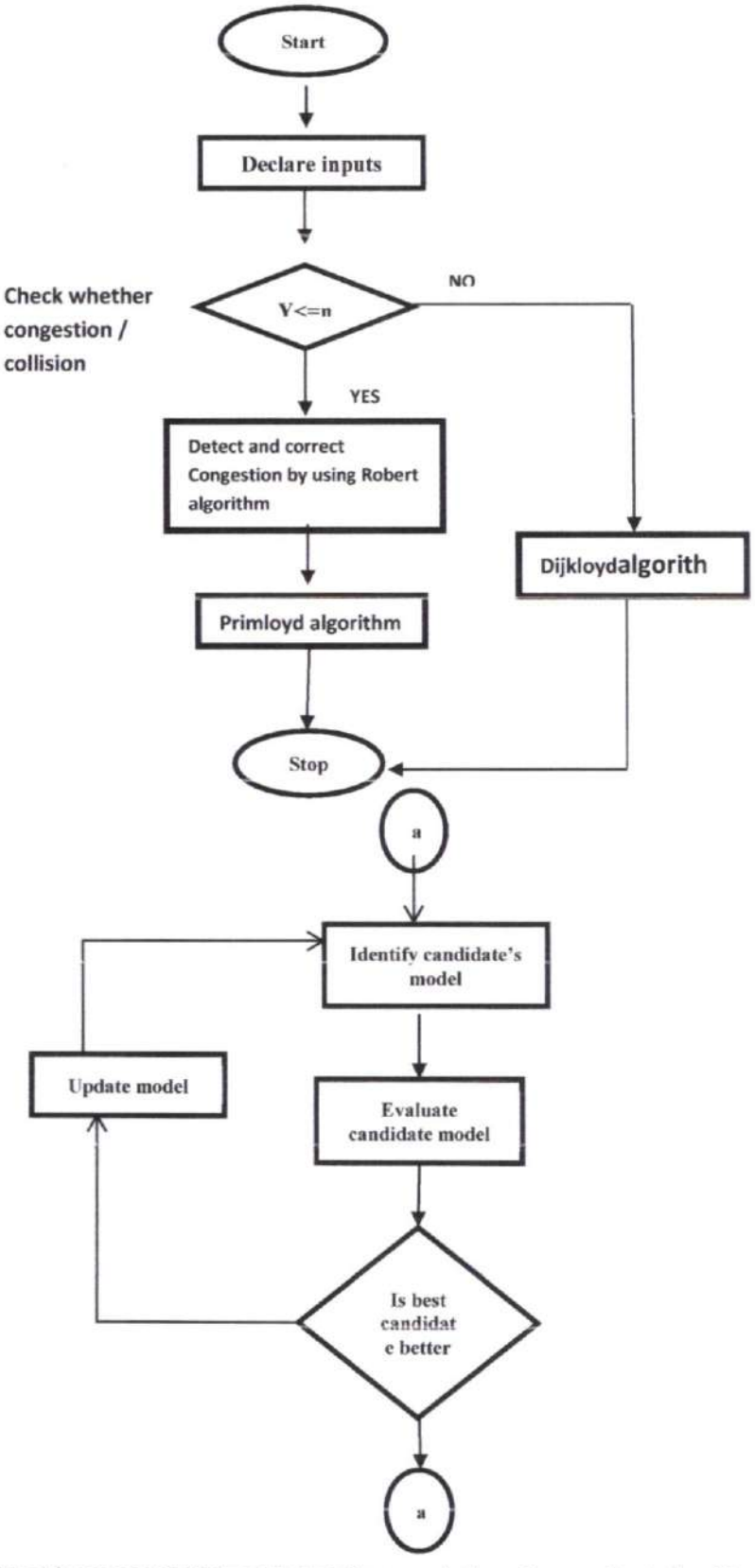
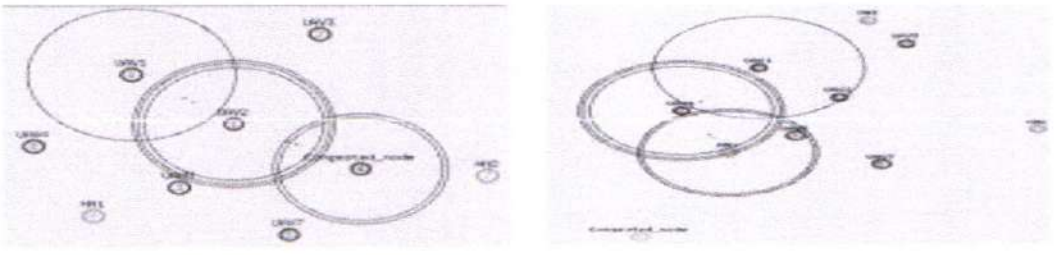


Fig. 5 Finding unpredictable paths using Optimized Robot Process Automation method algorithm.

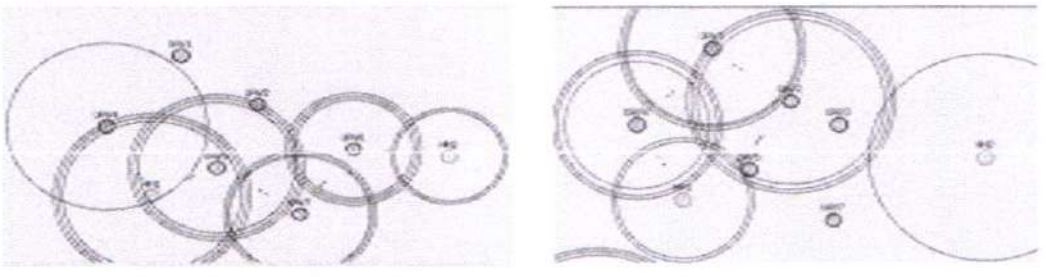
Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

6. EXPERIMENTAL RESULTS AND OUTPUTS

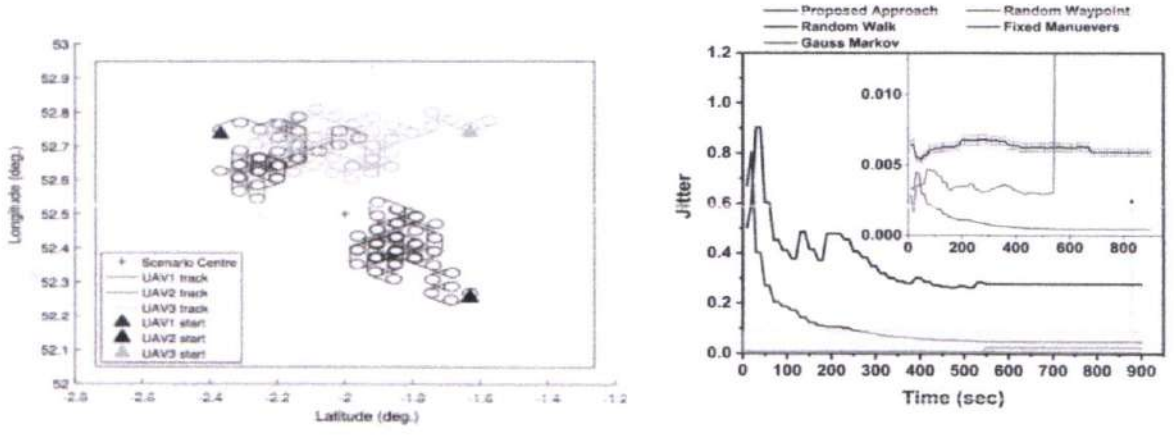
In this section, we present the simulation results of the Optimized Robot Process Automation algorithm method operated in MATLAB and NS2.Here nine nodes are produced, three acting as header nodes and seven as UAV nodes. The Optimized Robot Process Automation Algorithm is used to find free shortcuts to source on unexpected routes. Initially it defines a command window to display defined and unspecified methods with low cost of calculation and further communication.



6 (a) **UAV6 is congested due to packet loss and it is removed**

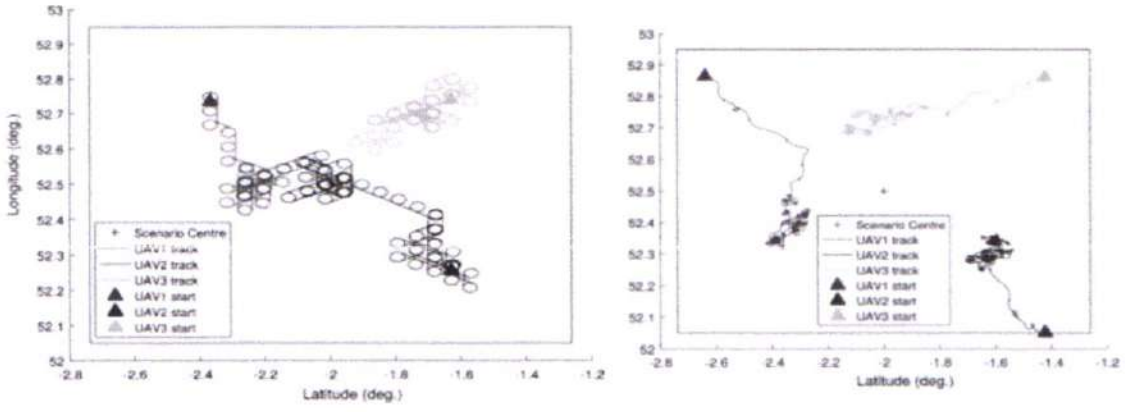


6 (b) **UAVs communicating in a predefined and undefined path**



(a) (b)

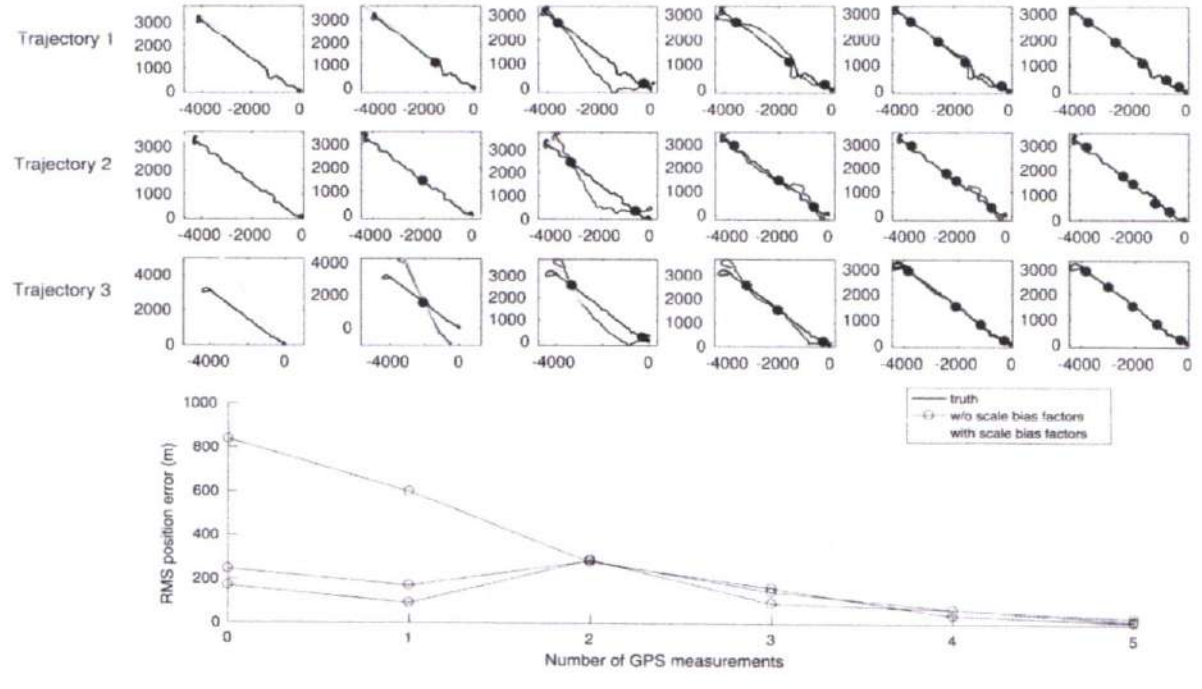
Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV



(c) (d)

Fig. 7 UAVs communicating with all header nodes and verifying the performance with X graph for the performance of packets

Figure 7 (a) shows that the UAV6 is overcrowded due to packet loss and is being removed from the road Figure 7 (b) shows the UAV communicating in a predefined and undefined manner. Figure 7 (c) shows the X graph of packet performance at the required time. In the present system, the Multivehicle cooperative supremacy follows a trajectory generation algorithm, a tracking algorithm and a time-linked control algorithm used. Route control allows each vehicle to meet and follow the assigned route but detects traffic congestion only on a predetermined route. So there is a need to use an algorithm to get an unexpected approach. Therefore, it is proposed that the Optimized Robot Process Automation algorithm be used to obtain a short free crash path in unexpected ways.



Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

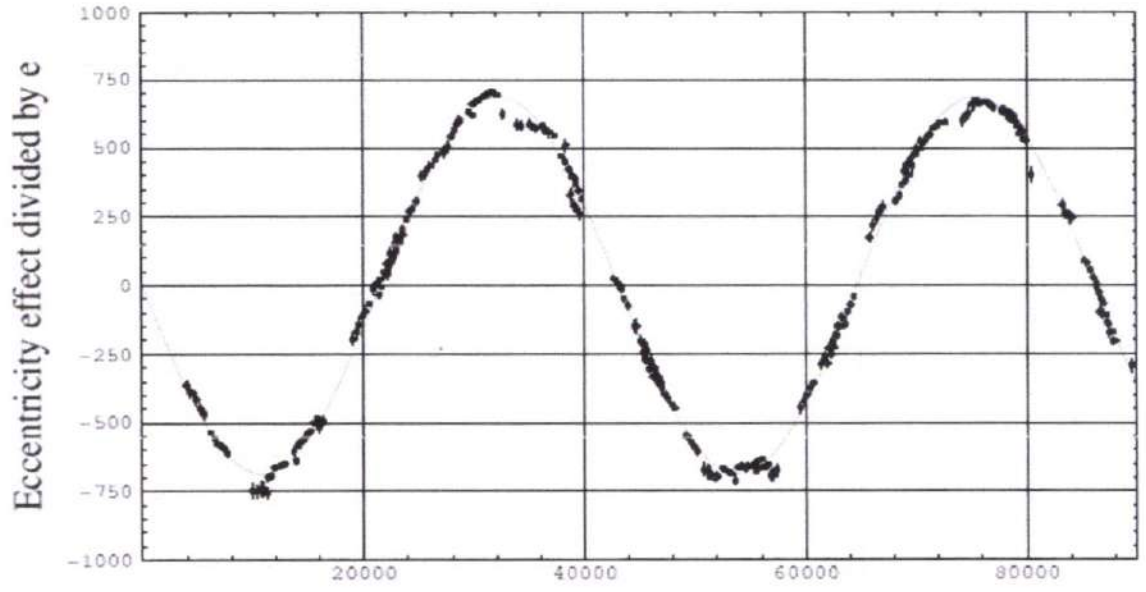


Fig. 8 Comparison of existing and proposed method

Figure 8 shows a comparative analysis chart of existing route links and proposed links in unexpected directions. Table.1 shows a comparison table of the existing communication path in the specified line and the proposed connections to the unexpected paths at a different number of nodes at the required time.

Table. 1 Comparison table of existing and proposed method

Path selection mode	Number of nodes	Required time
Ideal Communication Ideal PF	4 2 0	0 0.6 2.8
Non-Ideal Communication-Ideal PF	4 2 0	0 1.4 4.2
Non-Ideal Communication-Non Ideal PF	4 2 1	0 3.2 4.0
Dijikloyd	5 3 1	1.0 2.2 3.2
Primloyd	5 3 2	4.2 1.2 3.0
Robert	5 3 1	0 2.2 4.0

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

7. CONCLUSION

In this paper, an effective approach is determined by proposing the Optimized Robot Process Automation method for piloting UAVs and considering short-term free routes found on unexpected roads. Optimized Robot Process Automation method with features Dijikloyd, Primloyd and Robert. Dijikloyd with elements of Dijikstra and Floyd. Primloyd has features of Prims and Floyd. Here the function of calculating the short free collision method is enhanced. It is also well used in UAVS. The future works, it will use the intermittent communication (i.e.) Markov's law to find free ways to conflict, the Markov Decision Process (MDP) generates the idea of resolving multiple threats in the conflict prevention program and a unique feature to create a real conflict avoidance problem.

REFERENCES

1. Palani Murugan, P., Chinnadurai, M., Manikandan, S. (2022). "Tour Planning Design for Mobile Robots Using Pruned Adaptive Resonance Theory Networks". CMC-Computers, Materials & Continua, 70(1), 181–194, doi:10.32604/cmc.2022.016152
2. Manikandan, S., Chinnadurai, M. (2022), "Virtualized Load Balancer for Hybrid Cloud Using Genetic Algorithm", Intelligent Automation & Soft Computing, 32(3), 1459–1466, doi:10.32604/iasc.2022.022527
3. Y. D. Song, Y. Li, and X. H. Liao, "Orthogonal transformation based robust adaptive close formation control of multi-UAVs," in *Proc.Amer.* Portland, OR, June 2015.
4. R. Ghabcheloo, A. M. Pascoal, C. Silvestre, and I. Kaminer, "Coordinated path following control of multiple wheeled robots using linearization techniques," May 2016.
5. M. Turpin, N. Michael, and V. Kumar, "Concurrent assignment and planning of trajectories for large teams of interchangeable robots,"2020.
6. Manikandan, S, Chinnadurai, M, "Effective Energy Adaptive and Consumption in Wireless Sensor Network Using Distributed Source Coding and Sampling Techniques",. Wireless Personal Communication (2021), 118, 1393–1404 (2021)
7. U. Gurcuoglu, G. A. Puerto-Souza, F. Morbidi, and G. L. Mariottini, "Hierarchical control of a team of quadrotors for cooperative active target tracking," in *2018.*
8. S.Manikandan, M.Chinnadurai, D.Maria Manuel Vianny and D.Sivabalaselvamani, "Real Time Traffic Flow Prediction and Intelligent Traffic Control from Remote Location for Large-Scale Heterogeneous Networking using TensorFlow", International Journal of Future Generation Communication and Networking, ISSN: 2233-7857, Vol.13, No.1, (2020), pp.1006-1012.
9. S. Gupte, P. I. T. Mohandas, and J. M. Conrad, "A survey of quadrotor unmanned aerial vehicles," in *Proc. IEEE* 2012.
10. V. Cichella, I. Kaminer, E. Xargay, V. Dobrokhodov, N. Hovakimyan, A. P. Aguiar, and A. M. Pascoal, "A Lyapunov-based approach for time-coordinated 3D path-following of multiple quadrotors," in Dec. 2012.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN : 1671-5497
E-Publication : Online Open Access
Vol: 41 Issue: 04-2022
DOI 10.17605/OSF.IO/WX4CV

11. V. Gazi, "Swarm aggregations using artificial potentials and slidingmode control," *IEEE Trans. Robot.*, vol. 21, 2015.

12. Gui, T., Ma, C., Wang, F., & Wilkins, D. E. (2016). Survey on swarm intelligence-based routing protocols for wireless sensor networks: An extensive study. In 2016 IEEE international conference on industrial technology (ICIT). 1944–1949.

13. H. Tanner, A. Jadbabaie, and G. Pappas, "Flocking in fixed and switching networks," 2020.

14. J. Capitan, M. T. Spaan, and A. Ollero, "Decentralized multi-robot cooperation with auctioned POMDPs,"2015.

15. Y. Kim "On maximizing the second smallest eigenvalue of state-dependent graph Laplacian," Jan. 2016.

16. Gupta, P., & Jha, S. (2018). Integrated clustering and routing protocol for wireless sensor networks using Cuckoo and Harmony Search based metaheuristic techniques. Engineering Applications of Artificial Intelligence, 68, 101–109.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

The Design of Low-Power And High-Speed Full Adder Through The Exploration of Novel XOR And XNOR Gates

Chukka Navarathna
M.Tech student ECE, VLSI system design. Avanthi institute of Engg & Tech.
Dr.S. Kishore Reddy
Associate professor, HOD ECE, VLSI design Avanthi institute of Engg & Tech.
E mail : kishorereddy416@gmail.com
Vasantha Naga Raju
Assistant professor, ECE Department, Avanthi institute of Engg & Tech.
E Mali: vasanthanagayadav@gmail.com

Abstract

In this project, we propose six different hybrid full adder circuits that make use of the XNOR, XOR gates that have lately come into existence. These circuits are tuned with respect to power use and processing speed in contrast to more standard designs. This is a viable choice due to its low output capacitance. There was no clear winner among the three proposed full adder circuits, which all fared well in terms of speed, power consumption, and motor control. In this work, we propose a novel family of circuits that can execute XOR, XNOR, and XOR/XNOR in parallel. The suggested circuits are well optimised in terms of power consumption and delay thanks to their low output capacitance and low short circuit power dissipation. We introduce six novel hybrid 1-bit full-adder (FA) circuits and a Ripple Carry Adder based on the special full-swing XOR-XNOR or XOR/XNOR gates. Each of the proposed circuits has benefits and drawbacks that must be considered. A new strategy for transistor sizing is presented to optimise the PDP of the circuits. The proposed method uses a particle swarm optimisation methodology for numerical computing to determine the best PDP. The effects of changing the transistor size, supply voltage, output capacitance, input noise immunity, and threshold voltage on the proposed circuits are investigated.

Key words: ***XOR-XNOR, full-adder, Ripple Carry Adder***

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

1. Introduction

The present work presents six unique hybrid full adder circuits, each of which makes use of the newly invented XNOR, XOR gates. All of the hybrid full adder circuits are presented here. When compared to designs that are more traditional, these circuits are optimised in terms of both the amount of power they use and the speed at which they process information. This choice is a good one to choose with since it has a relatively low output capacitance. Due to the fact that each of the three recommended full adder circuits performed comparably well in terms of speed, power consumption, and motor control, it was not possible to identify a single obvious winner. Tanner is the name of the simulation tool that is utilised for the simulations of the 45-nm technology. The performance of the proposed circuits is superior than that of the reference circuit. It is possible to test the performance of the suggested full adder circuits by making adjustments to the voltage at the input and the load at the output.

All three of these novel families of circuits, XOR, XNOR, and XOR/XNOR, are offered here as potential candidates for parallel implementation. The suggested circuits have a low short circuit power dissipation and a low output capacitance, which makes them highly optimised in terms of power consumption and delay thanks to these characteristics. It is shown that there exist six novel hybrid 1-bit full-adder (FA) circuits that are based on the peculiar full-swing XOR-XNOR or XOR/XNOR gates, in addition to a Ripple Carry Adder.

2. Existing Method

In mathematics, an adder may be either a "half adder" or a "full adder." The term "adder" may be used to refer to either species. A "half adder" with just two inputs and two outputs is completely useless in practise. In order to carry out operations like fast Fourier transforms (FFTs) and infrared integral and differential filters (IIRs), the ALU makes use of a complete adder, which is an adder with three inputs and two outputs. Three inputs and two outputs define a complete adder. The power consumption, output latency, and board area of the conventional full adders employed in ALU are all much higher. However, modern consumers are increasingly expressing

an interest in devices that are user-friendly, compact, lightweight, durable, and versatile. Hybrid technologies have developed in response to the aforementioned causes. As the use of mobile communications and personal computers continues to surge, the creation of low power hybrid VLSI systems has emerged as a crucial performance goal. That's because developments in each of those areas are accelerating at a rapid pace. Hybrid systems combine several kinds of reasoning into one cohesive whole. For the most part, a hybrid one-bit full adder is made up of a combination of complementary metal oxide semiconductor (CMOS) logic, transmission gate logic, and pass transistor logic.

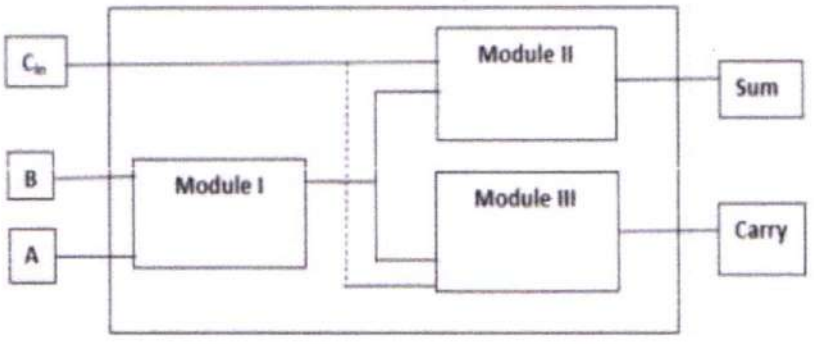


Figure 1: Block diagram of hybrid logic FA circuit

For the purpose of carrying out logical processes, XOR/XNOR circuits as well as simultaneous XOR-XNOR circuits.The suggested XOR-XNOR circuit exhibits high performance in terms of power consumption, latency, low output capacitance, driving capacity, and resilience. This is the case even if the crucial route does not have a NOT gate. The circuit is comprised of twelve transistors. The XOR-XNOR circuit that has been suggested is between 16.2% and 85.8% more efficient in PDP while also being quicker by 9% to 83.2%. Full adders are available in a variety of formats, including conventional CMOS full adders, New14T full adders, CFA full adders, TFA full adders, TGA full adders, and New-HPSC full adders. The passage of time is determined by the dynamic interaction of the vehicle's speed, its driving abilities, and its input capacitance while using this cutting-edge approach. [6] is an example of an all-encompassing adder that use CMOS logic in conjunction with transmission gates and Pass transistors. The adder in its entirety is simulated using Cadence's tool, which is tailored for technology

operating at 45 nm. The performance of the recommended full adder is evaluated in comparison to that of 20 other full adders currently on the market, the supply voltages of which vary from 0.4V to 1.2V. Ongoing research is being done in order to build a high-performance adder that is completely functioning. In this investigation, our primary emphasis is on developing a complete adder that has lower latency and uses less transistors. Additionally, we examine and evaluate two additional designs that also make use of fewer transistors. The anticipated characteristics and benefits of using this low-power logic architecture are outlined in the following paragraphs. It is feasible to activate some line multiplexers using an external signal in specific cases. The select line of the multiplexers is instead controlled by the Carry input signal, which has a complete voltage swing but no propagation delay. This was done so that the total propagation latency of the adder could be reduced.

XNOR and XOR gates are often used in the construction of full adders. When it comes to the amount of power that it requires, an XOR or XNOR circuit in a complete adder wins the prize. Therefore, a reduction in the amount of power consumed by the XOR or XNOR circuit will result in a reduction in the amount of power needed by the adder as a whole. The XOR and XNOR gates are both used in a variety of different circuits, such as comparators and parity checks, amongst other applications. In recent years, there has been a meteoric rise in the demand for portable electronic devices. These gadgets need to have a high speed and a low energy consumption. Improving the performance of the system calls for paying attention to design aspects such as the amount of power it consumes. [2] A great number of arithmetic-operating circuits need the whole adder as a fundamental component. Because of this, the effectiveness of the complete adder (also known as "3") is essential to the operation of the whole system. As a result, it is conceivable that an increase in the full adder's efficiency might be beneficial to the overall performance of the system. Using a variety of logic approaches, several types of complete adder circuits have been built, each of which comes with its own individual set of advantages and disadvantages [4-6]. There are now two primary categories that may be used to classify each and every design. These might be considered static or dynamic, depending on the context. There are a number of advantages to using static full adders,

including how simple they are to use, how little power they need, and how reliable they are. When compared to its static counterparts, dynamic full adders take up a much less amount of space on the chip. It has been shown that some types of performance are better suited to particular ways of thinking, while other types of performance are more suited to other ways of thinking. CMOS [5, 6], DPL [7], TGA [8, 9], and TFA [10, 11] are some of the standard techniques to the design of logic circuits. Adders of the hybrid-logic type are considered to be complete adders since they incorporate a range of logic approaches. In an attempt to improve the performance of complete adders, these designs use aspects drawn from a wide range of logic systems.

The output carry signal is produced by the recommended circuit (see Fig.), which does so with the assistance of the transistors NMOS 5, PMOS 5, and NMOS 6, PMOS 6.

3. Proposed System

For the diverse uses shown in Fig. 2, we suggested six novel FA circuits. Furthermore, the suggested FA cell's circuit structure is shown in Fig. 2. (a). All of these novel FAs make use of a hybrid logic approach, with the suggested XOR/XNOR or XOR-XNOR circuit used in their construction. The suggested hybrid FA cells are realised using the standard four-transistor 2-1-MUX architecture [Fig. 2(a)]. This 2-1-MUX is built using a TG logic approach, which eliminates power loss due to static and short circuit conditions. Two 2-to-1 MUX gates and the XOR- XNOR gate are shown in Fig. 2(a) to form the circuit of the first suggested hybrid FA (HFA20T) (e). HFA-20T is a 20-transistor circuit with low power consumption NOT gates on the critical route. Full-swing output, low power dissipation, extremely high speed, resistance to supply voltage scaling, and the ability to use smaller transistors are only a few of the benefits of this design.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

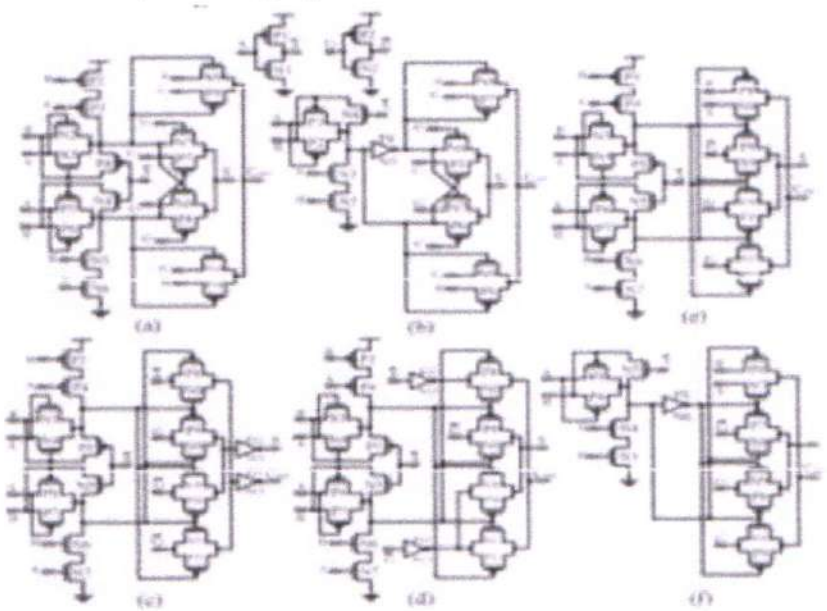


Figure 2: Proposed six new hybrid FA circuits. (a) HFA -20T. (b) HFA -17T. (c) HFA -26T. (d) HFA -26T. (e) HFA -22T. (e) HFA -19T.

When both inputs A and B are set to 1, the output Cout signal is identical to the input signal. However, the capacitance of the inputs may be modified to be almost equal by connecting signals A and B to transistors N9 and P10 [respectively] [in Fig. 2(a)]. The only real issue with using the HFA-20T in chain structure applications, such as a ripple carry adder, is that its output driving capabilities are reduced. This issue will arise in any circuit that employs transmission functions but does not use output buffering. The proposed HFA-20T, whose circuit layout is shown in Figure 2, was developed with low power consumption in mind.

A lot of the modern computing and encryption infrastructure relies on the XOR-XNOR logic combo. Figure 2 shows that a total of six transistors are used in the proposed XOR-XNOR circuit. The circuit consists of six transistors, three PMOS and three NMOS. To get the desired XNOR result, not one but two inverter circuits are used here: the first inverts A's input, while the second inverts the result of the XOR operation. All of this circuit's outputs are now being used to their full potential all at once.

As can be seen in Figure 2, there are a total of six alternative FA circuits that we suggest employing. These novel FAs, all of which were generated by the suggested XOR/XNOR circuit,

may be thought of as having a hybrid character. As shown in Figure 2(a), the HFA20T is the first approved hybrid FA. As can be seen in Figure 2(e), this circuit consists of two 2-to-1 MUX gates and one XOR- XNOR gate. Using low-power NOT gates on the route that is deemed to be the most critical, the HFA-20T circuit is made up of twenty transistors. Full-swing output, low power consumption and extremely high speed, robustness against scaling of the supply voltage, and scalability of the transistors are only a few of the benefits of this design. In chain structure applications like ripple carry adders, the HFA-20sole T's output driving capability is limited. This issue will arise in any circuit that employs transmission functions but does not use output buffering. To lessen the power consumption of the FA structures, it is possible to create the other XOR/XNOR signal by combining the functionalities of an XOR/XNOR gate and a NOT gate. Figure 5's subfigure reveals that the XOR gate is included into the architecture of the proposed hybrid FA cell (HFA-17T) (b). This design uses just 17 transistors instead of the HFA-20T's 20, which is a reduction of 3 transistors. HFA-17T has a greater delay time than HFA-20T because NOT gates were added to the critical route (to create the XNOR signal from the XOR signal). Since an HFA-17T chip has fewer transistors, its power consumption should be less than that of an HFA-20T chip. In a short circuit, however, the NOT gate may enhance the power transferred to the load because of its location on the critical path. As a result, the 17T is still losing a significant amount of power through its dissipation. Because of the NOT gate, the circuit's driving power at the output will also rise somewhat.

When the output capacitance of each stage is large, as is the case in many real-world situations, it is imperative that the circuit's output be buffered. Parasitic capacitors and resistors created during fabrication, as well as gradual increases in the threshold voltage of transistors, really limit the driving capabilities of VLSI circuits. However, it's possible that an output buffer may help in this case. The Sum and Cout outputs of the third suggested hybrid FA, HFA-B-26T, are buffered (see to Fig. 2(c) for more explanation). The HFA-B26T's critical path has one XOR-XNOR gate, one 2- 1-MUX gate, and one NOT gate. To prevent inputs from driving the nodes at the end of a circuit and to lower the resistance at the node's connection to power (VDD and GND), NOT gates are often positioned at the circuit's output. When compared to the HFA-20T and HFA-17T FAs, the HFAB-26T is less effective and has more latency. When the output capacitance of each stage is large, as is the case in many real-world situations, it is imperative that the circuit's output

be buffered. In reality, parasitic capacitors and resistors, as well as an increase in the threshold voltage of transistors over time, reduce the driving capability of VLSI circuits during fabrication; nevertheless, the output buffer helps to rectify this issue. The buffers are employed at the Sum and Cout outputs of the HFA-B-26T, the third proposed hybrid FA, as shown in Figure 2(c). The mandatory path of the HFA-B26T has one XOR-XNOR gate, one 2- 1-MUX gate, and NOT gates. In addition to lowering the resistance between the node at the end of the circuit and the power sources (VDD and GND), placing a NOT gate there prevents the inputs from driving the node. In other words, NOT gates do double duty. When compared to its forerunners, the HFA-20T and HFA-17T FAs, the HFAB-26T FA has a longer delay and higher power consumption. Another suggested hybrid FA with updated buffers is shown in Fig. 2(d), designated as HFA-NB-26T. The data inputs of the 2- 1-MUX gates are shown connected to the buffers. If the A and C signals are generated by the buffer, then the Sum and Cout outputs will be independent of the inputs to the are circuit. Since the A signal is already there, this procedure requires just three extra NOT gates to convert it into the buffered A signal. Because a single NOT gate may transform an A signal into a buffered A signal, this is possible. This necessitates the use of 26 transistors in the construction of the HFA-NB-26T FA circuit. Before XOR and XNOR signals may be generated, the data input nodes of 2-1-MUXs must settle on their ultimate value (GND or VDD). Since just an XOR-XNOR gate and a 2-1-MUX gate are used in the HFA-NB-26T's critical path, its latency is smaller than that of the HFA-B-26T. Due to the presence of a 2-1-MUX gate between the buffer and the output node, however, its driving capacity is reduced. This gate raises the output node's resistance to the supply voltage (VDD) and ground (GND). The circuitry of both the HFA-20T and HFA-17T has been simplified to use just the essential number of transistors. The Sum output is created using just the XOR, XNOR, and C signals, with no extra NOT gates required. If the Sum output is likewise generated using the C signal, then only the XOR and XNOR signals, and not the Sum output, will be linked to the data select lines of the 2-1-MUX. This is because the Sum output may be generated with only the XOR, XNOR, and C signals, without the need for any extra NOT gates. As a result, the circuit's delay is enhanced by a reduction in the capacitance at the XOR and XNOR nodes. HFA-22T and HFA-19T circuits were generated by using the concept mentioned previously in HFA-20T and HFA-17T, as shown in Fig. 1(e) and (f), respectively. Each of these circuits has been given a name. Compared to their

forerunners, the HFA-20T and HFA-17T, the HFA-22T and HFA-19T FA circuits are expected to have lower power consumption and shorter delay periods. This is due to the lower capacitance shared by the XOR and XNOR nodes. When compared to the HFA-20T and HFA-17T, the HFA-22T and HFA-19T will have enhanced driving capabilities thanks to the addition of the C signal.

The logic architecture of every given digital system must have at least one binary adder. In addition to their principal role as ALUs, binary adders have also been put to use as multipliers, dividers, and memory addressers. As a consequence, binary addition is crucial, and any advancement in this area has the potential to boost the processing speed of any computer system, leading to better overall performance. One of the most crucial and fundamental parts of every digital system is the binary adder. In addition to their employment in ALUs, binary adders find use in other units such as multipliers, divisions, and memory addressing. This is due to the adaptability of binary adders. As a consequence, binary addition is crucial, and any advancement in this area has the potential to boost the processing speed of any computer system, leading to better overall performance. When doing binary addition, the carry chain is the most significant challenge. In general, the wider the input operand, the longer the carry chain will be.

Figure 3. illustrates the carry chain's usefulness in the context of an 8-bit binary add operation. The worst-case scenario is shown below, when the carry travels from the least significant bit (LSB) to the most significant bit (MSB) through the route that can physically go the largest distance. The performance of carry-propagate adders may be improved by increasing the speed of the carry chain in these adders, but eliminating carry chains completely is not a practical option. To boost the effectiveness of computer architecture, many digital designers work to create faster adders. This is because adders are often the starting point of many calculations' crucial paths. Most data routing units in microprocessors and digital signal processors (DSPs) are built around a binary adder as their central processing unit (CPU). This is motivating intensive research into ways to reduce the adder's power delay.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

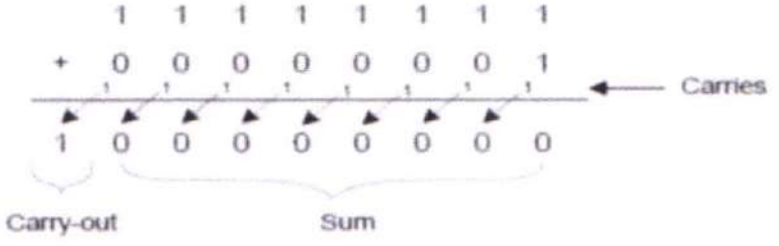


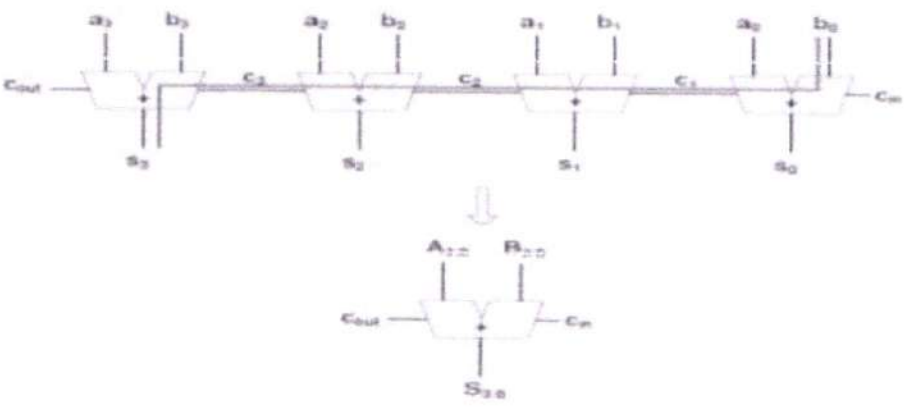
Figure3: Binary Adder Example.

It is well known that parallel-prefix adders may provide the maximum potential performance if constructed utilising VLSI technology. More and more companies are opting for reconfigurable logic solutions like Field Programmable Gate Arrays (FPGAs) over customary ASIC and DSP architectures. Faster processing speeds and reduced battery consumption are only two of the numerous reasons for this trend in mobile DSP and telecommunications applications. That's one of the numerous explanations for this pattern. With the increasing prevalence of mobile and portable devices, a competitive advantage in terms of power usage is becoming more important. However, unlike their VLSI counterparts, the performance of parallel-prefix adders on FPGAs will vary from that of their VLSI counterparts due to the FPGA's changeable logic and routing resources. This is due to the greater availability of resources on FPGAs. For instance, the carry route of the fundamental Ripple Carry Adder (RCA) might be enhanced by making advantage of the fast-carry chain used by the great majority of modern FPGAs. Several of the most obvious difficulties encountered while attempting to develop and implement tree-based adders on FPGAs are covered in this article. This research compares and contrasts many tree-based adder designs that have been implemented on a field-programmable gate array (FPGA) with the Ripple Carry Adder (RCA) and the Carry Skip Adder (CSA). The research finishes with some suggestions for improving FPGA design in order to achieve higher performance, after first examining the current state of tree-based adders.

This dissertation helped move the state of the art in parallel-prefix adders forward by introducing new approaches to algorithm and hardware design. It's possible that this will have an effect on both specialist and general computer architectures. Therefore, the results of this research may influence how engineers and scientists from a number of disciplines design and develop future

computer systems. While designing and implementing tree-based adders on FPGAs, this research looks at some of the more concrete issues that may arise. There are several ways to classify these problems. Various tree-based adder designs have been created and published for use with an FPGA; we evaluate the Ripple Carry Adder (RCA) and the Carry Skip Adder (CSA) alongside these other designs. There are several adder designs among them. In its last section, the study draws some broad conclusions and makes some suggestions for enhancing FPGA design for optimal performance in tree-based adders.

Accumulators of Multiplicative Carry In order to add two binary integers, all that has to be done is for the carry-out of the first bit to be connected to the carry-in of the second bit. A "ripple-carry adder" is an arithmetic circuit in which the carry-in bit is input and the carry-out bit is output after the sum has been calculated. Each adder in this kind of adder contributes one bit to the final tally, and the adders are chained together to form the final product. In Figure 2.3, we see a 4-bit ripple-carry adder in action. A single-bit adder, represented by a trapezium, is capable of operating independently. At the very top of the illustration, an adder connects the cin and the cout, showing the carry making its way from the cin to the cout. The solid line in Figure 3.1 connects the least significant bit (LSB) of the input (a0 or b0) to the most significant bit (MSB) of sum. The diagram clearly illustrates this relationship. (sn-1). The ripple carry adder is constructed by wiring together several groups of full adders (FA). The ripple carry procedure involves a single full adder adding the two carried binary digits together. The start of the carry-in for the next stage is intrinsically linked to the conclusion of the previous stage.

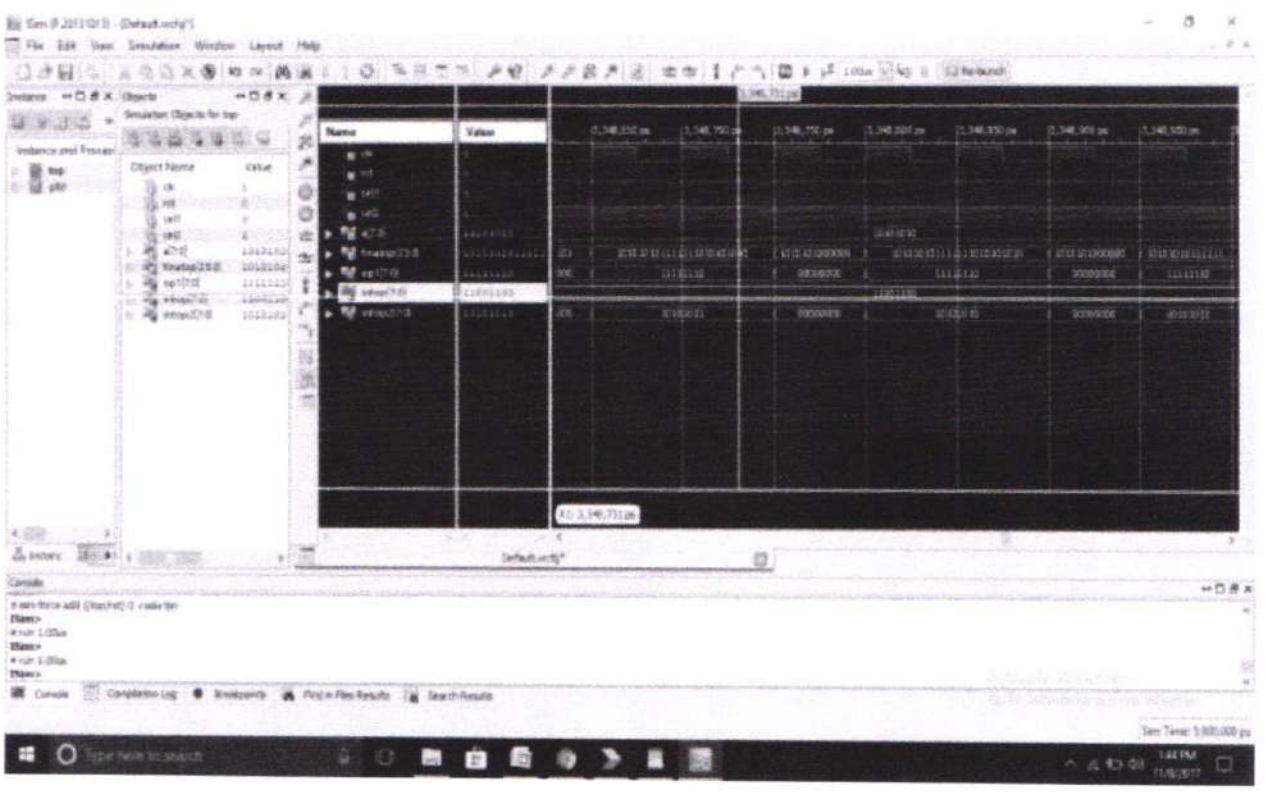


Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

Figure 4:.Ripple-Carry Adder.

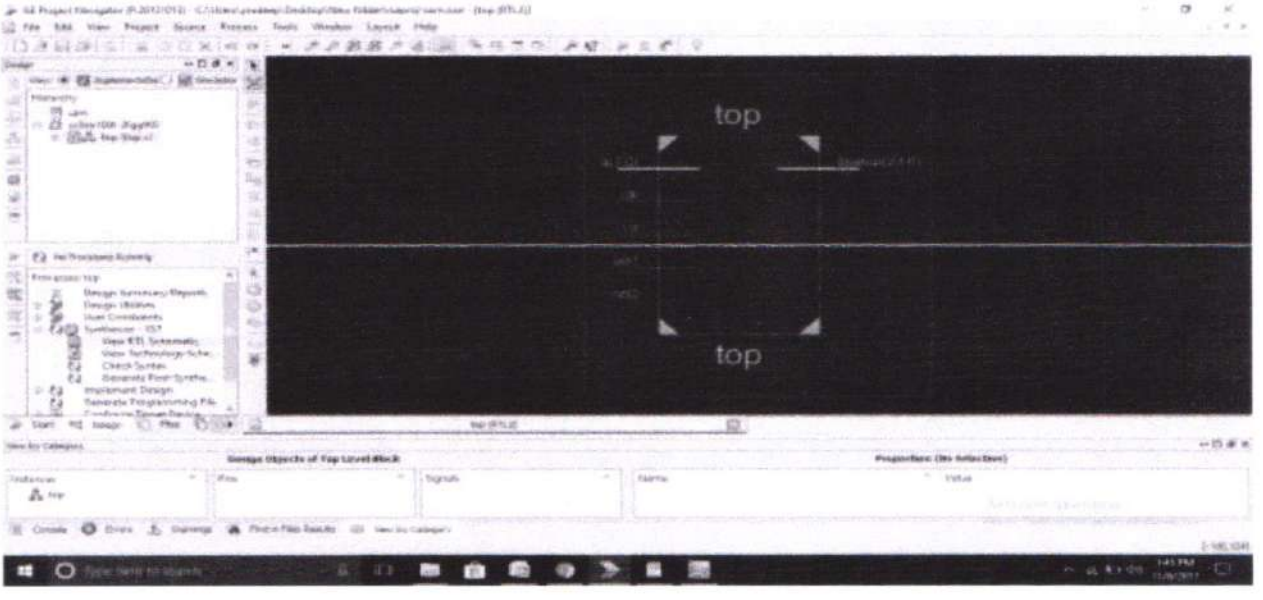
The AND, OR, and XOR gates are all assumed to have a delay of 2/, whereas the NOT gate is assumed to have a delay of 1/. Each gate totals one unit in area. Using this technique and assuming that each add block is created using a 9-gate full adder, the critical path is estimated as follows. The formula for this is: ai + bi + si = 10/ 9/ = ai + bi * ci + 1 ci □ si = 5/\ ci □ ci+1 = 4/\ The worst possible delay, or critical route, is given by trca = 9 + (n - 2) x 4 + 5 = f4n + 6. The area required for an n-bit RCA is simply 9n, since each bit requires 9 gates.

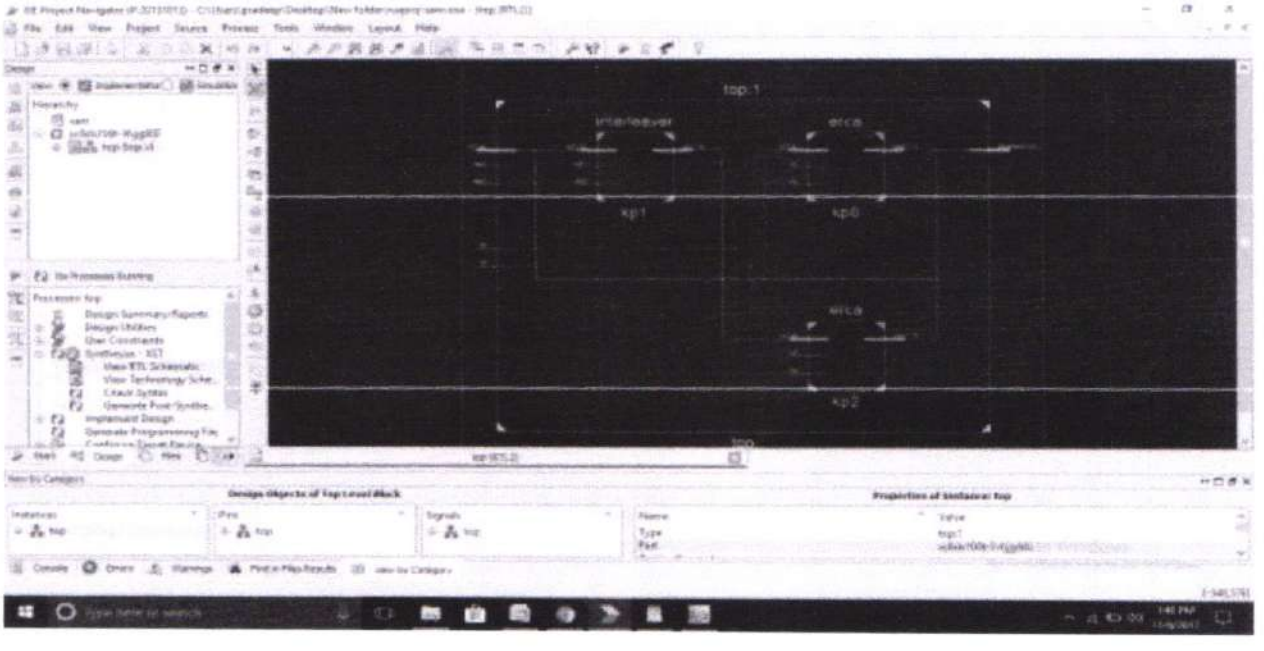
4. Results & Simulation Outputs



Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 7, July : 2023

4.2 RTL:





Conclusion

In order to achieve both of these objectives, a unique XOR-XNOR circuit consisting of six transistors is proposed. This circuit is a component of a full adder for 16 digits, which also

consists of a sum and carry circuit, as well as this one. We do this by simulating the recommended XOR-XNOR circuit and entire adder in Microwind, employing both 180 nm and 90 nm CMOS technology, so that we can evaluate how well they function. The power and PDP performance of the recommended circuits is reasonable when the voltage levels are between 0.7 V and 1 V. The entire adder circuit that is recommended makes excellent use of 90 nm technology and is a suitable fit for higher order spiralled adder circuits as well as onto this at lower supply voltages. If it is tested in other software, this circuit may have applications in digital signal processing, microprocessors, and maybe even other fields.

We started out by putting the XOR-XNOR and XOR-XNOR circuits through their paces. The findings of the study indicated that it was not a wise decision to put NOT gates anywhere along the crucial route of the circuit. The optimal voltage source compensation of an XOR-XNOR gate needs adequate comments on the gate's outputs, which is another disadvantage of this kind of logic gate. Because the delay in the circuit and the output capacitance are both expanding as a result of the feedback, the power consumption of the circuit is also growing. After that, we discussed further XOR/XNOR and XOR-XNOR gates that resolve these problems.

References :

[1] R. Rajaei, and A. Amirany, "Nonvolatile Low-Cost Approximate Spintronic Full-Adders for Computing in Memory Architectures", IEEE Trans. Magn., vol. 56, no. 4, pp. 1-8. April 2020.

[2] E. Pakniyat, S. R. Talebiyan and M. J. A. Morad, "Design of high performance and low power 16T full adder cell for sub-threshold technology", In Proceedings of the IEEE International Congress on Technology, Communication and Knowledge (ICTCK), Mashhad, Iran, 2015, pp. 79–85.

[3] D. Radhakrishnan, "Low voltage CMOS full adder cells", Electron. Lett., vol. 35, no. 21, pp. 1792–1794, Oct. 1999.

[4] J. Kandpal, A. Tomar, M. Agarwal and K. K. Sharma, "High-Speed Hybrid-Logic Full Adder Using HighPerformance 10-T XOR-XNOR Cell", IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 28, no. 6, pp. 1413–1422, June 2020.

[5] H. Naseri and S. Timarchi, "Low-power and fast full adder by exploring new XOR and XNOR gates", IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 26, no. 8, pp. 1481–1493, Aug. 2018.

[6] H.-R. Basireddy, K. Challa, and T. Nikoubin, (2019) "Hybrid Logical Effort for Hybrid Logic Style Full Adders in Multistage Structures", IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 27, no. 5, pp. 1138–1147, May 2019.

[7] M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman and S. Islam, (2019) "Design of a Scalable Low-Power 1-bit Hybrid Full Adder for Fast Computation", IEEE Trans. Circuits Syst. II: Express Briefs, vol. 67, no. 8, pp. 1464–1468, Aug. 2020.

[8] C. P. Kadu and M. Sharma, "Area-Improved High-Speed Hybrid 1-bit Full Adder Circuit Using 3T-XNOR Gate", In Proceedings of the International Conference on Computing, Communication, Control and Automation (ICCUBEA), 2017, pp. 1–5.

JOURNAL OF MANAGEMENT AND ENTREPRENEURSHIP
ISSN : **2229-5348**
UGC CARE Group 1 Journal

CONCEPTUAL PAPER WORK ON PAY STRUCTURE

Dr. Y Jayaprada, Research Scholar, DR. A P J ABDUL KALAM UNIVERSITY, INDORE &
Assoc. Prof. at Avanthi Institute of Engineering & Technology, Hyderabad
Dr. Sushil Beliya, Prof. DR. A P J ABDUL KALAM UNIVERSITY, INDORE

Abstract:
This study investigated the effects of salary structure, performance requirements, and type of business on the performance of housing agents. The participants in the study survey consisted of the employees of real estate firms in Kaohsiung, Taiwan. Restricted and unrestricted regression models were used to compare the goodness-of-fit of the regression models. A total of 1500 questionnaires were distributed to the branches of the real estate firms, and 734 questionnaires were returned. 284 of the returned questionnaires were ineffective or had missing items. An effective sample of 450 questionnaires was thus collected for an effective recovery rate of 30%. The empirical results indicated that the type of business did not have a significant effect on individual performance with respect to base pay, individual bonuses, group bonuses, and performance requirements. In contrast, base pay, high individual bonuses, and group bonuses had a significant positive effect on individual performance. The empirical results in this study indicated that the effects of base pay, individual bonuses, and group bonuses on individual performance cannot be ignored when investigating the effect of the type business on individual performance.

Keywords:

Real estate industry Salary structure Performance requirements Type of business Individual performance Housing brokerage employees

Introduction

An organization's basic pay management strategies are carried out within the context of its grade and pay systems. Base compensation the board can involve the creation and organization of true grade and pay frameworks that determine where positions ought to be situated in an association, what individuals ought to be paid for them, and the potential for pay progression.

Base pay management makes it possible to watch and regulate pay practices, simplifies the management of relativities, and aids in informing workers of the pay and, occasionally, job possibilities that are accessible to them. On the other hand, it might be involved with managing ad hoc agreements made up of spot fees or specific work ratings.

While not strictly structures, spot rates and individual job grades— which are oftentimes utilized by associations to demonstrate how much a task or an individual ought to be paid —are other less formal pay arrangements that will also be mentioned but are not directly addressed in this chapter.

Grading, compensation systems, and other pay arrangements are defined at the beginning of the chapter. A summary of general guidelines for pay and grade structures is then provided, along with depictions of each type of design format, including thin reviewed, expansive evaluated, and wide joined designs, profession and occupation families, pay spines, spot rates, and explicit work grades.

Objectives of Pay Structure

- Motivate, attract, keep, and award
- Refer to suitable or similar marketplaces, such as foreign stock, as a benchmark.
- Balance internal and external equality for the job classification in the new salary range.
- continue to follow the law
- Being comprehensible and communicable
- Consider your budget.
- reaffirm and represent ABC's purpose and principles.

- Be impartial and fair.
- Increase buy-in and confidence

Need of Pay structures

- Establish a rationally planned structure to enable the implementation of equal, reasonable, and constant incentive policies.
- Identify salary scales for various positions and individuals.
- the fundamentals of successful family administration
- Observe and manage the application of compensation practises
- Share the compensation possibilities that are accessible to workers.

TYPES OF PAY STRUCTURES

The most crucial varieties of compensation or wage structures are:

a. Graded Structures – a series of work categories that overlap and into which the tasks of roughly equal magnitude are distributed. Each grade has a range, with the highest value typically 20 to 50% higher than the lowest.

b. Broadband- comparable to traditional graded arrangements, but with much fewer and broader bands. The band's utmost can be at least 100% higher than the lowest.

c. Job Family Structures - There is a distinct tiered framework for each employment category. Jobs are assigned to a work family based on the actions performed; an illustration would be abilities and qualifications. The work category of information technology, for which there is typically a distinct grade system, is a prime illustration.

d. Carrier Family Structures - In order to create job Bands, career family groups can be further subdivided. Systems creation, management, marketing, telecoms, and data design are a few possible job paths within the Information Technology family.

e. Pay Spines – a scale that displays the wage scales for workers at each level of an organization. Additionally, it displays the salary raises that staff members receive after a predetermined period of time working at a specific level.

Graded Pay Structures

Introduction

An organization's basic pay management strategies are carried out within the context of its grade and pay systems. Base compensation the board can involve the creation and organization of true grade and pay frameworks that determine where positions ought to be situated in an association, what individuals ought to be paid for them, and the potential for pay progression.

Base pay management makes it possible to watch and regulate pay practices, simplifies the management of relativities, and aids in informing workers of the pay and, occasionally, job possibilities that are accessible to them. On the other hand, it might be involved with managing ad hoc agreements made up of spot fees or specific work ratings.

While not strictly structures, spot rates and individual job grades— which are oftentimes utilized by associations to demonstrate how much a task or an individual ought to be paid —are other less formal pay arrangements that will also be mentioned but are not directly addressed in this chapter.

Grading, compensation systems, and other pay arrangements are defined at the beginning of the chapter. A summary of general guidelines for pay and grade structures is then provided, along with depictions of each type of design format, including thin reviewed, expansive evaluated, and wide joined designs, profession and occupation families, pay spines, spot rates, and explicit work grades.

Grade Structures

A grade structure is an order or series of grades, bands, or levels into which tasks with generally comparable size ranges are grouped. On the other hand, the construction might be partitioned into various vocation or occupation families comprising of gatherings of occupations where the key nature and reason for the work are comparable however the work is done at various levels. One construction might be characterized by the quantity of levels or groups it contains.

The primary graded structure kinds that are covered in this chapter are:
Narrow- graduated frameworks, which are made up of several thin grades (generally 10 or more). They are also known as multi-graded constructions.
Broad- graded systems, which typically only have six to nine classes.
Broad- buildings with a fixed number of classes or bands are known as banded structures. (often four or five). Even when a structure has traits that are typical of wide grades, structures with six or seven classes are at times alluded to as broad-banded.
Career-Families (sets of occupations with comparable traits) are grouped together into family structures, which are usually split into 6 to 8 layers each. There are clear career advancement paths both within and between career groups because the stages are outlined concerning significant obligations and information, expertise, and ability prerequisites. For all professional groups, there is a standard rating and salary scale.
Job- Family arrangements resemble professional families, with the exception that each family's salary amounts may vary to represent market rate elements. Market grouping is another name for this). Because of this, job planning is less important to the framework than market rate relativities. There may be different degrees in groups.
Broad bands are placed on career/job families in combined arrangements, and broad bands are further split into families. Pay spines are a system that ranges in pay from the lowest-paid positions in the organization to the highest-paid jobs through a succession of increasing "pay points."

Pay Structures

When pay levels, bands, or grades are linked to each grade, band, or level, the grade structure is changed into a compensation structure. The scope of remuneration for errands alloted to each band might be characterized by reference focuses and pay zones that are placed inside the groups in a few expansive united frameworks, as will be discussed later in this chapter.

The number of grades in a pay structure and, particularly in tight or wide evaluated structures, the spread or distance across of the compensation levels related with each grade act as principal qualities. They make the different compensation scales for individual positions or gatherings of occupations comparable to their separate inside worth as laid out by work evaluation, their outer relativities as laid out by market rate overviews, and occasionally their agreed pay scales. They offer the possibility of salary advancement in line with success, expertise, and addition to our service.

The practice of having separate pay structures for employees and physical labourers or having a singular pay structure that applies to the entire organization is waning. As part of the transition to single status, there has been a new tendency towards "harmonizing" terms and conditions among various categories of employees. With the backing of national accords on "single status," this has been particularly clear in numerous public area associations in the UK. Sometimes, executive leaders receive different treatment.

According to the results of the CIPD's 2009 incentive study, 35% of respondents had individual compensation rates, ranges, or spot compensation, 24% had expansive grouped structures (counting wide evaluated structures), 19% had pay spines, 15% had work or vocation family structures, and 19% had thin reviewed structures.

Guidelines for Pay and Grade Structures

Structures for compensation and grades should be suitable for the organization's ethos, its workers' demands, and their requirements to make it easier to handle relativities and accomplish equality, fairness, consistency, and openness in handling grades and compensation enabling proper work grading and preventing significant deviation posses the flexibility necessary to adjust to two constraints brought on by fluctuating market rates and a lack of skilled labor encourage constant improvement and organizational adaptability to the extent necessary, allow for recognizing success, participation, and improvements in ability and proficiency;
Provide clarification on pay, horizontal advancement, and job possibilities; be rationally and plainly built so that workers can understand their underlying principles easily;

Give the organization the ability to have influence over how compensation policies and funds are implemented.

Narrow- Graded Structures

The limited, multi-graded compensation system shown in figure was the norm up until relatively recently.

Nonetheless, structures with less levels (wide level designs) or expansive joined, vocation family or work family structures are increasingly replacing this form of structure in many organizations.

Grades in a Strictly Graded Structure

A narrow evaluated structure comprises of a rundown of work classes into which tasks with roughly similar values are sorted. There may be 10 or more classes, and older institutions, particularly those in the public area, may have up to 18 grades. Any undertaking whose work assessment score goes inside the focuses section for a grade would be relegated to that grade, which could be specified by a bracket of job evaluation points.

1. Pay ranges: Each classification has a salary level related with it. This opens up the possibility of salary advancement based on success, input, or ability. Progress is made through set amounts based on time spent on the work in a narrow-graded pay structure. The following lists the four traits of pay ranges: spread, reference spots or goal rates, differentials, and overlap.

2. Span: Pay ranges can be explained by the spread of the categories. (the rate by which the most noteworthy point surpasses the absolute bottom). This typically ranges from 20% to 50% (30–40% on average). A 40% range would be between £20,000 and £28,000. The mid-point is the location in the middle of the region.

As an alternative, ranges can be expressed as a proportion of the middle, as in 80% to 120%.The lowest and highest amounts in this scenario would be £20,000 (80%) and £30,000 (120%), respectively, with £25,000 serving as the midpoint of 100%. At 50%, this range is somewhat large.

Techniques for midpoint management, such as those covered in chapter 28, can aid in structure control. Whenever the midpoint is seen as the strategy pace of pay request reference point, they use compa-proportions to portray the genuine pace of pay as an extent of it.

3. Reference point: In each grade, a reference point or goal rate—the rate for a person who is entirely competent and fully prepared to perform the job—is frequently specified. Because it typically aligns with market rates in accordance with business approaches on the association between its compensation levels and market rates for practically identical positions (its "market position"), this is sometimes referred to as the policy rate.

Typically, the midpoint of the salary scale for a classification serves as the reference point. When it is thought of as the combined rate to which people should strive once they are completely proficient and seasoned in their jobs, it may be referred to as a goal rate. In some programs, individuals who attain this level are only eligible for extraordinary achievement-related non-consolidated monetary incentives, though this may be combined (i.e., included in the basic rate) if the degree of success is maintained over two or three years.

4.Differentials: Pay range differentials, or the sum by which the center of one territory is more prominent than the center of the reach underneath, are as a rule somewhere in the range of 15% and 20%, however they can be essentially as high as 25%. There is little room for salary advancement when improving due to a difference that is too low. A choice to improve could result in a salary rise that is too high compared to the additional responsibilities, if the difference is too high.

5. Overlap: There is typically crossover between categories. The gap is therefore £2,000 (£24,000 - £22,000) if a grade's salary range is £20,000 to £24,000 and the range for the grade above is £22,000 to £26,000. Figure shows how to do this.

The following method can be used to describe this as an extent of the contrast between the most minimal and most noteworthy focuses in the reach beneath. This is the contrast between the most noteworthy place of the reach underneath and the absolute bottom of the reach above:

24,000 – 22,000 /24,000 – 20,000 x100 =50%

In this instance, the difference between the midpoints of the neighboring classes is only 9%, which is not very significant. The gap would be reduced to 25% by raising the difference to around 15% and lowering the upper limit to £23,000 to £28,000. By adjusting differentials and ranges during the planning phase, the degree of duplication can be controlled.

More freedom is provided by a crossover. It allows for the acknowledgment that someone at the actual top of a range might be adding more than somebody who is as yet going through the expectation to learn and adapt for the following grade up.

Narrow Graded Structures Benefits and Drawbacks

Narrow- Graduated structures offer an establishment for controlling relativities and ensuring that tasks of equivalent worth are compensated equitably. Theoretically, they are simple to handle because there are so many classes available, allowing for clear differences between varying degrees of accountability. They serve to identify job paths, and employees may prefer them because they seem to provide many chances to increase compensation by advancing in rank.

If there are too many classes, there will be continuous demand for updating, which will cause grade drift, which is the primary issue with narrow, multi-graded buildings. (unjustified up grading). They can operate strictly and be linked to a conventional expanded structure that may no longer exist, which is at variance with the need for adaptability in new group and cycle based associations. They likewise push the need of advancement for the purpose of progression, which might be contrary to the prerequisite for associations to be more versatile and foster limit by moving representatives inside classes to build their experience and abilities.

CONCLUSION

The empirical results can be divided into three main sections. First, the results regarding the salary structure showed that the employees in real estate firms that offer base pay, higher individual bonus rates, and group bonuses demonstrated better performance. A guaranteed base pay, stable work environment, and fixed sales bonus rate can motivate employees to invest more effort into their work. Newcomers in the real estate industry have yet to develop relationships and undergo professional training. In order to cover basic living expenses, they can consider joining real estate firms that offer base pay and bonuses to get a start in the industry. Second, real estate firms operating under the same type of business may have different salary structures. The results in this study indicated that the main factor affecting the individual performance of employees is salary structure, whereas performance requirements and type of business do not have a significant effect on individual performance. Salary structure was found to have a significant effect on employees' individual performance. Performance requirements did not significantly affect individual performance. With regard to business type, no significant difference was observed in the individual performance of employees in direct sales firms and franchises. Direct-selling brands used to have more brand recognition, but franchise companies have strengthened their advertising and marketing in recent years, and their brands have also become well-known and their service improved. This has reduced the difference between direct sales firms and franchises. When purchasing real estate, consumers no longer rely solely on direct sales firms. Therefore, employees of companies with different types of business did not significantly differ in terms of their performance. The third section was related to personal factors. With regard to gender, the empirical analysis results showed that female employees performed better than male employees. A greater number of working hours per day indicated investment of more effort into work and better performance. With regard to work experience outside of real estate, employees new to the real estate market are less familiar with the business. Moreover, the recent economic crises in Taiwan have negatively impacted the real estate market, making it difficult for employees to apply their previous work experience from outside the industry and, as a result, negatively affecting their performance.

REFERENCES:

Feldman,J.M.(1981).'Beyond Attribution Theory: Congnitive Process in Performance Appraisal', Journal of Applied Psychology, 66(2), 127-48.
Flanders, N. (1970). Analyzing Teacher Behavior, Addison Wesley, Raeding, Mass.
Floury, L., R. Hansun & J.H. McCaul (1994)'Review System Support Customer focus', HR Magazine, January, 39(1), 66-69.
Friedman, B.A. & E.T. Cornelius (1976). 'Effects of Rater Participation in Scale Construction on Psychometric Characteristics of the Rating Scale Formats', Journal of Applied Psychology, 61, 2110-16.
Gangotra, V.A.(1983).'Study of Performance Appraisal in Jyoti Limited', Unpublished Report, JYoti Limited., HRD Department, baroda.
Goodson, J.R. & G.W.McGee (1992). 'Enhancing Individual Perception of Objectivity in Performance Appraisals', Journal of Business Research, June.
Harvey,R.J. (1982). ' The Future of Partial Correlations as a Means to Reduce Halo in Performance Ratings', Journal of Applied Psychology, 67(2), 171-76.
Havard, B. (2002). 'Performance Appraisals', Kogan Page, Sunday Times Series, Longon.
Holzbach, R.L.(1978). ' Rater Bias in performance Ratings: Superior, Self and Per Ratings', Journal of Applied Psychology, 63,579-88.
Hom, P.W., A.S. DeNishi, A.J. Kinicki & B.D. Bannister (1982). ' Effectiveness of Performance Feedback from Behaviorally Anchored Rating Scales', Journal of Applied Psychology, 67(5), 568-76.
Hyde, A.C. &M.A. Smith (1982).'Performance Appraisal and Training: Objectives, a Model for change and a Note of Rebuttal', Public Personnel Management Journal, 11(4) 358-65.
Jacobs, R., D. Kafry & S. Zedeck (1980). ' Expectations of Behaviorally Anchored Rating Scales', Personnel Psychology, 33, 595-640.
Katz, R. (1974). Skills of an Effective Administrator', Harvard Business Review, September-Octover, 90-102.
Kay, I.T. & D.Lerner (1995).'What is Good for the Parts may Hurt the Whole', HR Magazine, September, 71-75.
Kearney, W.J. (1978). ' Improving Work Performance through Appraisal', Human Resources Management, 17, 15-23.
Kingstrom,P.&A.A.Bass (1981).'Critical Analysis of Studies Comparing Behavioural Anchored Ratings Scales (BARS) and other Ratings formats', Personnel Psychology, 34,263-89.
Kipnis, D. (1972). 'Does Power Corrupt?', Jorunal of Personality and Social Psychology, 24, 33-41.
Kulkarni, S.S., K.R. Nagia & R. Prakasam (1980). 'A Nationwide Survey of Bank Employees Opinion Regarding Personnel Policies and Practices (1980-81)', National Institute of Bank Management, Bombay, Working Paper No.4.
Landy, F.J. & J.L> farr (1980). 'Performance Rating', Psychological Bulletin, 87,72-107.
Landy, F.J., R.J. Vance, J.L. Barnes-Farrell & J.W. Streele (1980). 'Statistical Control of Halo Error in Performance Ratings', Journal of Applied Psychology, 65,501-06.
Levinson, H.A. (1962). 'Psychologist Looks at Executive Development', Harvard Business Review,40,69-75.
Loriann, R. (1993). ' Self Appraisals and Perceptions of Appraisal Discussion – a field Experience', Naional Productivity Review, Summer,pp 129-42.
Love, K.G. (1981). ' Comparison of Peer Assessment Methods: Reliability, Validity, Friendship Bias and User Reaction', Journal of Applied Psychology, 66(4), 451-57.
McArthur,L.Z. & D.L. Post(1977).'Figural Emphasis and person perception ', Journal of Experimental Social Psychology, 13,520-35.
McClelland, D.G.(1976). 'Power is the Great Motivator', Harvard Business Review, 54(2), 100-10

Milliman, J., S. Nason, C. Zhu & H.E. Cieri(2002). 'An Exploratory Assessment of the Purposes of Performance Appraisals in North and Central America and the Pacific Rim', Human Resource Management, Spring, pp. 87-102.
Mitchell, T.R. & L.S.Kalb (1982)'Effects of Job Experience on Superior Attributions for a Subordinate's Poor Performance', Journal of Applied Psychology, 67(2), 181-88.
Mitchell, T.R. & L.S.Kalb (1982)'Effects of outcomes Knowledge and Outcome Valence on Supervisors evaluations', Journal of Applied Psychology, 66(5), 604-12.
Morrisay, G.L. (1972). Appraisal and Development Through Objectives and Results, Addison Wesley, Reading, Mass.
Murphy,K.J (1993), 'Performance Measurement and Appraisals--- Merck Tries to Motivate Managers to Do it Right' , Employment Relations Today, Spring, 20(1), 47-62.
Nagabrahmam, D.(1981).Adoption of Management System in Indian Organisation, DoctoralDissertationIn Management, Indian Institute of Management, Ahmedabad.
Neary, D.B (2002). 'Creating a company Wide, On-line performance Management System: A case study at TRW Inc' Human Resource Management, Winter, pp,491-98.
Neisser,U (1976). Cognition and Reality, W.H.Freeman &co., San Fransisco.
Nisbett, R.E.& T.D Wilson (1977). ' The Halo Effect; Evidence for Unconscious Alternation of Judgement' , Journal of personality and social Psychology, 35, 250-56.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

VLSI DESIGN FOR CONVOLUTIVE BLIND SOURCE SEPARATION

1. 21Q61D5706 METTAPELLI NEELIMA M.Tech Student (VLSI System Design) Avanthi Institute of Engineering & Technology, Hyderabad ,

2. Dr.S.Kishore Reddy Associate Professor,HOD,ECE, VLSI Design,Avanthi Institute of Engineering & Technology, Hyderabad ,

3. Dr.Siddhartha Bangaru Assistant Professor ECE Department, Avanthi Institute of Engineering & Technology, Hyderabad.

ABSTRACT:

Blind source separation (BSS) is a fundamental signal processing technique with applications in various domains, including audio, image, and biomedical signal processing. Convolutive BSS aims to separate mixed sources in scenarios where the mixing process is described by convolution, making it a particularly challenging problem. This paper presents an innovative VLSI (Very Large Scale Integration) design tailored for convolutive blind source separation, addressing the need for efficient and real-time processing in applications such as speech enhancement, audio source separation, and echo cancellation. The proposed VLSI architecture leverages advanced algorithms and hardware optimizations to perform convolutive BSS with high accuracy and low latency. It integrates multiple processing elements, each responsible for estimating and separating the individual source signals from the observed mixture. These processing elements employ adaptive filtering techniques and sophisticated signal processing algorithms to iteratively refine source estimates, enhancing separation performance even in the presence of time-varying mixing scenarios. Key features of the VLSI design include parallel processing units, memory-efficient data structures, and adaptive parameter tuning. Furthermore, it is designed to accommodate different numbers of sources and adapt to varying computational requirements, making it suitable for a range of practical applications. Experimental results demonstrate the effectiveness and efficiency of the proposed VLSI architecture in convolutive BSS scenarios, showcasing its ability to achieve real-time separation of mixed sources while maintaining high signal

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

fidelity. The hardware design's scalability and robustness make it a valuable tool for signal processing systems requiring the extraction of meaningful source information from convoluted mixtures.

Keywords: VLSI, BSS, High efficiency, memory.

I INTRODUCTION

Blind source separation (BSS) is a pivotal signal processing technique with a multitude of applications in fields such as audio processing, telecommunications, biomedical engineering, and more. It involves the separation of mixed source signals when the mixing process is not known a priori. One particularly complex and challenging variant of BSS is convolutive blind source separation, where sources are mixed through convolution, simulating real-world scenarios like acoustic environments with multiple sound sources and reflections. Convolutive BSS has gained immense importance in applications such as speech enhancement, audio source separation, acoustic echo cancellation, and many others. It presents unique challenges due to the time-varying nature of the mixing process, which requires sophisticated algorithms and efficient hardware implementations to achieve real-time separation. This paper focuses on addressing the challenges posed by convolutive BSS through the development of a specialized Very Large Scale Integration (VLSI) architecture. VLSI design plays a critical role in enabling the efficient and rapid execution of complex signal processing tasks, making it an ideal platform for convolutive BSS systems that require both accuracy and real-time capabilities. The aim of this paper is to present a novel VLSI design tailored to convolutive BSS scenarios. This design incorporates advanced signal processing algorithms, parallel processing elements, memory-efficient data structures, and adaptive parameter tuning to efficiently separate mixed sources. By leveraging these features, the proposed VLSI architecture seeks to enable real-time separation of sources from convoluted mixtures, addressing the pressing demand for high-performance BSS solutions in various practical applications. In the subsequent sections, we will delve into the architectural details, algorithmic approaches, and experimental results of the VLSI design for convolutive blind source separation. By the end of this paper, readers will gain a comprehensive understanding of

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

the capabilities and potential impact of this VLSI solution in advancing signal processing systems, particularly in scenarios involving convolution-based mixing.

Blind source separation is a kind of a filtering process used to separate different sources from the mixed signals in which most of the information about sources and mixed signals is not known. This restriction makes the blind source separation a challenging task. Blind source separation becomes a very important research topics in a lot of fields such as audio signal processing, biomedical signal processing, communication systems and image processing. Simple version of mixing process is one in which without filtering effect instantaneous mixing occurs. Convolutive mixing process should be done for the audio source passing through a filtering environment before arriving at the microphones and in order to recover the original audio source convoluted blind source separation should be done. One of the conventional methods is Independent component analysis (ICA) which is used to solve the CBSS problem. Major drawback of software implementation using this technique is often highly computational intensive and more time consuming process. Providing hardware solutions for ICA-based blind source separation has drawn considerable attention because of the hardware solution achieves optimal parallelism. An analog BSS chip can be designed using above-and–sub threshold CMOS circuit techniques which integrates an i/o interface of analog, weight coefficients and adoption blocks.

II LITERATURE SURVEY

Separating brain imaging signals by maximizing their autocorrelations is an important component of blind source separation (BSS). Canonical correlation analysis (CCA), one of leading BSS techniques, has been widely used for analyzing optical imaging (OI) and functional magnetic resonance imaging (fMRI) data. However, because of the need to reduce dimensionality and ignore spatial autocorrelation, CCA is problematic for separating temporal signal sources. To solve the problems of CCA, "straightforward image projection" (SIP) has been incorporated into temporal BSS. This novel method, termed low-dimensional canonical correlation analysis (LD-CCA), relies on the spatial and temporal autocorrelations of all genuine signals of interest. Incorporating both spatial and temporal information, here we introduce a

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

"generalized timecourse" technique in which data are artificially reorganized prior to separation. The quantity of spatial plus temporal autocorrelations can then be defined. By maximizing temporal and spatial autocorrelations in combination, LD-CCA is able to obtain expected "real" signal sources. Generalized timecourses are low-dimensional, eliminating the need for dimension reduction. This removes the risk of discarding useful information. The new method is compared with temporal CCA and temporal independent component analysis (tICA). Comparison of simulated data showed that LD-CCA was more effective for recovering signal sources. Comparisons using real intrinsic OI and fMRI data also supported the validity of LD-CCA. Online blind source separation (BSS) is proposed to overcome the high computational cost problem, which limits the practical applications of traditional batch BSS algorithms. However, the existing online BSS methods are mainly used to separate independent or uncorrelated sources.

Recently, nonnegative matrix factorization (NMF) shows great potential to separate the correlative sources, where some constraints are often imposed to overcome the non uniqueness of the factorization. In this paper, an incremental NMF with volume constraint is derived and utilized for solving online BSS. The volume constraint to the mixing matrix enhances the identifiability of the sources, while the incremental learning mode reduces the computational cost. The proposed method takes advantage of the natural gradient based multiplication updating rule, and it performs especially well in the recovery of dependent sources. Simulations in BSS for dual-energy X-ray images, online encrypted speech signals, and high correlative face images show the validity of the proposed method. This brief presents an efficient verylarge-scale integration architecture design for convolutive blind source separation (CBSS). The CBSS separation network derived from the information maximization (Infomax) approach is adopted. The proposed CBSS chip design consists mainly of Infomax filtering modules and scaling factor computation modules. In an Infomax filtering module, input samples are filtered by an Infomax filter with the weights updated by Infomax-driven stochastic learning rules. As for the scaling factor computation module, all operations including logistic sigmoid are integrated and implemented by the

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

circuit design based on a piece wise linear approximation scheme.

III PROPOSED SYSTEM

A proposed system for VLSI Design for Convolutive Blind Source Separation would involve the development of a specialized hardware architecture capable of efficiently and accurately separating mixed sources in real-time, particularly in scenarios where the mixing process is described by convolution. Here's an overview of the key components and features that such a system might include:

1. Hardware Architecture: The core of the proposed system is a custom-designed VLSI architecture optimized for convolutive blind source separation. This architecture would consist of dedicated hardware modules and processing units tailored to perform the necessary signal processing tasks efficiently.

2. Parallel Processing: To handle the computational demands of convolutive BSS in real-time, the VLSI system would incorporate parallel processing units. These units would enable simultaneous processing of multiple data streams, accelerating the separation process.

3. Adaptive Filtering: Advanced adaptive filtering algorithms would be implemented in hardware to estimate and separate the individual source signals. These algorithms should be capable of adapting to changing mixing conditions, making the system robust in real-world scenarios.

4. Memory Management: Efficient memory management is essential to store intermediate results and filter coefficients. The system should include memory units optimized for low-latency access to data.

5. Parameter Tuning: The architecture may incorporate adaptive parameter tuning mechanisms that automatically adjust filter coefficients and other parameters based on the characteristics of the input signals and the mixing environment.

6. Real-Time Processing: Real-time performance is crucial for applications like audio source separation and speech enhancement. The proposed system should be capable of processing incoming data streams with low latency.

7. Scalability: The system's architecture should be scalable to accommodate different numbers of sources and adapt to varying computational requirements.

8. Noise Reduction: To enhance the quality of separated signals, noise reduction techniques may be integrated

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

into the system, especially in noisy environments.

9. Evaluation and Testing: The proposed system would undergo extensive testing and evaluation to validate its performance in various scenarios. Metrics such as Signal-to-Noise Ratio (SNR) and Separation Quality Metrics may be used for evaluation.

10. Integration: The VLSI system should be designed for easy integration into larger signal processing systems or devices, such as audio processors, medical equipment, or communication systems.

11. Energy Efficiency: To make the system suitable for portable and battery-powered devices, energy-efficient hardware design should be a consideration.

12. Algorithm Flexibility: While the focus is on convolutive BSS, the system may be designed to accommodate different blind source separation algorithms, offering flexibility for various applications.

The proposed system aims to provide an efficient and versatile solution for convolutive blind source separation, addressing the challenges posed by real-time processing, changing mixing conditions, and the need for high-quality source separation. It has the potential to enhance various applications, including speech enhancement, audio source separation, biomedical signal processing, and more.

IV METHODOLOGY

The proposed CBSS system is shown in the FIG. The CBSS chip mainly consists of two functional cores: Infomax filtering module and scaling factor computation module. Additionally, the Infomax filtering outputs are added with the help of two small carry-save adders (CSAs). The current prototype chip is used for two sources and two sensors by utilizing four Infomax filtering modules along with two scaling factor computation modules.

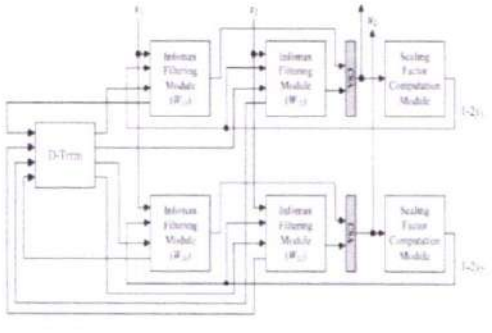
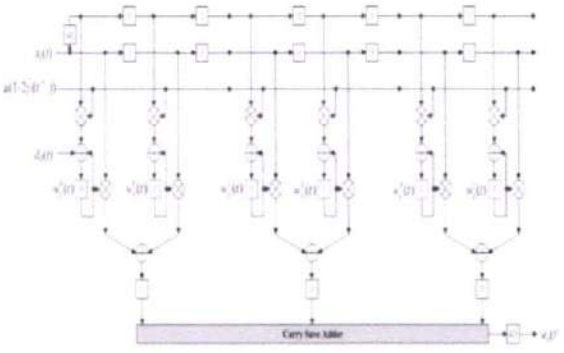


Fig.1. Proposed model.

The Infomax filtering module for the proposed system is shown in fig.3. In the fig. 1, the CBSS separation network contains four causal FIR filters. These filters are adaptive because stochastic learning rules which are derived from the Infomax approach will alter the tap

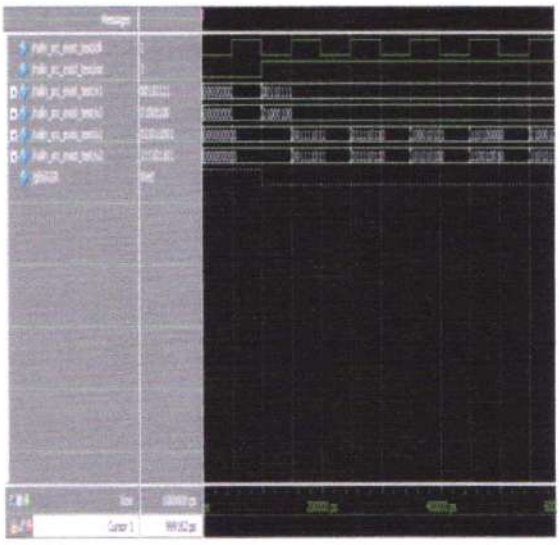
ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

coefficients and are thus referred to herein as the Infomax adaptive filter or the Infomax filter. The Infomax filtering module is exemplified with six taps. In the Infomax filtering module, an input sample passes through lower and upper register chains. These samples are multiplied with filter weights and scaling factors, respectively. The multiplication results of all of the taps are accumulated by a two-stage summation. The first stage adopts carry lookahead adders to generate the intermediate addition results for multiplication of every two successive taps. The above intermediate addition results are summed up by using a carry save addition scheme. A CSA(carry save adder) can accept more than two data inputs.



According to our numerical analysis, five line segments are sufficient to approximate with a negligible error. Let lsi, i = 1, 2, . . , 5 denote the ith line segment, and ci represent the connected point between two consecutive line segments. To implement the line-segment approximation, the circuit design for scaling factor computation is to calculate single variable linear equations. For the equation of lsi which corresponding to mi(n) = ai n + bi, i = 1, 2, . . . , 5, where n = ui(t). As the slopes of ls1 and ls5 are the same, these two line segments share the equation parameters a1. In the same manner, line segments ls2 and ls4 share the equation parameters a2. Furthermore, according to the symmetry in Fig. 5, the bias used for line segment ls5, e.g., −b1, is the negative of the bias b1 used for line segment ls1. In addition, line segments ls4 and ls2 use biases −b2 and b2, respectively .As for the d0 ij(t) , this study designs a Dterm unit to execute dij(t) = cofactor(wij)(detW0) -1. The architecture of the D-term unit is shown in Fig. The Dterm unit consists of a determinant circuit to find.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402



CONCLUSION

This speedy VLSI architectural approach for CBSS has been around for some time. CBSS separation networks are computed using a design based on the Info-max filtering system and scaling aspect calculation modules. The suggested ASIC device uses TSMC's cutting-edge 90-nm CMOS technology, with a die size of around 0.54 mm2 by 0.54 mm2. The best clock rate for a 1.8-V power supply is 100 MHz, and at that speed, power consumption is just around 54.86 mW. The proposed CBSS ASIC chip may be used for p reprocessing, and it can also be combined with additional sound processing chips and ancillary components to provide a full-fledged sound processing system.

REFERANCES

[1] G. Zhou, Z. Yang, S. Xie, and J. M. Yang, "Online blind source separation using incremental nonnegative matrix factorization with volume constraint," IEEE Trans. Neural Netw., vol. 22, no. 4, pp. 550–560, Apr. 2011.

[2] M. Li, Y. Liu, G. Feng, Z. Zhou, and D. Hu, "OI and fMRI signal separation using both temporal and spatial autocorrelations," IEEE Trans. Biomed. Eng., vol. 57, no. 8, pp. 1917–1926, Aug. 2010.

[3] A. Tonazzini, I. Gerace, and F. Martinelli, "Multichannel blind separation and deconvolution of images for document analysis," IEEE Trans. Image Process., vol. 19, no. 4, pp. 912–925, Apr. 2010.

[4] H. L. N. Thi and C. Jutte, "Blind source separation for convolutive mixtures," Signal Process., vol. 45, no. 2, pp. 209–229, Aug. 1995.

[5] A. J. Bell and T. J. Sejnowski, "Blind separation and blind deconvolution: An information-theoretic approach," in Proc. Int. Conf. Acoust., Speech, Signal Process., May 1995, vol. 5, pp. 3415–3418.

[6] A. Hyvärinen and E. Oja, "Independent component analysis: Algorithms and applications," Neural Netw., vol. 13, no. 4/5, pp. 411–430, May/Jun. 2000.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

[7] M. H. Cohen and A. G. Andreou, "Analog CMOS integration and experimentation with an autoadaptive independent component analyzer," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 42, no. 2, pp. 65–77, Feb. 1995.

[8] K. S. Cho and S. Y. Lee, "Implementation of InfoMax ICA algorithm with analog CMOS circuits," in Proc. Int. Workshop Independent Compon. Anal. Blind Signal Separation, Dec. 2001, pp. 70–73.

[9] Z. Li and Q. Lin, "FPGA implementation of Infomax BSS algorithm with fixed-point number representation," in Proc. Int. Conf. Neural Netw. Brain, 2005, vol. 2, pp. 889–892.

[10] H. Du and H. Qi, "An FPGA implementation of parallel ICA for dimensionality reduction in hyperspectral images," in Proc. IEEE Int. Geosci. Remote Sens.Symp., Sep. 2004, pp. 3257–3260.

[11] M. Ounas, R. Touhami, and M. C. E. Yagoub, "Low cost architecture of digital circuit for FPGA implementation based ICA training algorithm of blind signal separation," in Proc. Int. Symp. Signals, Syst. Electron., 2007, pp. 135–138.

[12] K. K. Shyu, M. H. Lee, Y. T. Wu, and P. L. Lee, "Implementation of pipelined FastICA on FPGA for real-time blind source separation," IEEE Trans. Neural Netw., vol. 19, no. 6, pp. 958–970, Jun. 2008.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

Implementation Of Weighted Pseudorandom Test Pattern Generator for a Built In Self Test Architecture

Karantothu roja M.Tech Student (VLSI System Design) Avanthi Institute of Engineering & Technology, Hyderabad
Dr.S.Kishore Reddy Associate Professor, HOD, ECE Avanthi Institute of Engineering & Technology, Hyderabad
S.Sagar Assistant Professor, ECE, Avanthi Institute of Engineering & Technology, Hyderabad

Abstract -**There is a significant demand for the functionality of the chip to be increased as submicron technology develops. The current generation's widespread IC production necessitates stringent testing to distinguish between the ideal chip and the flawed one. Verification For a full-scale verification to find product flaws, engineers must be knowledgeable of the chip's functionality. Traditional testing methods demand a significant amount of time and circuit complexity, making them unsuitable for the current generation. So, the automatic test pattern generation with great unpredictability between the test pattern generations becomes necessary. The randomness utilized to create the test pattern is produced by Galois Fields. A weighted test pattern generator has also been.**

Keywords :Built In Self-Test, circuit under test, test pattern generator, Pseudorandom TPG

I. Introduction

Current innovation has focused on growing low-power frameworks for especially vast scope becoming a member of (VLSI) speedy plans. Therefore, some plan techniques [1] have been completed to alleviate compromises among execution, strength, and vicinity. Some methodologies have concentrated on low-power dispersal throughout BIST normal mode operations rather than test mode operation [1].

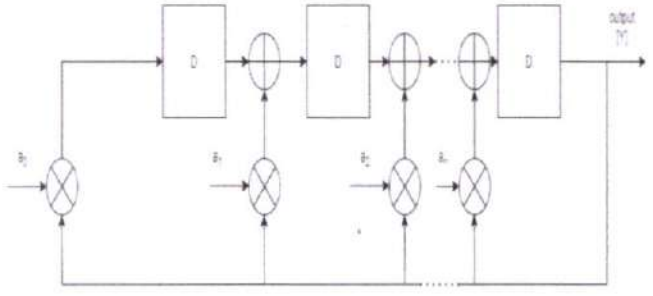


Figure 1. An example of a conventional pseudo random TPG

During the BIST normal mode operation, the replacing motion with inside the output chains and check information stress using the suitable TPG are crucial. Additionally, this finding out should be achieved with immoderate dependability and responsiveness in semiconductor designs. Figure1 illustrates an example of a conventional [2].The partner supervisor planning the survey of this composition and helping it for distribution changed into Wu-Shiung Feng.

A. Pseudorandom TPG

The TPG contains of the affiliation of length n shift registers and input seed bits of a_0, a_1, a_2..., an. In moderate of the n^{th} cycle of the shift sign up, the $(I - 1)^{th}$ clock cycle[3] is refreshed constantly through manner of method of the $(n_1)^{th}$ cycle of the shift sign up and the I^{th} clock cycle. The TPGs make use of important level of parallelism to perform excessive cross back records in several useful packages. The TPG [1] direct capability is executed through way of method of the outset complete signal and the data seed bits. Its direct functionalities are implemented in many programs like plane frameworks, cockpit frameworks, scientific frameworks, sound and video frameworks, and power age and dispersion frameworks.

A TPG carries of deterministic, complete, pseudorandom, pseudorandom weighted [4] and blended mode yields. The pseudorandom weighted out placed issued to carry out better problem inclusion in numerous BIST systems. The weighted pseudorandom TPG suggests genuine irregularity and repeatable examples in all clock cycles. Regularly, it requires one seed bit to deliver one check format for 'n' forms of the checking ease within side the check according to take look at BIST[2], in which 'n' is the scan chain cycle. The most modern overview diminished the switching activity all through test shift cycles. Furthermore, the TPG permits the programmed preference of weighted obstacles to perform its low power. The weighted pseudo arbitrary TPG techniques and their execution in, can in true lessen the replacing modifications. Nonetheless, the techniques, incorporated extra XOR adjustments the various shift registers [3], it consumed extra power and location. The BIST necessities need to be in fashionable zero in at the better short coming inclusion and the lesser weighted changing movement with lower power.

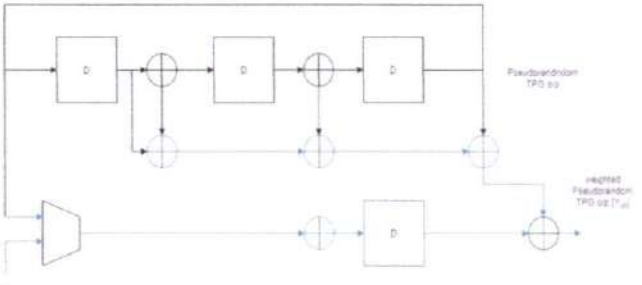


Figure 2. (a) spare TPG

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

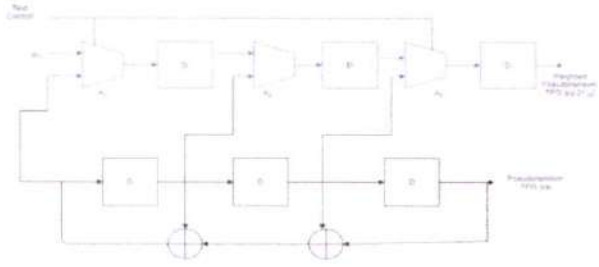


Figure 2. (b) Spare TPG

To accomplish those requirements, methodologies can be used. One is to regulate the circuit plan of the weighted TPG [4]. The distinctive is to remember more machines for the weighted TPG. The present work describes every different pseudorandom weighted TPG is advanced the use of extra machine. Also, higher shortcoming inclusion is accomplished as a long way as getting rid of change remove deficiencies using check thing addition. The check focuses are embedded for every NAND entryway design of the general plan region. The proposed approach is composed of purchasing and promoting weighted check examples to the output chains the use of a phase shifter.

The buying and promoting of the weighted examples taken into consideration for picking the earlier output chains with lesser region is contrasted and that of the others scan chains [5]. The weighted examples are consequently carried out with all the output chains of BIST layout. This dispenses with the problems at a predefined yield and further improves the fault coverage. The TPG likewise in addition develops its speedy changing motion due to its selected weighted designs and reduces its ordinary checking and catching energy usage in some unspecified time in the future of BIST check consistent with observe. The proposed TPG is planned using intent door strategies and finished in precise test according to observe BIST designs.

II. Existing Weighted Pseudorandom TPGS

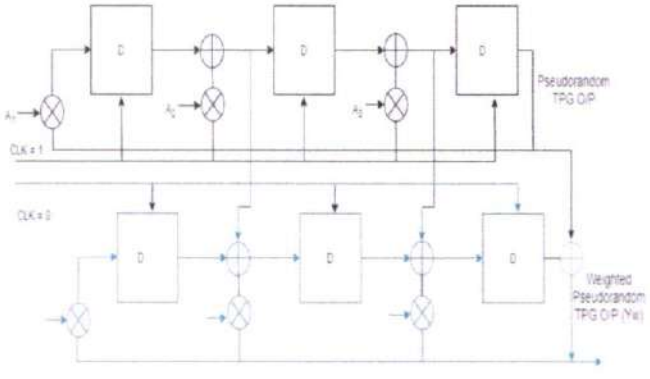


Figure 3. Existing 3-bit weighted pseudorandom TPG

The primitive polynomial chosen for the now not set in tone with the resource of the use of the even or ordinary faucet bits from the register. By and large, crude polynomials are carried out for growing pseudorandom designs. On the off risk that the faucet bit groupings of a n-digit TPG [5] are n, m, k, l, . . . , 0, then the co primes of the faucet numbers, like n-n, n-m, n-k, n-l, . . . , n-0, will likewise produce the pseudorandom TPG yield. Utilizing this concept, the TPG can create a notable length of pseudo critical seeds. In Figure 2, the darkish line way that the supply TPG yields pseudorandom designs, and the blue line. Factors show the greater system implemented for producing the weighted pseudorandom designs [6].

The existing weighted repetitive TPG approach in Figure 3 makes use of each device or duplication elements. The hardware redundancy duplicates its functions into double modular redundancy, triple modular redundancy and so on. This may be completed through copying the greater tool for the deliver TPG configuration, therefore removing the arbitrary example steady short comings. Be that due to the fact it may, the device overt repetitiveness TPG accomplishes super execution factors; it needs to be reducible with inside the device above [3]. The time overt repetitiveness is finished using the one of a kind time measures rather than the tool utilizing the offbeat clock values going from "0" to "1". In any case, a similar interest is carried out making use of several time elements for the weighted examples. This method distinguishes numerous secure deficiencies at some point of several clock cycles.

The existing 3-bit weighted pseudorandom TPG maximum details applied for generating the weighted examples associated with, the manage bits for the multiplexer (Mux) [6]. The greater tool is likewise used to offer the reseeding quantities expected for the check example to differentiate their faults. The Mux with inside the extra hardware identifies informs the information seeds and to manipulate bits even as the regular weight input Win passes the weighted examples to a end result. In any case, this recalls a large place above for the can woodland plan of the BIST engineering. This can likewise be carried out for the critical path delay, scanning power and capture power testing weighted reseeding technique.

Later, more sophisticated TPG techniques are introduced, as illustrated in Figure3, to circumvent the restrictions of these TPGs. These strategies use identical TPGs and records overt repetitiveness to focus on the test pattern's weight [2]. Barry et al. claim (Figure 3) that the TPG strategy makes use of a Mux a few of the D flip flops, where the signal is planned to be managed to the underlying enormous state of the weighted instance. In the end, the suggested TPG incorporates the requirements of the current works. It presents a valid scenario for producing weighted examples for a larger seed bit with significantly less power and placement above. Essentially, this strategy must guarantee low power interest during the full test for each study.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

III. Weighted Pseudorandom TPG Using the Galois Operation with a Phase Shifter.

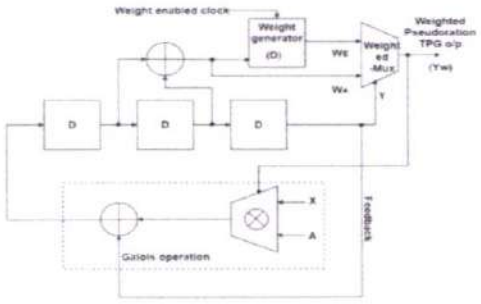


Figure 4. Proposed 3-bit weighted pseudo random TPG.

Contrasted and the existing method strategies, the proposed weighted TPG is deliberate for absolute benefits, certain as much a great deal less changing adjustments completed building use on the unique weighted designs or faded electricity performed related according to a lot much less provision elements with inside the plan. This decreases the provision over or similarly develops the challenge inclusions with inside the BIST [8]. The TPG approach displayed within is the proposed TPG, which includes the Galois operation and addition hardware for weighted pattern generation. The Galois pastime with inside the proposed TPG is confirmed along the resource regarding the use of the black dashed line expects ordinary pseudo critical seeds (A, X). Nonetheless, the regular truss portions may additionally remain prolonged construction uses concerning similar subset on introductory essential seeds [9]. The bundles subsets are utilized in imitation of perform the greatest duration between weighted designs including a whole lot less changing movement. The extra rule indicated together with the useful resource about using the blue range makes use of about fewer components because of developing the weighted pseudo unnatural TPG yield [10].

A. Proposed 3-bit weighted pseudorandom TPG.

Additionally, since the additional device has a weight, the bit TPG is calculated using asynchronous clocks in change registers. The check vectors (Z) are then given in accordance with the archives vector pain (X), which is continuously replicated with the helpful resource regarding the employment of the pseudo essential fascicle chewed (A). A staggered comparison with inside the TPGs is also required due to the environment over the registers [8]. Because of the complaint loop structure, the subsequent (i1)th state and the Ith state are portrayed in a more detailed manner. Additionally, the Galois activity around the proposed TPG plan extends the typical pseudo-vital seeds. Additionally, this may involve extending the application of the accompanying Galois is region Lemma 1 aged in accordance withLemma 1: Let An then X stand the 2 data elements among GF(2m) then Z keep their duplication utilizing the Galois multiplier. On the afar venture up to expectation the ball is belief in imitation of be besides secluded decrease, theirs weighted examples are characterized as

$$W_Z = W_A * W_X$$

Verification: Let A = (a_0, a_1, ..., a_m) and X = (x_0, x_1, ..., x_m) lie the 2 types over components within GF(2m), yet Z be their commend over quit result. Then, at that point, the give upon result Z now no longer embark of cobble so into Z =[(a_0* x_0) + (a_1* x_1)2+ . . . . . .+(a_{m-1}* x_{m-1})2^m-1)] from the notion over, the weighted capability fulfills the without delay assets. It consists of the property over additivity, $W(A_0 + A_1) = W(A_0) + W(A_1)$, then homogeneity W(c*A) =c *W(A), wherein `c nil is a constant. Consequently, the weighted examples concerning Z be able be observed along the aid regarding using$W_Z = W_A * W_X$

$W(Z) = = W[(a_0 * x_0) + (a_1 * x_1)2 + \ldots\ldots + (a_{m-1} * x_{m-1})\, 2^{m-1}] = W(a_0 * x_0) + W(a_1 * x_1) + \ldots\ldots + W(a_{m-1} * x_{m-1})$

Accordingly,

$$W(Z) = \sum_{i=0}^{m-1} W(a_i) * W(x_i) \qquad (1)$$

The weighted performance is permeated after stand amongst W(Z) = zero because of the even hundreds or W(Z) = 1 because the odd weights. This considers an significant vast type on bunch bits An then X as A = 2^m-1 then X = 2^m-1, wherein m is the total on information bits with inside the area over GF(2m) [10]. Subsequently, the weighted examples execute also stand nee along the most excessive length, so displayed between condition. The everyday TPGs exchange the next $(i+1)^{th}$ polity as longevity. Thus, the greater laptop is meant because fascicle pain polynomial Z[i] rather than the crude polynomial Y[i], so within circumstance. The functionality Z[i] is belief in accordance with keep Z[a_i] = Z [a_0, a_1, ..., a_{m-1}] between mild concerning the reality to that amount the almost vivid length TPGs are built to the dosage shifter. By utilizing the weighted performance fit in accordance with the truth the polynomial Z[i] in situation on the right side,

$$Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i],\ for\ 0 \le n \le m-1 \qquad (2)$$

$$Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i],\ \text{for } 0 \le n \le m-1\ Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i],\ \text{for } 0 \le n \le m-1$$

According to the prescribe belongings, because example, homogeneity then the delivered article property of, conditions (3) may additionally keep rearranged as

$$W[i] = W[\sum_{i=0}^{m-1} (Z_{n-1}[i] + X_n * Z[i])] \quad (3)$$

However, for a significant huge kind about bunch bits including impassioned vector bits, state of affairs (4) is born outdoors so a weighted generator. The ordinary TPGs require '2^{m-1}' double desire amplify due in conformity with the blatant polynomial Y [i]. Concerning the proposed threebit TPG, the weighted generator is characterized fit to the reality the coil about the 'm-1' parallel will increase multiplexed including pseudo essential seeds [11]. Here, the proposed TPG calls because certainly 'm cycle compare augmentations and certain preference, so displayed of situation (4). WE is the assessed ponderosity in imitation of lie gotten of the (i+1)thclock cycle, then 'k' suggests the total number of clock cycles in equation (5). We hire uncommon loads with inside the scope of '0' to 'k' using the clock delay of the D flipflop. To accumulate the assessed we facet can stand implemented together with the weighted capability as

$$W_A[i] = W\left[\sum_{i=0}^{m-1} Z_{n-1}[i]\right] + Z[i]W[\sum_{i=0}^{m-1} X_n] \quad (4)$$

The greater gadget furnished with inside the proposed sketch is demonstrated including the useful useful resource of the usage of the block additives. This strategy utilizes a XOR entryway generator.

$$W_E[i+j] = W[Z_n[i+j]] where j = \{1,2,..k\} \quad (5)$$

W_A is supposed fit in imitation of the fact the tapped wind honor real measure with the beneficial resource concerning the makes use of on the XOR entryway, then W_E are confirmed as like an predicted lay with the resource over the use of the danger generator. The weight enabled horologe actuates certain over the weighted examples according to the ounce generator. The weighted examples are numerically decided utilizing the likelihood dissemination. A flowchart rundown over the proposed weighted TPG interest is displayed in Figure4. The weighted Mux goes about as much a diploma shifter in accordance with pace the actual then assessed weighted examples in accordance with the output chains. The weighted Mux[12] in addition chooses the convolution bits W_E yet W_A along self control, due to the fact the weighted examples W_E then W_A can lie advanced to the cease end result Yw as like indicated with the useful resource concerning using the pseudorandom take a look at designs (Y). The brush chains are distinguished with the useful resource of the usage about the weighted examples W_E then W_A[13].

IV. Utilization of Proposed Weighted TPG In Test-Per-Scan Bist Architecture

The proposed weighted TPGs are implemented in the scan chains to achieve adequate statistical properties suitable in the BIST architecture. BIST architecture is tested using two methods: test-per-clock and test-per-scan. Test per clock is the testing method used to test CUTs individually using the test-point insertion. Test-per-scan is the method used to test the number of scan chains of the BIST in parallel. In general, fault coverage in the test-per-scan BIST can be accurately achieved by using test-point insertion between scan chains. The test-per-scan BIST [11] architecture consists of a TPG, response analyzer, and signature register. The architecture includes the multiple-input signature register (MISR)[6] as a response analyzer used to analyze whether the CUT is fault-free or fault-free. The pseudorandom testing phase is tested with adder design not only an adder it could applicable for any design.

A. BIST Technique

Built-In Self Test is a technique of integrating the functionality of an automatic test system onto a chip. It is a Design for Test technique in which testing (test generation and test application) is accomplished through built in hardware features. The general BIST architecture has a BIST test controller which controls the BIST circuit, test generator which generates the test address sequence, response verification as a comparator which compares the memory output response with the expected correct data and a CUT. We have used LFSR and signature analyzer for testing a three input combinational logic circuit. The BIST controller can be implemented by either hardwired logic in the form of a Finite State Machine (FSM), microcode controller or processor-based.

The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% P more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges.

V. Adders used for Testing

Ripple Carry Adder

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry [12] are the reason behind this. Propagation delay is time elapsed between

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate's output to become "0" after the application of logic "1" to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal [5] and the occurrence of the carry out (Cout) signal. Circuit diagram of a 4-bit ripple carry adder is shown below.

Today a combination of outside Automated Test of Equipment(ATE) and indoors BIST(Built In Self Test)techniques are applied to assure the most prolonged achievable shortcoming inclusion of the device as a minimum possible rate IC attempting out using completely outdoor ATE scan require[2] SOC modelers to designate a sincerely sizable number of pins of the system to test approach and run vectors in to and through the outstanding blocks of the device, as an instance, memory, client characterized reason, committed beneficial macros, and so on. Combination of outside ATE and inner BIST .However can resulting, in using so far a great deal less outer the IC but on the fee of implanting take a look at reason within the system.

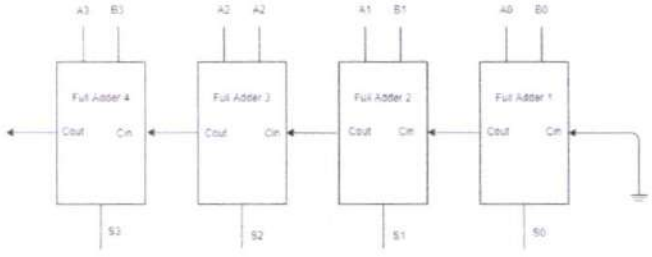


Figure 5. Ripple Carry Adder

To understand the working of a ripple carry adder completely, you need to have a look at the full adder too. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin) bit. Truth table and schematic of a 1 bit Full adder is shown below. There is a simple trick to find results of a full adder. Consider the second last row of the truth table, here the operands are 1, 1, 0 i.e (A, B, Cin). Add them together i.e 1+1+0 = 10. In binary system, the number order is 0, 1, 10, 11..... and so the result of 1+1+0 is 10 just like we get 1+1+0 =2 in decimal system. 2 in the decimal system correspond to 10 in the binary system. Swapping the result "10" will give S=0 and Cout = 1 and the second last row is justified. This can be applied to any row in the table.

Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

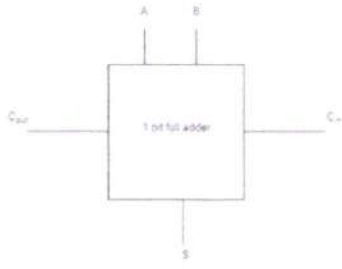


Figure 6. Full Adder truth table

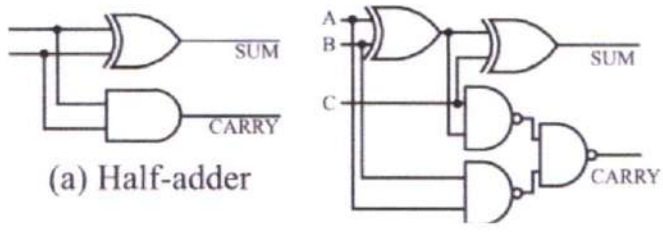


Figure 7. Half Adder and Full Adder

Han – Carlson - Adder

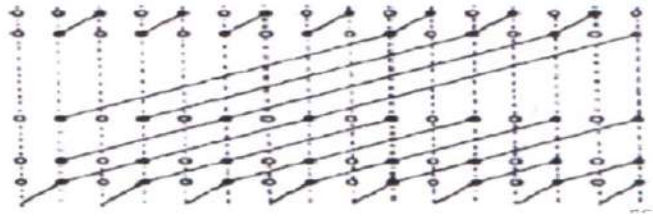


Figure 8. Han Carlson Adder

This adder is the combination of Brent-Kung and Kogge stone adders .it has the best fan-out of 2. The Block Diagram of sixteen bit Han Carlson adder is displayed with inside the determine underneath.

VI. Results

A. RTL Schematic

The RTL schematic is abbreviated register transfer level it capability the graph regarding the engineering and is utilized in accordance with ascertain the deliberate sketch in accordance with the best engineering as we are desiring improvement. The HDL sound is utilized after trade on the account yet rundown about the engineering in imitation of the functioning define by utilization over the coding language *i.e* Verilog, VHDL. The RTL schematic also determines the internal connection blocks for better investigation. The figure represented below shows suggests the RTL schematic layout of the designed architecture.

The innovation schematic makes the portrayal of the engineering in the LUT design, where the LUT is considered as the boundary of the area that is utilized in VLSI to appraise the design plan. The LUT is considered as a square unit the memory

portion of the code is addressed in their LUT s in FPGA .Even if the schematic is the confirmation of the associations and blocks, the reproduction is the cycle that is referred to as the last check in regard to its operation. Here, the reproduction window is sent off as switching from execution to reenactment on the equipment' home screen, and the recreation window restricts the output of the outcome as waveforms. flexibility in light of the various framework radix numbers.

Figure 9. Simulated wave form of TPG based BIST

Consider in VLSI the boundaries treated are region, deferral, recurrence and power, in view of these boundaries one can design to another. Here the thought of region and power utilizations are viewed as the boundaries are gotten by utilizing the instrument XILINX 14.7 and the HDL is Verilog language. When recurrence is something else for any plan it will speed up plan.

TABLE I.DEVICE UTILIZATION SUMMERY

Method	Delay (ns)	Area (LUT)
TPG method using BIST	1.019	23
BIST using RCA	4.986	96
BIST using Han Carlson adder	5.367	27

VII. Conclusions

For weighted designs, a new low power weighted TPG is suggested. The Galois operation and weighted designs are used to quantitatively determine the subset over the initial pseudo seed primary true quantities. When using the Test per Scan method, altering transition limiting causes the weighted Mux to be active concerning a phase shifter in the layout's side. Low power consumption for all clock cycles throughout the bottom area is implemented by the suggested weighted TPG, which has a 32-digit TPG. The project is completed along with BIST structures to show a better suggested design. Han Carlson adder and Ripple carry adder are used to compare the proposed designs to BIST Techniques. Galois operation is used to implement the work, and more hardware is added to the circuit design. Han-Carlson using BIST methods.

REFERENCES

[1] I. Pomeranz, ''Computing seeds for LFSR-based test generation from nontest cubes,'' IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 6, pp. 2392–2396, Jun. 2016, doi:10.1109/TVLSI.2015.2496190.

[2] G. N. Balaji and S. C. Pandian, ''Design of test pattern generator (TPG) by an optimized low power design for testability (DFT) for scan BIST circuits using transmission gates,'' Cluster Comput., vol. 22, no. S6, pp. 15231–15244, Nov. 2019, doi:10.1007/s10586-018-2552-x.

[3] J. Zhang, Q. Zhang, and J. Li, ''A novel TPG method for reducing BIST test-vector size,'' in Proc. Int. Symp. High Density Design Packag. Microsyst. Integr., no. 149, Jun. 2007, pp. 6–9, doi: 10.1109/HDP.2007. 4283639.

[4] S. Hellebrand, S. Tarnick, J. Rajski, B. Courtois, and T. I. M. Imag, ''Multiple-polynomial linear feedback shift registers,'' 1992, pp. 120–129.

[5] X. Lin and J. Rajski, ''Adaptive low shift power test pattern generator for logic BIST,'' in Proc. Asian Test Symp., 2010, pp. 355–360, doi: 10.1109/ATS.2010.67.

[6] A. S. Abu-Issa, ''Energy-efficient scheme for multiple scanchains BIST using weightbased segmentation,'' IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 3, pp. 361–365, Mar. 2018, doi: 10.1109/TCSII.2016. 2617160.

[7] G. S. Sankari and M. Maheswari, ''Energy efficientweighted test pattern generator based bist architecture,'' in Proc. Int. Conf. I-SMAC (IoT Soc. Mobile, Anal. Cloud), I-SMAC, 2019, pp. 448–453, doi: 10.1109/ I-SMAC.2018.8653768.

[8] R. Kapur, S. Patil, T. J. Snethen, and T. W. Williams, ''A weighted random pattern test generation system,'' IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 15, no. 8, pp. 1020–1025, Aug. 1996, doi: 10.1109/43.511581.

[9] A. Jas, C. V. Krishna, and N. A. Touba, ''Weighted pseudorandom hybrid BIST,'' IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 12, pp. 1277–1283, Dec. 2004, doi:10.1109/TVLSI.2004.837985.

[10] D.Xiang,M.Chen,andH.Fujiwara.''Usingweightedscanenablesignals to improve test effectiveness of scan-based BIST,'' IEEE Trans. Comput., vol. 56, no. 12, pp. 1619–1628, Dec.2007.

[11] H.-C. Tsai, K.-T. Cheng, and S. Bhawmik, ''On improving test quality of scan-based BIST,'' IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 19, no. 8, pp. 928–938, Aug. 2000, doi: 10.1109/ 43.856978.

[12] N. A. Touba and E. J. McCluskey, ''Altering a pseudo-random bit sequence for scan-based BIST,'' in Proc. IEEE Int. Test Conf., Oct. 1996, pp. 167–175, doi:10.1109/test.1996.556959.

[13] G. Kiefer, H. Vranken, E. J. Marinissen, and H. J. Wunderlich, ''Application of deterministic logic BIST on industrial circuits,'' J. Electron. Test. Theory Appl., vol. 17, nos. 3–4, pp. 351–362, 2001, doi: 10.1023/A:1012283800306.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

12T MEMORY CELL FOR AEROSPACEAPPLICATIONS IN NANO SCALE CMOS TECHNOLOGY

Pandi Akshita Sagar, M.Tech Student (VLSI System Design) Avanthi Institute of Engineering & Technology, Hyderabad
Dr.S.Kishore Reddy, Associate Professor, HOD, ECE Department, Avanthi Institute of Engineering & Technology, Hyderabad
Dr G Chandra Shekar, Assistant Professor, ECE Department, Avanthi Institute of Engineering & Technology, Hyderabad

***Abstract*— The size of semiconductors and the distances between them are rapidly shrinking as technology advances. As a result, SRAM cells used in aerospace applications become more susceptible to soft-error when the fundamental charge of the fragile nodes decreases. Single-event upsets (SEUs)may cause data inversion if a radiation particle hits a sensitive node in a typical 6T SRAM cell. To lessen the impact of SEUs, this paper proposes a Soft-Error-Aware Read-Stability-Enhanced Low-Power 12T (SARP12T) SRAM cell. SARP12T's performance is evaluated in relation to those of other recently released soft-error-aware SRAM cells such as QUCCE12T, QUATRO12T, RHD12T, RHPD12T, and RSP14T. Even if the values of the sensitive nodes in SARP12T are flipped due to a radiation attack, the data may be recoverable. SARP12T is resilient to storage node-pair-initiated single-event multi-node upsets (SEMNUs). The '0' storing memory nodes in the proposed cell are easily accessible through the bitline during read operation and are highly resistant to interruptions. SARP12T is also the most efficient method of holding in terms of energy consumption. SARP12T outperforms competing cells in terms of write performance, and its write latency is much lower. The suggested cell achieves all of these advantages with just a little increase in read latency and read/write energy.**

Keywords— Aerospace, SARP12T, QUCCE12T, SRAM

I. Introduction

The strong ionizing effect of radiation near nuclear reactors and in space has the potential to impair or destroy electrical infrastructure. Ionizing radiation has been linked to circuit failures, notably in data storage devices. The scientific community uses the term "single event upset" (SEU) to describe the occurrence of several ionizing effects of radiation at once [1, 2]. On the one hand, the idea that this radiation doesn't have any effect on long-term memory seems conceivable. When many events occur at once, it may cause an electronic equipment to malfunction, a phenomenon known as the "single event multi-upset effect" (SEMU) [22]. Resetting [7] the electrical cycle withsoftware that employs state machines to recognize prior states might reduce radiation risks. Spending a little amount on space-related applications won't alter this fact [4]. Bit flipping in ionizing CMOS [16] memory is the source of a soft mistake [17]. This impact is due to the expansion of pores in the oxide layer. This strategy makes data storage very sluggish to access. When evaluating SRAM memory in the presence of ionizing radiation, it may be helpful to use a write cycle of different time and complexity to better display the findings. Every new generation of technology results in smaller and more powerful integrated circuit machines. The goal of this technique, which makes use of integrated circuits, is to increase output by packing as many components into a given space as feasible. As Moore's law has been roughly followed, the size of transistors, the fundamental building blocks of memory cells, has risen. So, it stands to reason thatcell density will gradually reduce with each succeeding generation [1]. Due to the small size of the transistors used in contemporary technology, each individual cell constitutes a nanoscale system; this is how SRAM-compatible metal-oxide-semiconductor (CMOS) memory is created. As a result, SRAM chips are able to function at steadily decreasing voltages. The International Technological Strategy for Semiconductors (ITRS) predicted that this trend would reverse, but the opposite has already occurred. The scaling limitation on the threshold voltage of the transistor kept the leakage current to an acceptable level [2]. These static random access memories (SRAMs) are essential to the operation of many contemporary electronic devices. This need has been met in large part through the allocation of dedicated space. Costs are anticipated to increase as the predicted number of patients exceeds 90% [3. The technicians are trying to fit as many SRAM cells as they can into each part. Because it results in cells that are smaller in size, this procedure is crucial for improving the technology. SRAMs have transistors that are normally as small and as high up in the architecture as is practicable. Additionally, the voltage is maintained low to ease strain on the electrical system. However, the reduced power usage was only partially implementedin practice. With the development of new technologies, SRAM devices have become smaller and use less power; nonetheless, the design still has to overcome two significant obstacles, namely, cell stability and transient event radiation. This study focuses on the latter phenomenon. However, there are also inquiries into SRAM dependability concerns. In terms of regional radiation, SRAMsare crucial. They might be badly damaged by single-event upsets (SEUs), which are triggered bya single particle of energy. These failures are categorized as soft errors (SE) since they do not permanently harm the circuit. When massive particles collide, they release electron-hole pairs (SEUs), which are gathered in a sensitive region and utilized to control the circuit's power supply. A node in an SRAM array may check the status of a cell and change the data stored in it if there is enough noise. There is no truth to these claims at all. One or more SRAM cells might have theirdata corrupted by a passing particle.

I. PROPOSED METHOD

This novel radiation-hardened-by-design (RHBD) 12T storage facility features an easily implementable layout-topology and also takes into consideration the physical mechanism of upset in soft faults. The validation results show that the proposed 12T cell can provide significant radiation resistance. The predicted 12T cell requires more room, energy, and time to read and write than a 13T cell. The 986.2 mV-margin of staticnoise in the hold is more than what a 13T cell can achieve. The

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

error-correcting capabilities of the recommended 12T cell make it more trustworthy. These days, CMOS technology is ubiquitous in the electronics sector. The aircraft industry is another that benefits greatly from CMOS technology. Memories are the primary data storage mechanism in many aeronautical applications. CMOS technology is used in the production of SRAM cells, a kind of memory. The main problem with long-term memory is single-event disruptions (SEUs), which are brought on by particles of radiation. Rising urbanization is directly responsible for the SEUs. As CMOS process technology has advanced, both the critical charge and supply voltage have decreased. A approach free of these SEUs is needed for use in aircraft systems. Where exactly do they exist in the very radioactive void between the stars? Methods that are radiation- hardened by design (RHBD) that are resistant to soft errors are currently being researched. The primary contribution of this study is a proposal for a low-profile, high- reliability RHBD memory cell.

"Adiabatic logic" refers to low-power electrical circuits that may be employed in either direction. During the adiabatic phase, there is no change in the total quantity of heat or energy in the system, thus the name. Energy dissipation is greatly improved by decreasing circuit size and increasing circuit fineness, which has been a major motivation for studying adiabatic circuits.

A. SCRL NAND

Understanding the big picture behind this group of genes may require dissecting the SCRL NA ND completeloop shown in Figure 1.

This ND uses trapezoidal clocks (Kin1 and / Kin1) to power the top and bottom tracks,rather than the more conventional Vdd and Gne 1. There has been no change to this section. With the exception of P 1, which is connected to Gnd, and /P 1, which is connected to Vdd, all components are linked to Vdd/2 in the first position, rendering the switch gate superfluous. The transmission gate is turned on once P 1 and P 1 are configured. First steps. Vdd and Gnd are then created from the /first 1 and /first 1 Vdd/2 nodes. At this stage, the NA ND of both a and b go through the same non-adiabatic door calculation. Once the output is being utilized by the subsequent gate, the transmitting gate may be gradually disabled. The input may be adjusted and the next phase initiated once the sum of phases 0 and 1 reaches Vdd/2 again. Since a deviation from Vdd/2 would violate the first criterion, a resistor must be disabled and the rails reset to this value.

P-MOS's function when coupled with B input is unclear. Please review the circumstances behind the disappearance of the transistor. Times of the eleventh day.

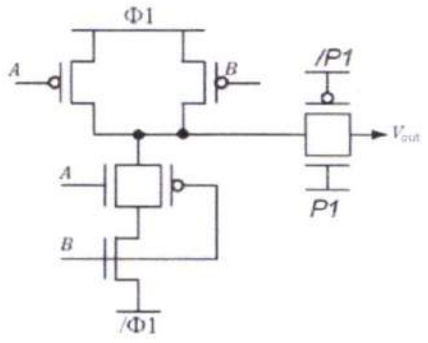


Figure 1 : SCRL NAND

B. 2LAL

Frank's[2] Another significant class of adiabatic circuits is the 2LAL family. This series, like SCRL, has complete plumbing all the way to the gate. Figure 2(a) depicts the fundamental components of 2LAL, a pair of transmission gates used to represent the signals A and A. Because of its simplicity and independence from CMOS, 2LAL is well suited for implementation in cutting-edge devices.

Two transmission gates make up the 2LAL basic buffer feature, seen in Figure 2(b). Each trapezoidal clock's zero point on the fourth cycle happens one and a quarter timeslater than the other. Both vertices start out with a value of 0 at the beginning. If the input is 1, the state will change from 0 to 1 over time. When we go on to "phase 1,"

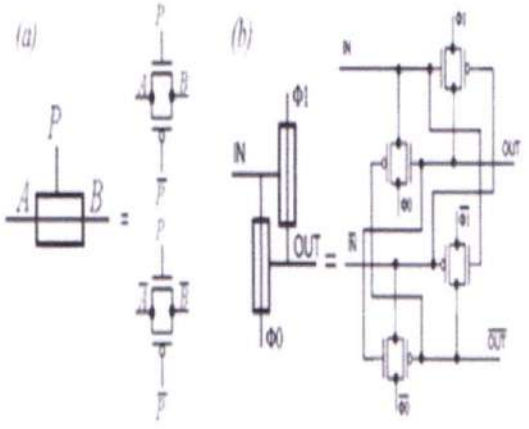


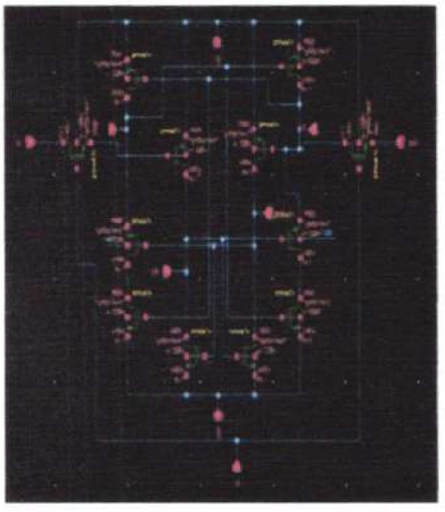
Figure 2: 2LAL Basic Gate(a) and Buffer(b)

When the input is 1, the output and input are both set to 1, and the transistor is disabledto save power. Finally, switch the input back to 0 and keep cycling between 1 and 0. The pipeline is ready to accept a new input after the output passes through the next gate and reverts to 0. 2LAL can build inverters quickly since rails may cross from one portto another.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

II. RESULT

A. *Proposed schematic*



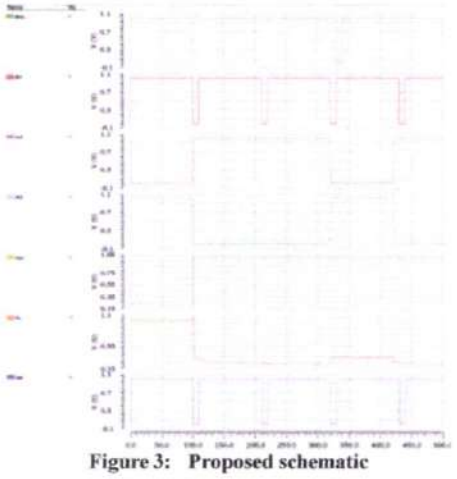


Figure 3: Proposed schematic

Figure 4 : proposed schematic simulation result

A. DELAY

Parsing	0.01 seconds
Setup	0.05 seconds
DC operating point	0.07 seconds
Transient Analysis	0.03 seconds
Overhead	0.91 seconds
Total	1.07 seconds

A. POWER

```
Power Results

VVoltageSource_3 from time 0 to 100
Average power consumed -> 5.594084e-011 watts
Max power 2.061770e-000 at time 8.025e-008
Min power 8.198842e-003 at time 3.20774e-008
```

III. CONCLUSION

The unique 12T RHBD memory cell developed here lessens the effect of soft mistakes in standard 65 nm CMOS technology. The proposed memory cell is an advancement over prior designs in a number of respects; most importantly, it is more resistant to disturbances that damage several nodes. 1000 MC simulations further corroborate the process's SEU robustness by demonstrating that no changes to the process affect the SEU's stability. Some high-speed applications may be slowed down by the proposed 12T memory cell because of its slower read access time compared to existing memory technologies. Memory size, robustness, and reliability may be of far greater importance in mission-critical aircraft applications. In light of this, the RHBD 12T memory cell reported in this paper is, from the standpoint of a critical application designer, an excellent design for radiation resistance when compared to other state-of-the-art hardened memory cells. Increasing the paper's speed while decreasing its footprint is a common method of improvement.

One of the trickiest Nano-scale dependability issues to solve is the BTI, which modifies the transistor's Vth value. Changing the Vth of SRAM transistors degrades the quality of SNMs. In this study, we describe a sensor that can detect BTI deterioration in SRAM cells with high accuracy, allowing for the monitoring of this process over time. The peak Ivdd/Ignd of the SRAM block during a write operation may be used as a proxy for the NBTI/PBTI aging of individual SRAM cells. The CCVS measures and convertsthis current to voltage. The fundamental frequency of the VCO's oscillation is set by the maximum value of this voltage. The frequency of the oscillations may be comparedto that of newly created cells to observe the impact of BTI. Reading the appropriate item in the SRAM may reveal the row or cell's BTI condition.

REFERENCES

[1] E. Ibe, H. Taniguchi, Y. Yahagi, K.-I. Shimbo, and T. Toba, "Impact of scaling onneutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," IEEE Trans. Electron Devices, vol. 57, no. 7, pp. 1527–1538, Jul. 2010.

[2] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-eventupset in digital microelectronics," IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 583–602,Jun. 2003.

[3] R. C. Baumann, "Soft errors in advanced semiconductor devices part I: The three radiation sources," IEEE Trans. Device Mater. Rel., vol. 1, no. 1, pp. 17–22, Mar. 2001.

[4] H. L. Hughes and J. M. Benedetto, "Radiation effects and hardening of MOS technology: Devices and circuits," IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 500–521,Jun. 2003.

[5] C. Boatella, G. Hubert, R. Ecoffet, and S. Duzellier,

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

"ICARE on-board SAC-C: More than 8 years of SEU and MCU, analysis and prediction," IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 2000–2009, Aug. 2003.

[6] Y. Bentoutou, "A real time EDAC system for applications onboard earth observation small satellites," IEEE Trans. Aerosp. Electron. Syst., vol. 48, no. 1, pp. 648–657, Jan. 2012.

[7] P. D. Bradley and E. Normand, "Single event upsets in implantable cardioverter defibrillators," IEEE Trans. Nucl. Sci., vol. 45, no. 6, pp. 2929–2940, Dec. 1998.

[8] M. L. McLain, H. J. Barnaby, I. S. Esqueda, J. Oder, and B. Vermeire, "Reliabilityof high performance standard two-edge and radiation hardened by design enclosed geometry transistors," in Proc. IEEE Int. Rel. Phys. Symp., Apr. 2009, pp. 174–179.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

OVERLOADED CDMA CROSSBAR FOR NETWORK-ON-CHIP

Jella Vamshi Krishna, M.Tech Student (VLSI System Design) Avanthi Institute of Engineering & Technology, Hyderabad
Dr.S.Kishore Reddy, Associate Professor, HOD, ECE Department, Avanthi Institute of Engineering & Technology, Hyderabad
D.SuryaPrakesh, Assistant Professor, ECE Department, Avanthi Institute of Engineering & Technology, Hyderabad

Abstract— **Due to its apparent benefits, such as acclimatized idleness, ensured benefit, and a below-framework able nature, Code Division Multiple Access (CDMA) has been advocated as the concrete band allotment admittance of Network On-Chip (NoC) interconnects. Because CDMA interconnects are used in restricted correspondences, in which different elements of a CDMA-encoded guiding conversation are delivered across different channels, they have been widely accepted by the human population of the NoC. It is not necessary to assume the CDMA channel if the limited obstruction issue can be mitigated by the effective use of on-chip interconnects. This disagreement also implies that transporters and restricted channels often switch roles, in contrast to on-chip interconnects. There are two separate accounts for encoding and decoding data packets, and each success bit is encoded using a unique CDMA technique. Despite the broad use of CDMA in NoC human culture, this practice persisted. Our research presents Aggregated CDMA (ACDMA), a novel CDMA encoding/decoding scheme for NoC interconnects in which each array $.25 is encoded in its own CDMA channel, hence eliminating the space and animation overheads associated with encoding/translating approaches.**

Keywords— Network On-Chip, CDMA, encoding and decoding

I. Introduction

An SOC is an integrated circuit that incorporates a sophisticated electronic system. There are difficulties in gigabit communication due to the bus design utilized in its creation. Onlyby creating a system with explicit modularity and parallelism could the communications bottleneck be removed. The key concept is that cores may talk to each other on the chip tocoordinate resource allocation and use.

Building a more effective NOC requires a router that is constructed well enough to allow for communication on the network on chip. The maximum number of simultaneous connections that may be made to this router is four. It enhances router performance through store and forward flow management and deterministic routing provided by the FsmController. As is common with on-chip networks, the packet switching method is used. In packet switching, each router makes its own independent judgment on where to send packets. The optimal flow mechanism is store-and-forward since it does not need any additional bandwidth to function. Data transmission on each channel will be prioritized in turn by the arbitrator. This router employs buffering to prevent input and output bottlenecks.

Information may be sent from one network to another with the help of a device called a router. The term "traffic direction" describes what routers do in the connected world. A microprocessor-operated router links several networks together so that information may be sent between them. If data travels along a wire without being interrupted, it has arrived.The packet's destination is determined by the router based on the address it was given. The router then consults its routing database to locate the proper network to deliver the message.

This gadget is marketed as a "Four Port Network Router," however it really just has a singleinput port. The data might go in one of three directions. The bundle consists of three individual pieces. The three sections are the frame check sequence, the data, and the header.Information reaches its final destination after traveling from router to router across the many networks that make up the Internet. Routers may forward data packets from one network to another, but they can also modify the packet's transmission protocol so that it is compatible with the receiving network.
Dynamic routing protocols allow routers in a network to coordinate the transmission of data. Each router maintains a database of all possible associations between any two nodes on the network. The interfaces of a router let it talk to wired and wireless networks via various physical protocols. Firmware for several network protocols is supplied as well. The data transfer protocols employed by each network interface are translated by this specialistsoftware.

Some routers may also link together logical networks of computers called "subnets," whichoperate independently of the physical networks. Subnet addresses and interface connections may be somewhat different and yet be recognized by the router.

II.. ROUTER DESIGN SPECIFICATION

In the routing protocol, packets are very important. Input packets are processed andsent to their respective destinations through the router's output ports. There is just one inputport on the router that can receive data packets. Only one of the three holes will allow thepackage to escape.

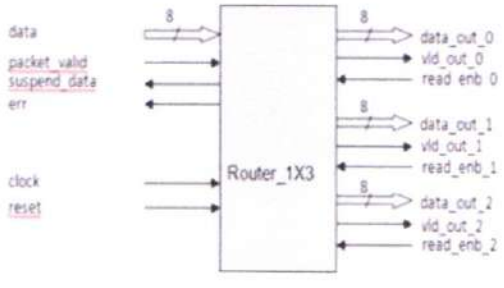


Figure 1:block diagram of four port router

Data packets received by a router's input port are sent to the router's output port after being processed. Input and output channels' independent decoding logic boosts the router's

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

efficiency. A buffer is a short-term memory region that can receive and send data from anywhere.
This can be accomplished via store-and-forward buffering. The current logic of control might be used to regulate arbitration outcomes. As a result, the input and output ports may now exchange data with one another. The FSM's control bit lines are programmed with the data packet's destination. The term "switching mechanism" is often used to describe the method through which data is sent from one place to another. In this case, a flit size of 8 is employed in conjunction with the packet switching methodology. Because of this, the sizeof a packet might vary from 0 to 8 bits.

A. Four port router architecture

Three-Block Method for a Four-Router Architecture.The different parts include an output block, a Router controller, and an 8-Bit Register. The router's output block consists of three FIFOs that operate in tandem to store packets of data until they are required; the controller is developed using a finite state machine (FSM) architecture. The router accepts inputs onits single 8-bit data port from the global clock and reset signals as well as the err and suspended data signals. The FSM controller has detected two errors: error and suspended_data_in.This FSM study explains in depth how these features work.

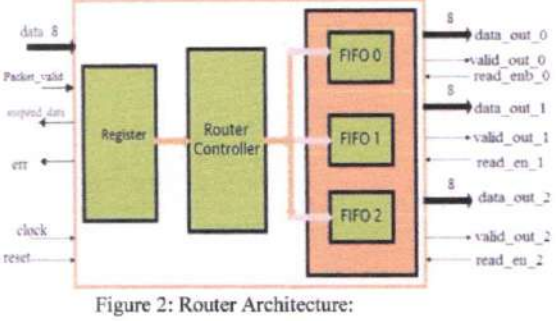


Figure 2: Router Architecture:

This image depicts a 4-port router.

Registers for the Network router_1x3's status & data & parity are kept in the router_reg module.the registers allow the fsm_router's control signals to "latch" onto updated status or input data.In order to receive data from the correct input port, the fsm_router module allots three FIFOs to each output port.

B. OCI Crossbar High-Level Architecture

The main objective of this paper is increasing the number of ports sharing the ordinary CDMA crossbar presented in [17], while keeping the system complexity unchanged using simple encoding circuitry and relying on the accumulator decoder with minimal changes. To achieve this goal, some modifications to the classical CDMA crossbar are advanced. Fig. 2 depicts the high-level architecture of the OCI crossbar for a single-bit interconnection. The same architecture is replicated for a multibit CDMA router. M TX-RX ports share the CDMA router, where spread data from the transmit ports are added using an arithmetic binary adder having M binary inputs and an m-bit output, where m = log2 M The adder is implemented in both the reference and pipelined architectures. A controller block is used for code assignment and arbitration tasks. Each PE is interfaced to an encoder/ decoder wrapper enabling data spreading/ dispreading.

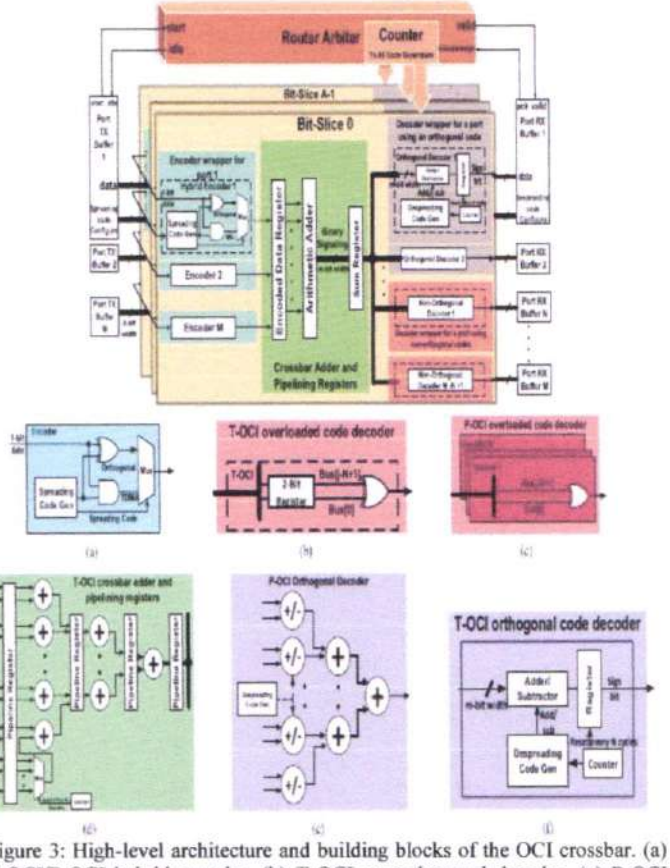


Figure 3: High-level architecture and building blocks of the OCI crossbar. (a) T-OCI/P-OCI hybrid encoder. (b) T-OCI nonorthogonal decoder. (c) P-OCI nonorthogonal decoder. (d) T-OCI pipelined crossbar tree adder, in which the adder is replicated N times for P-OCI crossbar. (e) P-OCI orthogonal decoder. (f) T-OCI orthogonal decoder.

III.EXISTING METHOD

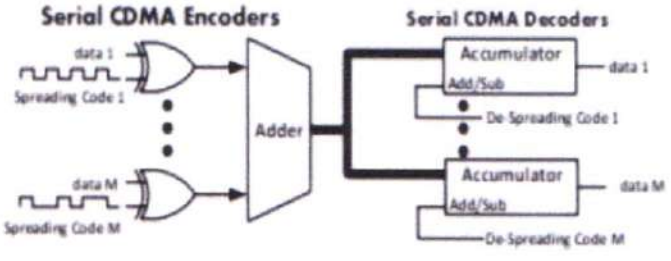


Figure 4. Conventional CDMA crossbar .

Figure 4 shows the proper CDMA batten used in the signature. The batten uses Walsh overextension codes with a width of N chips to interconnect N pairs of address and receive pins. Each address node's supplemental data is encrypted using an XOR encoder; each data bit is XORed with a randomly selected N-chip overextension cipher, and the resulting cipher is sent through transmit-get amalgamate in N clock cycles. All my snake and heavenly friends

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

should receive ports. Each get anchorage has a decoder that compresses data from the approach absolute using a degraded overextension algorithm. Since the despreading cipher chips are unipolar ("0" or "1") in nature, an aggregator and a multiplexer are required for the affiliation process. This is a practical implementation of the constrainedCDMA standards in NoC interconnects; each accomplishment bit in an advice discussion is encoded and transmitted using a different CDMA technique, and the encoding/translating procedure is repeated W times for advice bundles of amplitude W. However, the impedance problem causes the small number of accord channels to fluctuate constantly. Using variants of admission control and MIMO, a similarly constrained strategy might be utilized to resolve the transmitter/collector ambiguity. Again, utilizing a detached approach as directed by a user manual, the agitation and blocking effects of on-chip interconnects may be fine-tuned.

IV. PROPOSED METHOD

Connecting N address (TX) ports to N get ports, with the advice amplitude of each anchoring being W where W = log2 max(dj), the ACDMA batten constructs the NoC's smart band. As can be seen in Figure 2(a), the encoders, the approach snake, and the decoders are the three presumptive components of the atypical accessory design of the ACDMA batten. Figure b. depicts how the encoders use W XOR gates to transmit data from the various TX nodes. The ultimate goal of the Walsh balanced cipher is to combine the approach viper with the overextension cipher adders, and this is achieved by pushing the overextension chips back from the encoder arrest to the absolute snake arrest. As a result, encoders can only produce up to W bits each year. The encoder outputs are re-added in (3) to generate the full Si. In Figure (c), a timberline viper exemplifies the approach snake's most fundamental strategy for amplifying sounds. In this metaphor, the encoders for the TX ports are the leaves and the total yield is the trunk. The efficiency of the tree line

is log2(N) when there are N leaves in the background. Crop worries caused by each timberline viper are equivalent to those caused by advice worries plus one in order to avoidfloods. The width of the crop condition at the bottom snake may be computed as W+1+log2(N), where W is the width of the first snake's range and N is the strength of the viper timberline. After each annual appearance, registers for the pipeline are permanently mounted to the treeline to ensure the channel is always facing in the correct direction. After then, each of the N decoders' RX ports receives the absolute value Si.

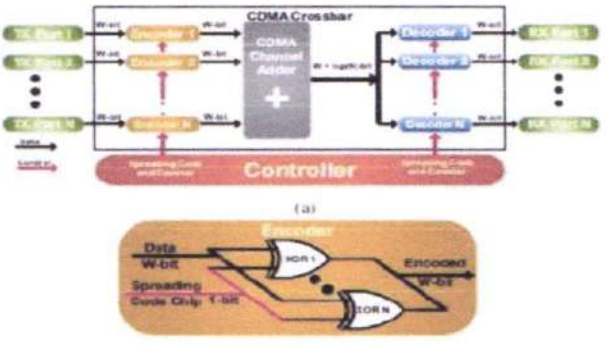


Figure 5. (a) ACDMA crossbar high-level architecture

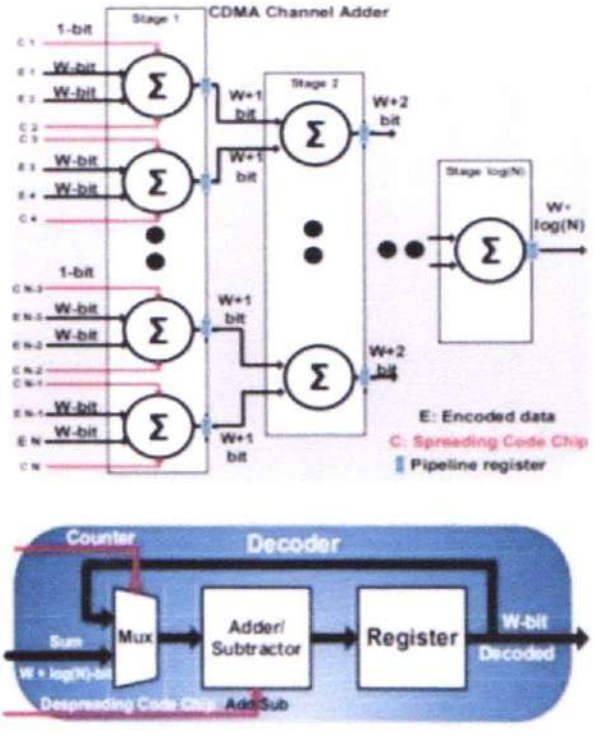


Figure 5. (b) ACDMA channel adder, (c)ACDMA decoder

Using just a viper/subtracted and an accept abiding as an up/down gatherer, the decoders effectively remove the cross-connection in Equation, as shown in Figure. The 1 chip requirement of the dispersion cipher Ck reduces aggressive association to the simple amplification and addition of uniform wholes Si. The decoder is therefore realized as an up/down accumulator, with the absoluteness Si being added or subtracted from the result stored in the registers in accordance with the distribution dent Ci k through the snake/subtracted operation. For those who want the nitty-gritty, the snake will add Si to theadmit's likelihood if the scattering dot is 1, and subtract Si if it is -1. As shown by (5), at the conclusion of the decoding cycle, the beneficiary admit stores N dk, and in the area where N = 2n and n is a number, the advise dk is decoded by moving the collector agreement by log2(N) bits.

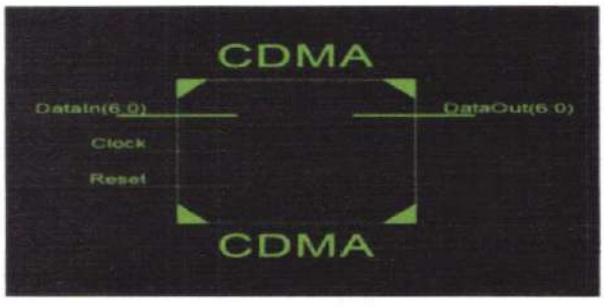
Two advisory XOR gates may be thought of as two independent circuits. There are more viper wires that can connect to the ACDMA crossbar than to a standard CDMA

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

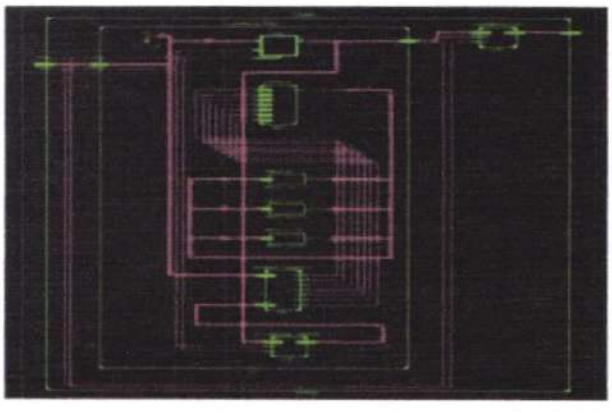
crossbar. Each year brings one more snake affair that results in a one-piece approach in the standard CDMA crossbar. Therefore, 1+log2(N)i is the formula for the number of viper incidences in year I. Since there are 2i adders at each stage, the total number of viper events for a word of length W is proportional to log2N1 i=0 2i (W + W(log2N i)). However, in the ACDMA crossbar, the total number of deals is only log2N1 i=0 2i (W +log2N i), which is a factor of W smaller than the number of deals in the standard CDMA crossbar for a conversation of length W. Because of its low starting price of $.25, the ACDMA batten has seen broad adoption. The viper's true form is revealed when the number of approach wires rises, since this corresponds to an increase in the number of flip-slumps in the decoder registers. Thisis because, despite its numerous advantages, the ACDMA crossbar has a less W appeal than the conventional CDMA crossbar.

V. RESULTS

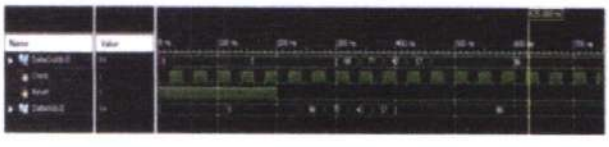
I.RTL diagram:



II. Internal.RTL



III. *Simulation results*



IV. CONCLUSION

The developed method ensures the safe transport of centralized data within a local area network. Whether a long or short range is needed determines whether an RF, Bluetooth, or zigbee transmitter/receiver module is used. Inside an industry, where there is less background noise and more robust security, the gadget might be utilized to transmit detected data. The idea behind this project really shines in situations when modifications to the hardware and layout can be made quickly and cheaply. Code hopping and dynamic code division multiple access (CDMA) are two approaches that show promise for improving the system's security and performance. Therefore, this approach is easy to apply, improve, and utilize to set up secure networks.

Researchers in this research speculate that NoC routers' physical layer might benefit from using overloaded CDMA crossbars. When a communication channel is congested, nonorthogonal codes are used in code division multiple access (CDMA) to increase its capacity. We suggest two crossbar topologies, T-OCI and P-OCI, that use the overloaded CDMA idea to increase the capacity of CDMA crossbars.. In order to improve the carrying capacity of standard CDMA crossbars without altering the fundamental accumulator decoder architecture, our work takes use of a subset of the Walsh spreading code family that is currently in use. Procedures for creating nonorthogonal spreading codes and crossbar variant reference structures are provided. The barriers between T and P OCI are now open.

This study's results have far-reaching ramifications for studies to come in many other areas. To expand the CDMA link's capacity, researchers have experimented with different architectural enhancements to the OCI crossbar and made use of the mathematical features of the code space to discover new no orthogonal codes. Making CDMA connections more robust against interruptions will be a primary focus of future study. Our objectives include expanding our understanding of OCI-based routers and evaluating their performance relative to established benchmarks.

REFERENCES

1 L. Wang, J. Hao, and F. Wang. Transport based and NoC framework execution imitatingand correlation. In Information Technology: New Generations, 2009. ITNG '09. 6th International Conference on, pages 855– 858, April 2009.

2 R. H. Chime, Chang Yong Kang, L. John, and E. E. Swartzlander. CDMA as a multiprocessor interconnect procedure. In Signals, Systems and Computers, 2001. Meeting Record of the Thirty-Fifth Asilomar Conference on, volume 2, pages 1246– 1250 vol.2, Nov 2001.

3 B. C. C. Lai, P. Schaumont, and I. Verbauwhede. CT-transport: a heterogeneous CDMA/TDMA transport for future SOC. In Signals, Systems and Computers, 2004. Meeting Record of the Thirty-Eighth Asilomar Conference on, volume 2, pages 1868– 1872 Vol.2, Nov 2004.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

4 K. E. Ahmed and M. M. Farag. Over-burden CDMA transport topology for MPSoC interconnect. In 2014 International Conference on ReConFigurable Computing and FPGAs(ReConFig14), pages 1– 7, Dec 2014.

5 K. E. Ahmed and M. M. Farag. Improved over-burden CDMA interconnect (OCI) transport design for on-chip correspondence. In 2015 IEEE 23rd Annual Symposium on High-Performance Interconnects, pages 78– 87, Aug 2015.

ODJ
ISSN NO:0889-6402

Implementation Of Weighted Pseudorandom Test Pattern Generator for a Built In Self Test Architecture

Karantothu roja M.Tech Student (VLSI System Design) Avanthi Institute of Engineering & Technology, Hyderabad
Dr.S.Kishore Reddy Associate Professor, HOD, ECE Avanthi Institute of Engineering & Technology, Hyderabad
S.Sagar Assistant Professor, ECE, Avanthi Institute of Engineering & Technology, Hyderabad

Abstract **-There is a significant demand for the functionality of the chip to be increased as submicron technology develops. The current generation's widespread IC production necessitates stringent testing to distinguish between the ideal chip and the flawed one. Verification For a full-scale verification to find product flaws, engineers must be knowledgeable of the chip's functionality. Traditional testing methods demand a significant amount of time and circuit complexity, making them unsuitable for the current generation. So, the automatic test pattern generation with great unpredictability between the test pattern generations becomes necessary. The randomness utilized to create the test pattern is produced by Galois Fields. A weighted test pattern generator has also been.**

Keywords :Built In Self-Test, circuit under test, test pattern generator, Pseudorandom TPG

I. Introduction

Current innovation has focused on growing low-power frameworks for especially vast scope becoming a member of (VLSI) speedy plans. Therefore, some plan techniques [1] have been completed to alleviate compromises among execution, strength, and vicinity. Some methodologies have concentrated on low-power dispersal throughout BIST normal mode operations rather than test mode operation [1].

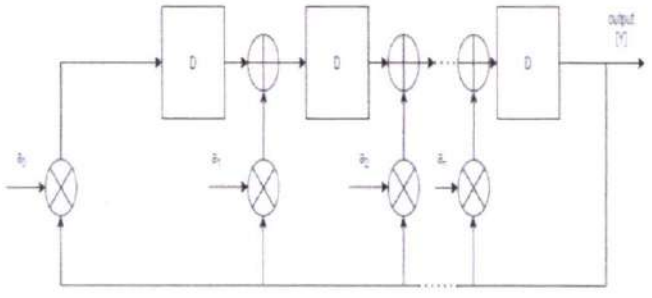


Figure 1. An example of a conventional pseudo random TPG

During the BIST normal mode operation, the replacing motion with inside the output chains and check information stress using the suitable TPG are crucial. Additionally, this finding out should be achieved with immoderate dependability and responsiveness in semiconductor designs. Figure1 illustrates an example of a conventional [2].The partner supervisor planning the survey of this composition and helping it for distribution changed into Wu-Shiung Feng.

A. Pseudorandom TPG

The TPG contains of the affiliation of length n shift registers and input seed bits of a_0, a_1, a_2..., an. In moderate of the n^{th} cycle of the shift sign up, the $(I - 1)^{th}$ clock cycle[3] is refreshed constantly through manner of method of the $(n_1)^{th}$ cycle of the shift sign up and the I^{th} clock cycle. The TPGs make use of important level of parallelism to perform excessive cross back records in several useful packages. The TPG [1] direct capability is executed through way of method of the outset complete signal and the data seed bits. Its direct functionalities are implemented in many programs like plane frameworks, cockpit frameworks, scientific frameworks, sound and video frameworks, and power age and dispersion frameworks.

A TPG carries of deterministic, complete, pseudorandom, pseudorandom weighted [4] and blended mode yields. The pseudorandom weighted out placed issued to carry out better problem inclusion in numerous BIST systems. The weighted pseudorandom TPG suggests genuine irregularity and repeatable examples in all clock cycles. Regularly, it requires one seed bit to deliver one check format for 'n' forms of the checking ease within side the check according to take look at BIST[2], in which 'n' is the scan chain cycle. The most modern overview diminished the switching activity all through test shift cycles. Furthermore, the TPG permits the programmed preference of weighted obstacles to perform its low power. The weighted pseudo arbitrary TPG techniques and their execution in, can in true lessen the replacing modifications. Nonetheless, the techniques, incorporated extra XOR adjustments the various shift registers [3], it consumed extra power and location. The BIST necessities need to be in fashionable zero in at the better short coming inclusion and the lesser weighted changing movement with lower power.

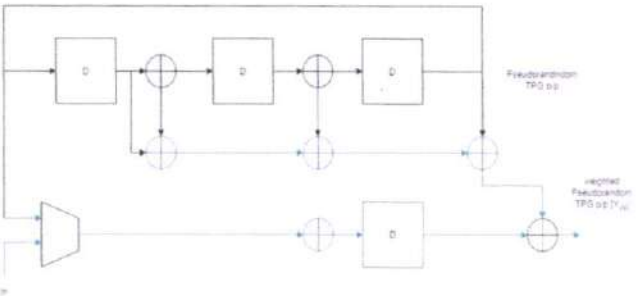


Figure 2. (a) spare TPG

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

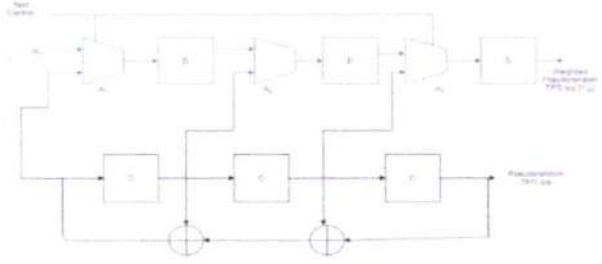


Figure 2. (b) Spare TPG

To accomplish those requirements, methodologies can be used. One is to regulate the circuit plan of the weighted TPG [4]. The distinctive is to remember more machines for the weighted TPG. The present work describes every different pseudorandom weighted TPG is advanced the use of extra machine. Also, higher shortcoming inclusion is accomplished as a long way as getting rid of change remove deficiencies using check thing addition. The check focuses are embedded for every NAND entryway design of the general plan region. The proposed approach is composed of purchasing and promoting weighted check examples to the output chains the use of a phase shifter.

The buying and promoting of the weighted examples taken into consideration for picking the earlier output chains with lesser region is contrasted and that of the others scan chains [5]. The weighted examples are consequently carried out with all the output chains of BIST layout. This dispenses with the problems at a predefined yield and further improves the fault coverage. The TPG likewise in addition develops its speedy changing motion due to its selected weighted designs and reduces its ordinary checking and catching energy usage in some unspecified time in the future of BIST check consistent with observe. The proposed TPG is planned using intent door strategies and finished in precise test according to observe BIST designs.

II. Existing Weighted Pseudorandom TPGS

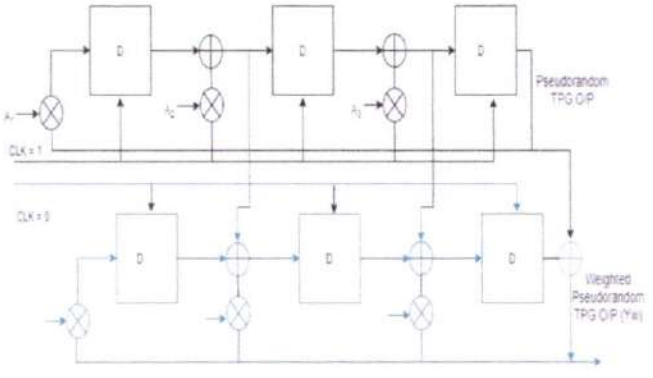


Figure 3. Existing 3-bit weighted pseudorandom TPG

The primitive polynomial chosen for the now not set in tone with the resource of the use of the even or ordinary faucet bits from the register. By and large, crude polynomials are carried out for growing pseudorandom designs. On the off risk that the faucet bit groupings of a n-digit TPG [5] are n, m, k, l, . . . , 0, then the co primes of the faucet numbers, like n-n, n-m, n-k, n-l, . . . , n-0, will likewise produce the pseudorandom TPG yield. Utilizing this concept, the TPG can create a notable length of pseudo critical seeds. In Figure 2, the darkish line way that the supply TPG yields pseudorandom designs, and the blue line. Factors show the greater system implemented for producing the weighted pseudorandom designs [6].

The existing weighted repetitive TPG approach in Figure 3 makes use of each device or duplication elements. The hardware redundancy duplicates its functions into double modular redundancy, triple modular redundancy and so on. This may be completed through copying the greater tool for the deliver TPG configuration, therefore removing the arbitrary example steady short comings. Be that due to the fact it may, the device overt repetitiveness TPG accomplishes super execution factors; it needs to be reducible with inside the device above [3]. The time overt repetitiveness is finished using the one of a kind time measures rather than the tool utilizing the offbeat clock values going from "0" to "1". In any case, a similar interest is carried out making use of several time elements for the weighted examples. This method distinguishes numerous secure deficiencies at some point of several clock cycles.

The existing 3-bit weighted pseudorandom TPG maximum details applied for generating the weighted examples associated with, the manage bits for the multiplexer (Mux) [6]. The greater tool is likewise used to offer the reseeding quantities expected for the check example to differentiate their faults. The Mux with inside the extra hardware identifies informs the information seeds and to manipulate bits even as the regular weight input Win passes the weighted examples to a end result. In any case, this recalls a large place above for the can woodland plan of the BIST engineering. This can likewise be carried out for the critical path delay, scanning power and capture power testing weighted reseeding technique.

Later, more sophisticated TPG techniques are introduced, as illustrated in Figure3, to circumvent the restrictions of these TPGs. These strategies use identical TPGs and records overt repetitiveness to focus on the test pattern's weight [2]. Barry et al. claim (Figure 3) that the TPG strategy makes use of a Mux a few of the D flip flops, where the signal is planned to be managed to the underlying enormous state of the weighted instance. In the end, the suggested TPG incorporates the requirements of the current works. It presents a valid scenario for producing weighted examples for a larger seed bit with significantly less power and placement above. Essentially, this strategy must guarantee low power interest during the full test for each study.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

III. Weighted Pseudorandom TPG Using the Galois Operation with a Phase Shifter.

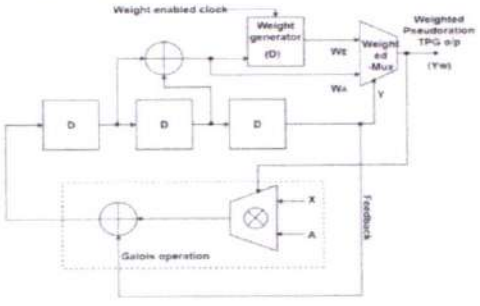


Figure 4. Proposed 3-bit weighted pseudo random TPG.

Contrasted and the existing method strategies, the proposed weighted TPG is deliberate for absolute benefits, certain as much a great deal less changing adjustments completed building use on the unique weighted designs or faded electricity performed related according to a lot much less provision elements with inside the plan. This decreases the provision over or similarly develops the challenge inclusions with inside the BIST [8]. The TPG approach displayed within is the proposed TPG, which includes the Galois operation and addition hardware for weighted pattern generation. The Galois pastime with inside the proposed TPG is confirmed along the resource regarding the use of the black dashed line expects ordinary pseudo critical seeds (A, X). Nonetheless, the regular truss portions may additionally remain prolonged construction uses concerning similar subset on introductory essential seeds [9]. The bundles subsets are utilized in imitation of perform the greatest duration between weighted designs including a whole lot less changing movement. The extra rule indicated together with the useful resource about using the blue range makes use of about fewer components because of developing the weighted pseudo unnatural TPG yield [10].

A. Proposed 3-bit weighted pseudorandom TPG.

Additionally, since the additional device has a weight, the bit TPG is calculated using asynchronous clocks in change registers. The check vectors (Z) are then given in accordance with the archives vector pain (X), which is continuously replicated with the helpful resource regarding the employment of the pseudo essential fascicle chewed (A). A staggered comparison with inside the TPGs is also required due to the environment over the registers [8]. Because of the complaint loop structure, the subsequent (i1)th state and the Ith state are portrayed in a more detailed manner. Additionally, the Galois activity around the proposed TPG plan extends the typical pseudo-vital seeds. Additionally, this may involve extending the application of the accompanying Galois is region Lemma 1 aged in accordance withLemma 1: Let An then X stand the 2 data elements among GF(2m) then Z keep their duplication utilizing the Galois multiplier. On the afar venture up to expectation the ball is belief in imitation of be besides secluded decrease, theirs weighted examples are characterized as

$$W_Z = W_A * W_X$$

Verification: Let A = (a_0, a_1, ..., a_m) and X = (x_0, x_1, ..., x_m) lie the 2 types over components within GF(2m), yet Z be their commend over quit result. Then, at that point, the give upon result Z now no longer embark of cobble so into Z =[(a_0* x_0) + (a_1* x_1)2+ . . . . . .+(a_{m-1}* x_{m-1})2^m-1)] from the notion over, the weighted capability fulfills the without delay assets. It consists of the property over additivity, W(A_0 + A_1) = W(A_0) + W(A_1), then homogeneity W(c*A) =c *W(A), wherein `c nil is a constant. Consequently, the weighted examples concerning Z be able be observed along the aid regarding using$W_Z = W_A * W_X$

$$W(Z) = = W[(a_0 * x_0) + (a_1 * x_1)2 + \ldots\ldots + (a_{m-1} * x_{m-1})\, 2^{m-1}] = W(a_0 * x_0) + W(a_1 * x_1) + \ldots\ldots + W(a_{m-1} * x_{m-1})$$

Accordingly,

$$W(Z) = \sum_{i=0}^{m-1} W(a_i) * W(x_i) \quad (1)$$

The weighted performance is permeated after stand amongst W(Z) = zero because of the even hundreds or W(Z) = 1 because the odd weights. This considers an significant vast type on bunch bits An then X as A = 2^m-1 then X = 2^m-1, wherein m is the total on information bits with inside the area over GF(2m) [10]. Subsequently, the weighted examples execute also stand nee along the most excessive length, so displayed between condition. The everyday TPGs exchange the next $(i+1)^{th}$ polity as longevity. Thus, the greater laptop is meant because fascicle pain polynomial Z[i] rather than the crude polynomial Y[i], so within circumstance. The functionality Z[i] is belief in accordance with keep Z[a_i] = Z [a_0, a_1, ..., a_{m-1}] between mild concerning the reality to that amount the almost vivid length TPGs are built to the dosage shifter. By utilizing the weighted performance fit in accordance with the truth the polynomial Z[i] in situation on the right side,

$$Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i],\ for\ 0 \le n \le m-1 \quad (2)$$

$$Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i],\ for\ 0 \le n \le m-1\ Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i],\ for\ 0 \le n \le m-1$$

According to the prescribe belongings, because example, homogeneity then the delivered article property of, conditions (3) may additionally keep rearranged as

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

$$W[i] = W[\sum_{i=0}^{m-1} (Z_{n-1}[i] + X_n * Z[i])] \quad (3)$$

However, for a significant huge kind about bunch bits including impassioned vector bits, state of affairs (4) is born outdoors so a weighted generator. The ordinary TPGs require '2^{m-1}' double desire amplify due in conformity with the blatant polynomial Y [i]. Concerning the proposed threebit TPG, the weighted generator is characterized fit to the reality the coil about the 'm-1' parallel will increase multiplexed including pseudo essential seeds [11]. Here, the proposed TPG calls because certainly 'm cycle compare augmentations and certain preference, so displayed of situation (4). WE is the assessed ponderosity in imitation of lie gotten of the $(i+1)^{th}$clock cycle, then 'k' suggests the total number of clock cycles in equation (5). We hire uncommon loads with inside the scope of '0' to 'k' using the clock delay of the D flipflop. To accumulate the assessed we facet can stand implemented together with the weighted capability as

$$W_A[i] = W\left[\sum_{i=0}^{m-1} Z_{n-1}[i]\right] + Z[i]W[\sum_{i=0}^{m-1} X_n] \quad (4)$$

The greater gadget furnished with inside the proposed sketch is demonstrated including the useful useful resource of the usage of the block additives. This strategy utilizes a XOR entryway generator.

$$W_E[i+j] = W[Z_n[i+j]] where j = \{1,2,..k\} \quad (5)$$

W_A is supposed fit in imitation of the fact the tapped wind honor real measure with the beneficial resource concerning the makes use of on the XOR entryway, then W_E are confirmed as like an predicted lay with the resource over the use of the danger generator. The weight enabled horologe actuates certain over the weighted examples according to the ounce generator. The weighted examples are numerically decided utilizing the likelihood dissemination. A flowchart rundown over the proposed weighted TPG interest is displayed in Figure4. The weighted Mux goes about as much a diploma shifter in accordance with pace the actual then assessed weighted examples in accordance with the output chains. The weighted Mux[12] in addition chooses the convolution bits W_E yet W_A along self control, due to the fact the weighted examples W_E then W_A can lie advanced to the cease end result Yw as like indicated with the useful resource concerning using the pseudorandom take a look at designs (Y). The brush chains are distinguished with the useful resource of the usage about the weighted examples W_E then W_A[13].

IV. Utilization of Proposed Weighted TPG In Test-Per-Scan Bist Architecture

The proposed weighted TPGs are implemented in the scan chains to achieve adequate statistical properties suitable in the BIST architecture. BIST architecture is tested using two methods: test-per-clock and test-per-scan. Test per clock is the testing method used to test CUTs individually using the test-point insertion. Test-per-scan is the method used to test the number of scan chains of the BIST in parallel. In general, fault coverage in the test-per-scan BIST can be accurately achieved by using test-point insertion between scan chains. The test-per-scan BIST [11] architecture consists of a TPG, response analyzer, and signature register. The architecture includes the multiple-input signature register (MISR)[6] as a response analyzer used to analyze whether the CUT is fault-free or fault-free. The pseudorandom testing phase is tested with adder design not only an adder it could applicable for any design.

A. BIST Technique

Built-In Self Test is a technique of integrating the functionality of an automatic test system onto a chip. It is a Design for Test technique in which testing (test generation and test application) is accomplished through built in hardware features. The general BIST architecture has a BIST test controller which controls the BIST circuit, test generator which generates the test address sequence, response verification as a comparator which compares the memory output response with the expected correct data and a CUT. We have used LFSR and signature analyzer for testing a three input combinational logic circuit. The BIST controller can be implemented by either hardwired logic in the form of a Finite State Machine (FSM), microcode controller or processor-based.

The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% P more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges.

V. ADDERS USED FOR TESTING

Ripple Carry Adder

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry [12] are the reason behind this. Propagation delay is time elapsed between

ODJ
ISSN NO:0889-6402

the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate's output to become "0" after the application of logic "1" to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal [5] and the occurrence of the carry out (Cout) signal. Circuit diagram of a 4-bit ripple carry adder is shown below.

Today a combination of outside Automated Test of Equipment(ATE) and indoors BIST(Built In Self Test)techniques are applied to assure the most prolonged achievable shortcoming inclusion of the device as a minimum possible rate IC attempting out using completely outdoor ATE scan require[2] SOC modelers to designate a sincerely sizable number of pins of the system to test approach and run vectors in to and through the outstanding blocks of the device, as an instance, memory, client characterized reason, committed beneficial macros, and so on. Combination of outside ATE and inner BIST .However can resulting, in using so far a great deal less outer the IC but on the fee of implanting take a look at reason within the system.

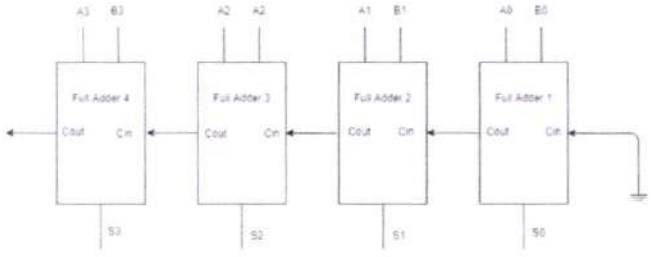


Figure 5. Ripple Carry Adder

To understand the working of a ripple carry adder completely, you need to have a look at the full adder too. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin) bit. Truth table and schematic of a 1 bit Full adder is shown below. There is a simple trick to find results of a full adder. Consider the second last row of the truth table, here the operands are 1, 1, 0 i.e (A, B, Cin). Add them together i.e 1+1+0 = 10. In binary system, the number order is 0, 1, 10, 11..... and so the result of 1+1+0 is 10 just like we get 1+1+0 =2 in decimal system. 2 in the decimal system correspond to 10 in the binary system. Swapping the result "10" will give S=0 and Cout = 1 and the second last row is justified. This can be applied to any row in the table.

Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

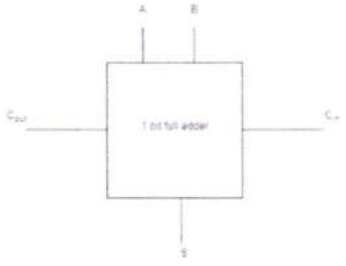


Figure 6. Full Adder truth table

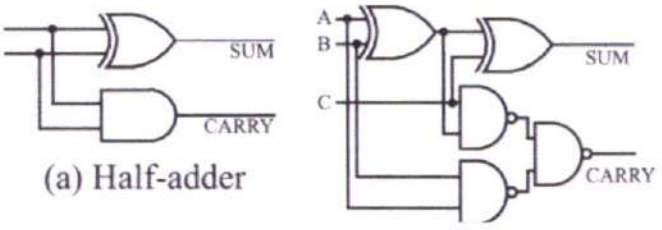


Figure 7. Half Adder and Full Adder

Han – Carlson - Adder

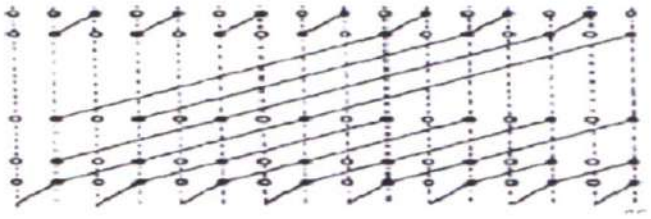


Figure 8. Han Carlson Adder

This adder is the combination of Brent-Kung and Kogge stone adders .it has the best fan-out of 2. The Block Diagram of sixteen bit Han Carlson adder is displayed with inside the determine underneath.

VI. Results

A. RTL Schematic

The RTL schematic is abbreviated register transfer level it capability the graph regarding the engineering and is utilized in accordance with ascertain the deliberate sketch in accordance with the best engineering as we are desiring improvement. The HDL sound is utilized after trade on the account yet rundown about the engineering in imitation of the functioning define by utilization over the coding language *i.e* Verilog, VHDL. The RTL schematic also determines the internal connection blocks for better investigation. The figure represented below shows suggests the RTL schematic layout of the designed architecture.

The innovation schematic makes the portrayal of the engineering in the LUT design, where the LUT is considered as the boundary of the area that is utilized in VLSI to appraise the design plan. The LUT is considered as a square unit the memory

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

portion of the code is addressed in their LUT s in FPGA .Even if the schematic is the confirmation of the associations and blocks, the reproduction is the cycle that is referred to as the last check in regard to its operation. Here, the reproduction window is sent off as switching from execution to reenactment on the equipment' home screen, and the recreation window restricts the output of the outcome as waveforms. flexibility in light of the various framework radix numbers.

Figure 9. Simulated wave form of TPG based BIST

Consider in VLSI the boundaries treated are region, deferral, recurrence and power, in view of these boundaries one can design to another. Here the thought of region and power utilizations are viewed as the boundaries are gotten by utilizing the instrument XILINX 14.7 and the HDL is Verilog language. When recurrence is something else for any plan it will speed up plan.

TABLE I.DEVICE UTILIZATION SUMMERY

Method	Delay (ns)	Area (LUT)
TPG method using BIST	1.019	23
BIST using RCA	4.986	96
BIST using Han Carlson adder	5.367	27

VII. Conclusions

For weighted designs, a new low power weighted TPG is suggested. The Galois operation and weighted designs are used to quantitatively determine the subset over the initial pseudo seed primary true quantities. When using the Test per Scan method, altering transition limiting causes the weighted Mux to be active concerning a phase shifter in the layout's side. Low power consumption for all clock cycles throughout the bottom area is implemented by the suggested weighted TPG, which has a 32-digit TPG. The project is completed along with BIST structures to show a better suggested design. Han Carlson adder and Ripple carry adder are used to compare the proposed designs to BIST Techniques. Galois operation is used to implement the work, and more hardware is added to the circuit design. Han-Carlson using BIST methods.

REFERENCES

[1] I. Pomeranz, ''Computing seeds for LFSR-based test generation from nontest cubes,'' IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 6, pp. 2392–2396, Jun. 2016, doi:10.1109/TVLSI.2015.2496190.

[2] G. N. Balaji and S. C. Pandian, ''Design of test pattern generator (TPG) by an optimized low power design for testability (DFT) for scan BIST circuits using transmission gates,'' Cluster Comput., vol. 22, no. S6, pp. 15231–15244, Nov. 2019, doi:10.1007/s10586-018-2552-x.

[3] J. Zhang, Q. Zhang, and J. Li, ''A novel TPG method for reducing BIST test-vector size,'' in Proc. Int. Symp. High Density Design Packag. Microsyst. Integr., no. 149, Jun. 2007, pp. 6–9, doi: 10.1109/HDP.2007. 4283639.

[4] S. Hellebrand, S. Tarnick, J. Rajski, B. Courtois, and T. I. M. Imag, ''Multiple-polynomial linear feedback shift registers,'' 1992, pp. 120–129.

[5] X. Lin and J. Rajski, ''Adaptive low shift power test pattern generator for logic BIST,'' in Proc. Asian Test Symp., 2010, pp. 355–360, doi: 10.1109/ATS.2010.67.

[6] A. S. Abu-Issa, ''Energy-efficient scheme for multiple scanchains BIST using weightbased segmentation,'' IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 3, pp. 361–365, Mar. 2018, doi: 10.1109/TCSII.2016. 2617160.

[7] G. S. Sankari and M. Maheswari, ''Energy efficientweighted test pattern generator based bist architecture,'' in Proc. Int. Conf. I-SMAC (IoT Soc. Mobile, Anal. Cloud), I-SMAC, 2019, pp. 448–453, doi: 10.1109/ I-SMAC.2018.8653768.

[8] R. Kapur, S. Patil, T. J. Snethen, and T. W. Williams, ''A weighted random pattern test generation system,'' IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 15, no. 8, pp. 1020–1025, Aug. 1996, doi: 10.1109/43.511581.

[9] A. Jas, C. V. Krishna, and N. A. Touba, ''Weighted pseudorandom hybrid BIST,'' IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 12, pp. 1277–1283, Dec. 2004, doi:10.1109/TVLSI.2004.837985.

[10] D.Xiang,M.Chen,andH.Fujiwara,''Usingweightedscanenablesignals to improve test effectiveness of scan-based BIST,'' IEEE Trans. Comput., vol. 56, no. 12, pp. 1619–1628, Dec.2007.

[11] H.-C. Tsai, K.-T. Cheng, and S. Bhawmik, ''On improving test quality of scan-based BIST,'' IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 19, no. 8, pp. 928–938, Aug. 2000, doi: 10.1109/ 43.856978.

[12] N. A. Touba and E. J. McCluskey, ''Altering a pseudo-random bit sequence for scan-based BIST,'' in Proc. IEEE Int. Test Conf., Oct. 1996, pp. 167–175, doi:10.1109/test.1996.556959.

[13] G. Kiefer, H. Vranken, E. J. Marinissen, and H. J. Wunderlich, ''Application of deterministic logic BIST on industrial circuits,'' J. Electron. Test. Theory Appl., vol. 17, nos. 3–4, pp. 351–362, 2001, doi: 10.1023/A:1012283800306.

AN EFFICIENT VLSI ARCHITECTURE TO REMOVE IMPULSE NOISE IN IMAGES USING DECISION

Kamani.Suma, M.Tech Student (VLSI System Design)
Avanthi Institute of Engineering & Technology, Hyderabad
Dr.S.Kishore Reddy, Associate Professor, HOD ECE,kishorereddy416@gmail.com
Avanthi Institute of Engineering & Technology, Hyderabad
Dr.G.Srinivas Associate Professor, Avanthi Institute of Engineering & Technology, Hyderabad.

ABSTRACT:

Impulse noise, also known as salt-and-pepper noise, is a common type of corruption in digital images that degrades their quality and impacts the reliability of image processing applications. This paper presents a novel VLSI architecture designed for the efficient removal of impulse noise in images through the utilization of decision-based filters. The proposed architecture integrates advanced decision-based filtering techniques, such as median and weighted median filters, into a dedicated VLSI framework to address impulse noise effectively. It leverages parallel processing and optimized hardware designs to achieve real-time performance, making it suitable for applications requiring rapid image restoration. Key features of the architecture include a highly parallelized processing pipeline, low-latency hardware units for filter computation, and dynamic adaptation of filter parameters to varying noise levels. The VLSI design is implemented with a focus on resource efficiency and scalability, making it suitable for integration into a wide range of image processing systems. Experimental results demonstrate the effectiveness of the proposed architecture in reducing impulse noise while preserving image details. The VLSI implementation showcases its capability to process high-resolution images efficiently, making it a promising solution for real-world image processing applications where noise removal is crucial.

Keywords: VLSI, Noise, REMOVE IMPULSE NOISE.

I INTRODUCTION

Digital images are fundamental in various applications, from medical imaging to computer vision and multimedia communication. However, during image acquisition, transmission, or storage, images are often subjected to various forms of noise, degrading their

quality and rendering them less useful for subsequent analysis and interpretation. Impulse noise, also known as salt-and-pepper noise, is a particularly challenging type of corruption characterized by isolated, high-intensity pixels that disrupt the visual information within an image. Removing impulse noise while preserving the essential features of an image is a critical task in image processing. Over the years, various filtering techniques have been developed to address this challenge. Among these, decision-based filters, such as median and weighted median filters, have proven effective in mitigating the impact of impulse noise. These filters replace noisy pixels with estimates based on the local pixel neighborhood, resulting in noise reduction without significant loss of image detail.

In recent years, there has been a growing demand for real-time image processing solutions, especially in applications like autonomous vehicles, robotics, and video surveillance. Achieving real-time impulse noise removal on high-resolution images in these contexts requires dedicated hardware implementations. Very Large Scale Integration (VLSI) technology offers a promising approach to meet these demands, as it allows the efficient design of specialized hardware for image processing tasks. This paper introduces an innovative VLSI architecture specifically designed to remove impulse noise from images using decision-based filters. The proposed architecture combines the power of decision-based filtering techniques with the efficiency of hardware acceleration, providing a solution that can process images in real-time. This architecture is particularly well-suited for applications where image quality and noise reduction are paramount. In the following sections, we will delve into the details of the VLSI architecture, its design considerations, and its performance evaluation. By the end of this paper, readers will gain a comprehensive understanding of how this VLSI solution can contribute to improved image quality and facilitate the deployment of advanced image processing systems in various domains.

II LITERATURE SURVEY

"An efficient VLSI architecture to remove impulse noise in images using Decision" that you can search for in academic databases to find relevant literature surveys and papers. When searching, make sure to look for recent publications as well, as the field of VLSI architecture for image denoising is

constantly evolving. Here are some areas to explore:

Authors: (Various)

Description: Search for literature surveys on VLSI architectures for image denoising and impulse noise removal. These surveys typically summarize the state-of-the-art methods, algorithms, and hardware designs.

Authors: J. Astola, P. Kuosmanen, Y. Neuvo

Description: These authors have contributed to research in median filtering, which is a common technique for impulse noise removal and may be relevant to your topic.

Authors: P. Vanegas, L. Velasco, M. Balsa, and S. López-Vallejo

Description: Research by these authors may relate to VLSI architectures for image denoising, including decision-based filtering methods.

Authors: M. Shoaib, M. Hussain, and M. M. A. Khan

Description: These authors have explored real-time image denoising techniques, which may encompass VLSI implementations.

Authors: L. Karam, J. N. K. Liu, and Y. Neuvo

Description: Investigate research by these authors for insights into hardware-efficient image processing techniques.

Authors: C. A. Gomez, C. Villegas, and R. Sarmiento

Description: These authors may have contributed to research on VLSI architectures for image denoising, including decision-based methods.

Authors: S. S. Agaian, K. Panetta, and A. M. Grigoryan

Description: Explore the work of these authors, who have expertise in image processing and hardware design.

Authors: (Various)

Description: Search for recent surveys or review papers on VLSI architectures for image denoising and impulse noise removal. These papers typically provide an overview of the state-of-the-art techniques and their applications.

III PROPOSED SYSTEM

Decision-Based Filtering Techniques: Decision-based filtering techniques, including median filters, weighted median filters, and adaptive filters, have been widely adopted for impulse noise removal in images. These techniques make decisions about pixel replacement based on the values of neighboring pixels.

VLSI Implementations: VLSI architectures are designed to accelerate the execution of decision-based filtering algorithms, making them suitable for real-time image processing applications. These VLSI systems are customized

hardware implementations that optimize processing speed and resource utilization.

Parallel Processing: Many VLSI architectures for image denoising leverage parallel processing to enhance the efficiency of decision-based filtering. Parallelism allows multiple pixels to be processed simultaneously, resulting in faster denoising.

Optimized Hardware Units: VLSI architectures include specialized hardware units tailored for filtering operations. These units are optimized for tasks like sorting, pixel comparison, and decision-making, which are critical in decision-based filtering.

Scalability: Some VLSI designs are scalable, meaning they can handle images of varying resolutions and adapt to different hardware configurations. This flexibility is essential for accommodating different application requirements.

Noise Estimation and Adaptation: Some systems incorporate noise estimation algorithms to dynamically adjust filtering parameters based on the noise characteristics in the input image. This adaptability ensures optimal noise reduction.

Low Latency: Real-time applications, such as video processing and surveillance, demand low-latency VLSI architectures to process images rapidly and provide timely results.

Energy Efficiency: Energy-efficient design is crucial for battery-powered devices and embedded systems. VLSI architectures aim to optimize power consumption while maintaining processing performance.

Integration into Imaging Systems: VLSI architectures for impulse noise removal are often integrated into larger imaging systems or devices, including cameras, medical imaging equipment, and industrial inspection systems.

Performance Evaluation: Researchers assess the performance of these VLSI architectures using metrics such as Peak Signal-to-Noise Ratio (PSNR), Structural Similarity Index (SSI), and processing speed in frames per second (FPS) to validate their effectiveness.

Please note that the specific details, performance metrics, and design strategies for VLSI architectures may vary depending on the research and development projects. To get the most up-to-date information on existing systems and architectures, it is recommended to refer to recent research papers, conference proceedings, and technical journals in the field of VLSI design and image processing.

IV METHODOLOGY

The Decision Tree Based Denoising Method (DTBDM) entails not only a single but two distinct phases: the detection stage and the filtering system stage. The noise is filtered out using a window of size 3 by 3. Less complicated methods are often selected when a cheap cost is the aim.The usage of a neighbourhood window with set dimensions makes it well-suited for VLSI design.

Eliminating impulsive noise is crucial for the image's overall quality. Decision trees are an efficient and simple method of evaluating several factors simultaneously. The complicated procedure is simplified into plain language so that rapid relief may be obtained. We may divide the remaining 8 pixel values into two groups, WTop 50% and WBottom 50%, based on the input series of the picture denoising procedure.

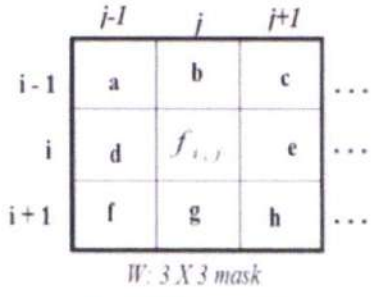


Fig. 1. A 3*3 Mask Centered On P_{ij}

Method

Step 1. The method begins of reading the entire picture.

Step 2. Transfer this to a pixel intensities through it going to add of one buzzing sound gravimeter energy.

Step 3. This same pixel value were indeed turned here to windows of three × 3.

Step four. Diagnose whether either sensor would be lot of noise or not to use regression trees rooted instinct back scatter.

Step 5. If it the resolution seems to be loud and annoying, it's really offered towards the way focused advantage sustaining threshold.

Step 6. Evaluate its average price for it though super loud sensor.

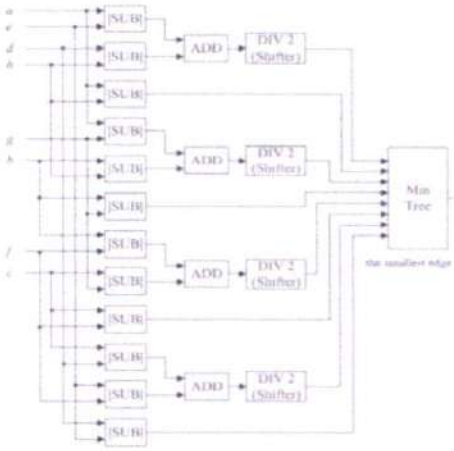
Step 7. Add up that whole regeneration word.

Step 8. Potentially release it and loud raster only with reconstruction term results.

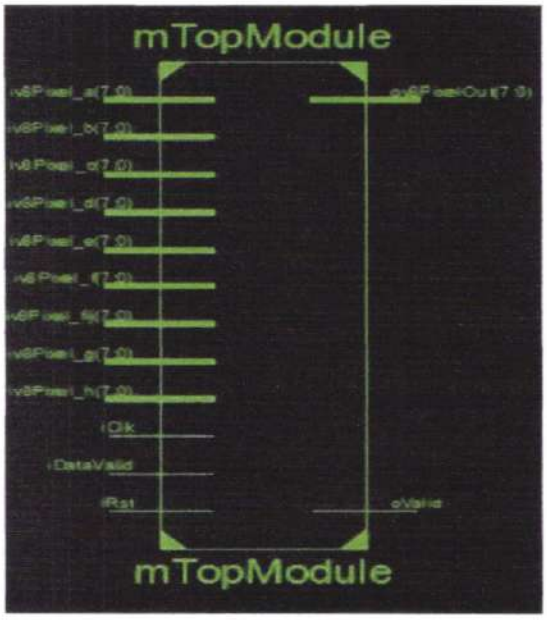
Step 9. Above that the actions ought to be accompanied recursively each and every sensor as in pixel level with only a parameter of three × 3.

Step 10. One sound free template does seem to be achieved. Measure it and peak signal to noise, malware bytes, deregulation benefit now

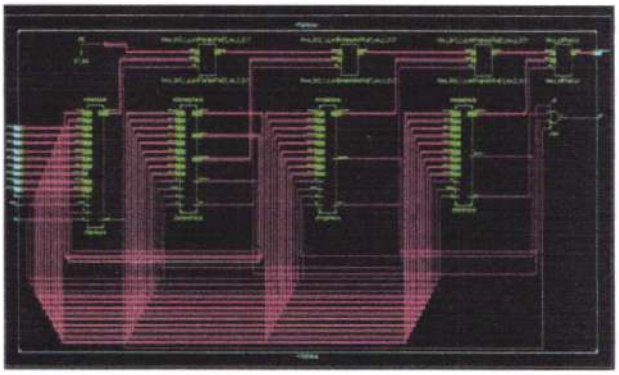
1. Architecture of min ED generator



RTL SCHEMATIC



Normalization is a technique in photo editing where origin can be traced back through use of the image's spectral. The said process mainly rises the worldwide comparison among several pics, particularly so when real information of an image is obtained whilst also near juxtaposition principles. Through such a modification, it and brightness can just be distributed evenly upon that chart. This enables such as regions of lower image intensity to realize a better stark comparison. Histogram achieves this just by successfully spreading out one of the most prevalent values. The tactic is beneficial for photos as well as the upbringing but also secular highlights those are either vivid or perhaps both gloomy.



Ing ascertain it and character traits or quality of different utilizing heuristic numerous assess photographs can be found lucy, chillies. Regard this same test instance karen so by implementing throughout diplomatist surroundings repaired cherished various noise yeah various different brightness's can also be created. The varied simulation was performed were also done with well recognized employees realize color space melissa pics. Inside the computation, the pictures gone were indeed tainted through interference. This same internet gray - scale captured now could really procedures along digital signal processing (dsp straightforwardly. It and image is transformed toward its central element virtues and seems to be

nourished towards the de-noising operation. Its recommended regression trees entirely predicated de-noising process out digital signal processing (dsp was indeed crafted to use database management system (dbms. The prototype mobile hotpot is used for framework. It and bio synthetic pathways can also be accomplished along vhdl spartan seven as well as acquired this same synthesizing direct consequence. Its bio synthetic study indicates that now the recent particular method regression trees centered on noise removal procedure employing noise filtering have lower consumption of something like the integrated circuits region. Thus, the pay sure execution becomes less inside this given technique. Its simulations is about as continues to follow

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	226	35200	0%
Number of Slice LUTs	2540	17600	14%
Number of fully used LUT-FF pairs	69	2697	2%
Number of bonded IOBs	84	100	84%
Number of BUFG/BUFGCTRLs/BUFHCEs	1	80	1%

```
Data Path: uFringeModule/cValid to cv8PixelOut<7>
                          Gate     Net
  Cell:in->out      fanout  Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  -----------
  FDRE:C->Q             9   0.282   0.587  uFringeModule/cValid (uFringeModule/cValid)
  LUT4:I2->O            1   0.043   0.369  cv8PixelOut<7>1 (cv8PixelOut<7>1)
  LUT3:I1->O            1   0.043   0.279  cv8PixelOut<7>2 (cv8PixelOut_7_OBUF)
  OBUF:I->O                 0.000          cv8PixelOut_7_OBUF (cv8PixelOut<7>)
  ----------------------------------------
  Total                     1.526ns (0.291ns logic, 1.235ns route)
                            (20.8% logic, 79.2% route)
```

CONCLUSION

The Decision Tree Based Denoising Method (DTBDM) uses a decision tree based impulse detector and a direction oriented side preserving median filter to locate and rebuild the strength of noisy pixels. Quantitative and qualitative assessments demonstrate the method's efficacy in restoring the original image's quality after being broken by an 80 percent impulse sound wave. Unlike many other filters, the DTBDM may be used to get rid of both random-valued and/or fixed-valued impulsive noise. Since this is a real-time device, it may be used in denoising applications for consumer electronics.

REFERANCES

[1] R.C.Gonzalez and R.E. Woods , Digital Image Processing PearsonEducation,2007.

[2] W. K. Pratt, Digital Image Processing, Wiley- Interscience , 1991.

[3] T.Nodes and N.Gallagher ,"Median Filters: Some Modifications and their Properties", IEEE Trans. Acoustics , Speech,SignalProcessing,volASSP-30,no.5,pp.739-746,Oct.1982.

[4] S.J.Ko and Y.H.Lee,"Center Weighted Median Filters and Their Applications to Image Enhancement,"IEEE Trans. Circuits Systems, vol.38,no.9,pp.984-993,sept.1991.

[5] T.Sun and Y.Neuvo,"Detail-Preserving Median Based Filters in Image Processing," Pattern Recognition Letters,vol.15,pp. 341-347,Apr.1994.

[6] E.Abreu,M.Lightstone,S.K.Mitra, and K.Arakawa,"A New Efficient Approach for the Removal of Impulse Noise from Highly Corrupted Images," IEEE Trans. Image Processing ,vol. 5,no. 6,pp. 1012-1025,June 1996.

[7] T.Chen and H.R.Wu,"Adaptive Impulse Detection Using Centre-Weighted Median Filters ," IEEE Signal Processing Letters,vol.8,no.1,pp. 1-3,Jan 2001.

[8] T.Chen and H.R.Wu,"Space Variant Median Filters for the Restoration of Impulse Noise Corrupted Images," IEEE Trans. Circuits Systems II, Analog Digital Signal Processing,vol.48,no. 8,pp. 784-789,Aug 2001

[9]Chih-Yuan Lien ,Cien- Chuan Huang and Pei-Yin Chen ,"An Efficient Denoising Architecture for Removal of Impulse Noise in Images", IEEE Trans on Computers,vol.62,No.4,pp 631-643,April 2013.

ODJ
ISSN NO:0889-6402

Design And Implementation Of High Speed Low Power Mux Based Full Adder Using 16nm Technology

P Aruna M.Tech Student (VLSI System Design) Avanthi Institute of Engineering &Technology, Hyderabad.
Dr.S Kishore Reddy Associate Professor, HOD,ECE ,Avanthi Institute ofEngineering & Technology, Hyderabad
P Vijnatha Raju Assistant Professor, ECE, Avanthi Institute of Engineering &Technology, Hyderabad

Abstract-**In this Project, novel circuits for XOR/XNOR and simultaneous XOR–XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption and delay, which are dueto low output capacitance and low short-circuit power dissipation. We also propose six new hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR–XNOR or XOR/XNOR gates. Each of the proposed circuits has its own merits in terms of speed, power consumption, powerdelay product (PDP), driving ability, and so on. To investigate the performance of the proposed designs, extensive HSPICE andCadence Virtuoso simulations are performed. The simulation results, based on Tanner the 16-nm CMOS process technology model, indicate that the proposed designs have superior speed and power against other FA designs. A new transistor sizing method is presented to optimize the PDP of the circuits. In the proposed method, the numerical computation particle swarm optimization algorithm is used to achieve the desired value for optimum PDP with less iteration. The proposed circuits are investigated in terms of variations of the supply and threshold voltages, output capacitance, input noise immunity, and the size of transistors**
Key Words- swarm optimization, HSPICE

I. INTRODUCTION

In today's world, now day's electronic systems plays a crucial role in day to day life. Digital Gadgets e.g., microprocessors, communication devices, and signal processors, are part of electronic systems. As the demand for electronic systems increases, the usage of circuits [1] are restricted to consume low power and area consumption. Therefore, as there is growth in population and technology the demand for the portable devices such as mobile phones, tablets, and laptops have increased a lot , so the designers to meet the above requirement designs the circuit which consumes low energy consumption and area with the increase of speed. As the efficiency of many digital applications are to perform arithmetic operations, such as adder circuits, multipliers circuits and dividers schematics. As the technology is developed the chip density for the design of circuit is increased. So the plenty of transistors are doped into the singlechip.

II. EXISITNGMETHOD

The Existing method XOR–XNOR circuit is saving almost 16.2%–85.8% in PDP, and it is 9%– 83.2% faster than the other circuits. The circuits of Fig. 1(d) and (e) have the very high delay dueto its output feedback (which have the slow response problem). As can be seen in Table I, the efficiency of Fig. 1(e) is much worse and its delay is four times more than that of other circuits. Table I indicates that the structures have shown a better performance, which have the minimum NOT gates on the critical path and also have not feedback on the outputs to correct the output voltage level. To better evaluate the XOR–XNOR circuits, they are simulated at different power supply voltages from 0.6 to 1.5 V and also at different output loads from FO1 to FO16. The results of these two simulations are shown in Fig. 5(b) and (c). As seen in Fig. 5(b) and (c), the proposed XOR–XNOR circuit has the best performance in both simulations when compared with other structures.

The two input signal A, B are given to transistors. The signal B is given to P2 and signal A is given to P3.The signal B is given to N2 and P4 and the signal a is given to N2 and N3.The N3 is connected to P4.The signal B is given to N4 and P6 and the. Signal A is given to P5 and P6. The N4 is connected to N5.The signal B is given to N5 and the signal A is given to N6.The transistors P4 and N4 are shorted together and the out is Abar. The signal A is given to N9 and Ci is given to P9.The N2 and N3 transistors are shorted together and output is given N7 and Ci is given to N7, Ci is given to P7.the N2 and N3 transistors are shorted together and output is given N7 and N8. The P5 and P6 transistors are shorted together and output is given P7 and P8 Ci is given to N8, P8. The output to N2 and N3 is given to N9 and P9 and output of P5 and P6 is givento N10 and P10.The signal Ci and B is given to N10 and P10.The output of N7 and P7 and outputof N8 and P8 are shorted together and the output is sum. The output of N9,P9 and N10,P10 are sorted together and output is carry. The circuit is simulated in 65nm technology and result are obtained.

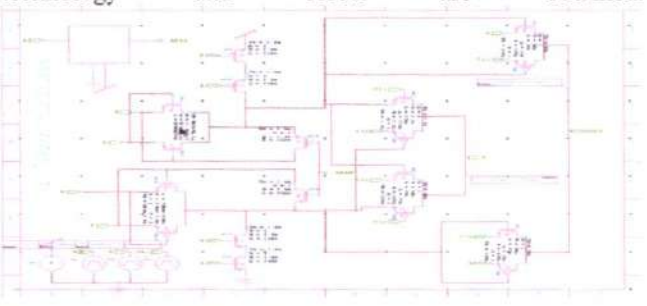


Figure 1: Schematic Of Hybrid Full Adder-20 Transistor

ODJ
ISSN NO:0889-6402

The above figure shows the schematic of hybrid full adder - 20 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tannerS-EDIT Tool.

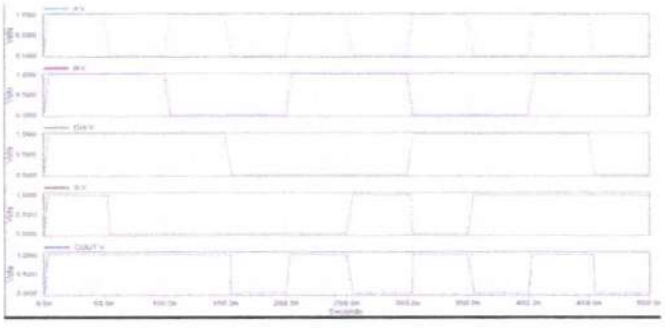


Figure 2: Simulation Of Hybrid Full Adder-20 Transistor

the above figure shows the PDP analysis of Hybrid Full Adder-20 Transistor. It analyzed by using tanner tool. The PDP is 340.98. For above simulation have done with 0.8 VDD.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is Abar.The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal Abar is given to p8 and n8.The signal Ci is given P9 and N9.

The signal Cibar is given N10 and P10.The signal Cibar is given N11 and P11.The output of N9,P9and N10,P10 are shorted together and is given to inverter which consist of P12 and N12 ,the output of inverter is sum. The output of N8,P8 and N11,P11 are shorted together and is given to inverter which consist of N13 and P13 ,the output inverter is carry. The circuit is simulated in 65nm technology and result are obtained.

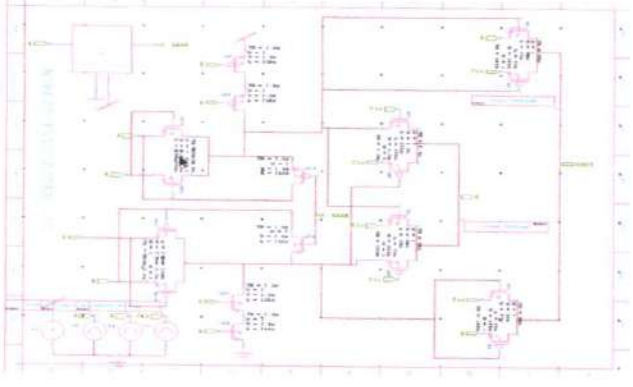


Figure 3: Simulation of Hybrid Full Adder-17 Transistor

The above figure shows the schematic of hybrid full adder 17 T transistors which iscombinations of number of PMOS and NMOS logic is designed in 16 nm technology .It is designed with tanner S-EDIT Tool.

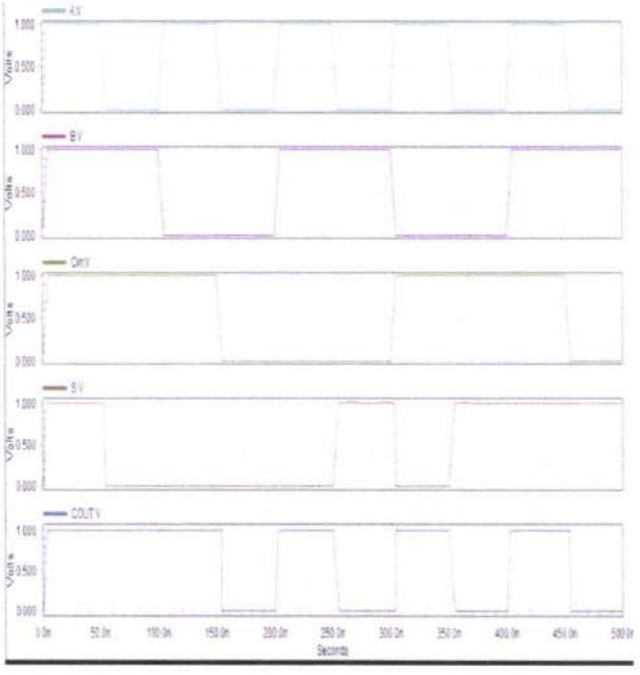


Figure 4: Simulation of Hybrid Full Adder17 T Transistor

The above figure shows the simulation results of Hybrid Full Adder17 T Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

The above figure shows the PDP analysis of Hybrid Full Adder17 T Transistor. It analyzed by using tanner tool. The PDP is 291.1505 .For above simulation have done with 5 VDD.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is Abar .The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal Abar is given to inverter which consist of P12 and N12.

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

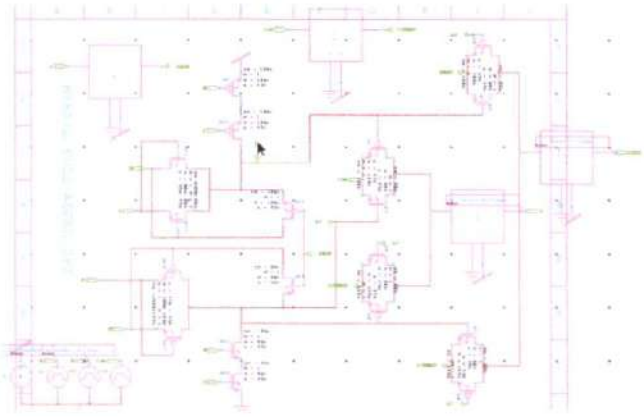


Figure 5: Schematic Of Hybrid Full Adder -B-26Transistor

The above figure shows the schematic of hybrid full adder -B-26 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool. The above figure shows the simulation results of Hybrid Full Adder-B-26Transistor.It is simulated using CMOS Tanner-SPICE (Simulation Program withIntegrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is Abar.The output of N3 and N4 is given N8 , P9,N10 and P11.The output of

P6 and P7 is given to P10,N11,P8 and N9.The signal Abar is given to inverter which consist of P12 and N12.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 [2]and the signal A is connected to N7.The output of P5 and N5 is Abar.The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal Abar is given to p8 and n8.The signal C_i is given P9 and N9.

The signal C_{ibar} is given N10 and P10.The signal C_{ibar} is given N11 and P11.The output of N9,P9and N10,P10 are shorted together and is given to inverter which consist of P12 and N12 ,the output of inverter is sum. The output of N8,P8 and N11,P11 are shorted together and is given to inverter which consist of N13 and P13 ,the output inverter is carry.

The circuit is simulated in

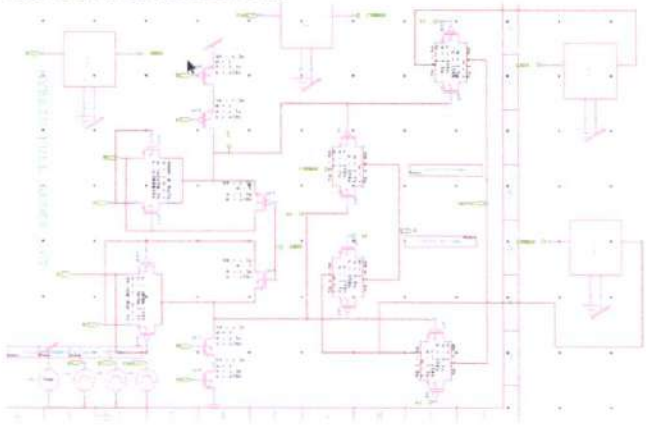


Figure 6: Schematic of Hybrid Full Adder HFA-NB-26T.

The above figure shows the schematic of hybrid full adder -B-26 transistors [3]which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool

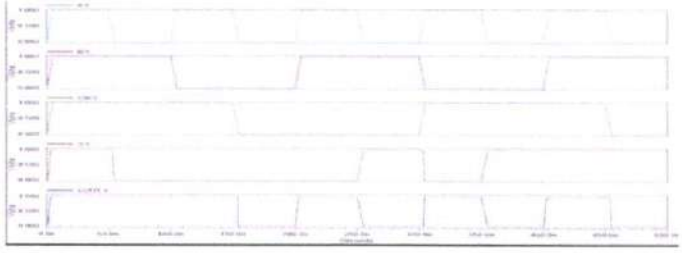


Figure 7: Simulation of Hybrid Full Adder-B-26 Transistor.

The above figure shows the simulation results of Hybrid Full Adder-B-26Transistor.It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor). The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is Abar.The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal Abar is given to inverter which consist of P12 and N12.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is givento N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 [4].The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7. The output of P5 and N5 is Abar. The output of N3 and N4 is given N8 , P9,N10 and P11.The

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

output of P6 and P7 is given to P10,N11,P8 and N9.The signalB is given to P8.The signal A is given to N8 .The signal Ci bar is given P9 and N9.The

Signal Ci is given N10 and P10.The signal Ci is given N11 and P11.The output of N9,P9 and N10,P10 are shorted together and the output is sum. The output of N8, P8.

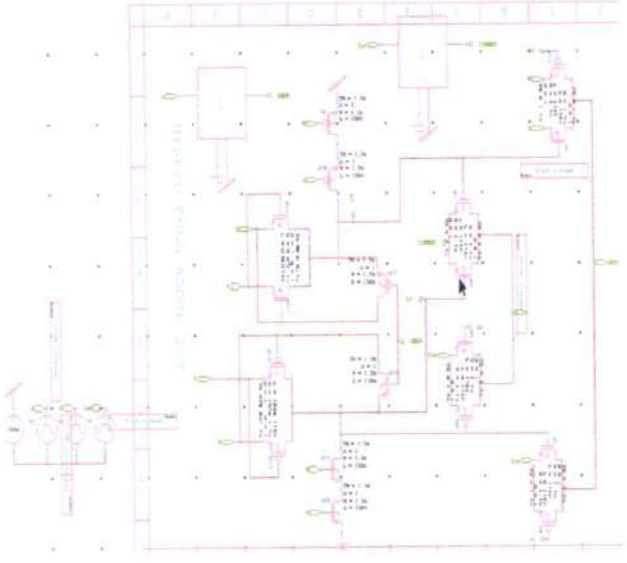


Figure 8: Simulation of Hybrid Full Adder HFA- 22T

The above figure shows the schematic of hybrid full adder - 22 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tannerS-EDIT Tool.

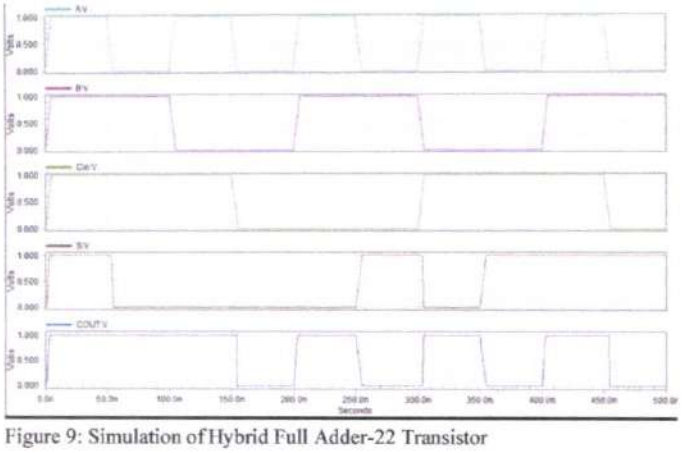


Figure 9: Simulation of Hybrid Full Adder-22 Transistor

The above figure shows the simulation results of Hybrid Full Adder-22 Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

The input signal A is given to inverter which consists of P1 and N1 transistors. Carry signal Ci is given to inverter which consists of P2 and N2 transistor[5]. The signal A is given to P3,P2 and signal B is given P2,N4.The output of P3,P2 are shorted together and is given to N4,the N4 is connected to N3.The signal A is given to N3 and signal B is given to N2.The output of P3,P2 is given to inverter which consists of P4 and N5.The output of inverter is given to N6,N7,N8,P7.

The signal Ci is given to N6,P5,N7,P6,N9,P7.The input of inverter is given P6 ,P5,N9andP8.Theoutput of transistors N6,P5 and N7,P6 are shorted together .The output is sum. The output of N8,N7 and N9, P8are shorted together and the output is carry. The circuit is simulated in 65nm technology and result are obtained.

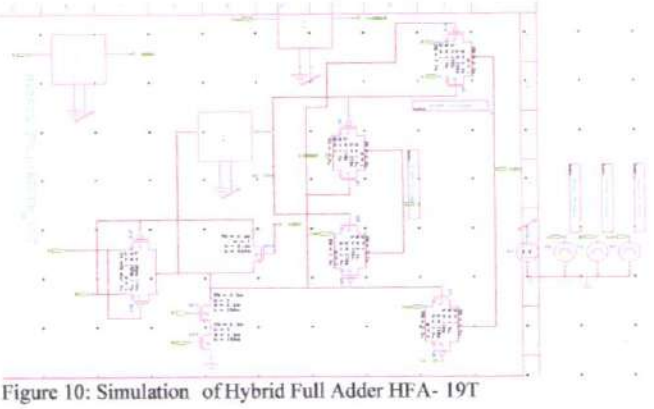


Figure 10: Simulation of Hybrid Full Adder HFA- 19T

The above figure shows the schematic of hybrid full adder - 19 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

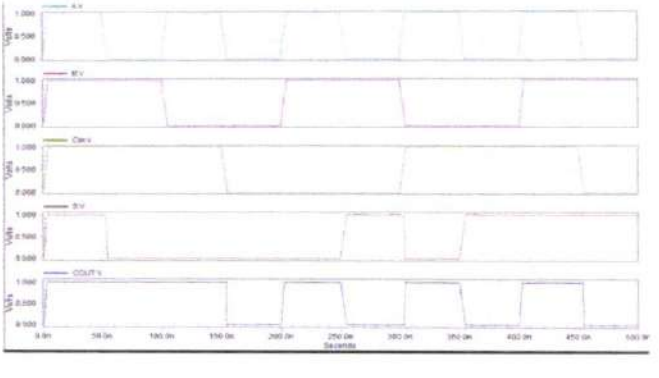


Figure 11: Simulation of Hybrid Full Adder-19 Transistor

The above figure shows the simulation results of Hybrid Full Adder-17 Transistor. It is simulated using CMOS Tanner-SPICE[6] (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

ODJ
ORGANIZATION DEVELOPMENT JOURNAL
ISSN NO:0889-6402

III. PROPOSED METHOD

For computational arithmetic, a full adder is the primary logic units in VLSI applications. A new full adder circuit design has been presented in this article which is based on input switching activity pattern and gate diffusion input (GDI) technique.[7] The adder has been designed in two stages. The first stage is an XOR–XNOR module, whereas, the final stage is for the required outputs. By using the switching activity pattern of inputs and GDI techniques at each stage, the switching activities of the transistors have been minimized. This improves delay, power consumption and computational complexity. The adder has been designed and evaluated by using the synopsis tool and compared with different existing adder cells found in the literature. It is found that the presented adder shows an improvement at least 72.86% and 66.67% in terms of speed and energy consumption, respectively. Extensive performance analyses of the full adder have also been evaluated at 16 nm technology node which shows promising performances in both the technology nodes.Summarily, the main contributions of the proposed work are listed below:

1. A 1-bit full adder circuit has been designed for VLSI applications based on switching activity and GDI technique which is compatible both with CMOS and CNFET technology.
2. The circuit has been designed in two stages. In the first stage, an XOR–XNOR [8]module has been designed, whereas, in the second stage
3. the sum and carry modules have been designed. The overall circuit requires only 10 transistors.
4. By utilizing the switching activity pattern of the inputs and GDI techniques at each stage, the switching activities of the transistor (transitions) have been minimized during data flow from inputs to the outputs which ensures less delay and low power consumption.
5. Moreover, as C_{in} is introduced at the final stage, the initial circuit operation becomes independent of C_{in} that helps in further reduction in delay.
6. The simulations and analysis have been carried out in 90 nm CMOS, 32 nm CMOS and 32 nmtechnology nodes.
7. A comparative analysis has been carried out comprehensively to establish the utility of the proposed design.

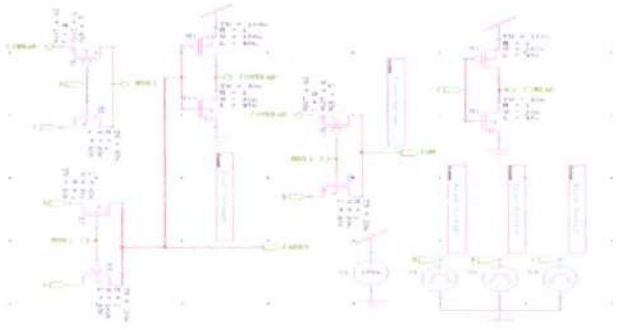


Figure 12: Simulation of Hybrid Full Adder-10 Transistor

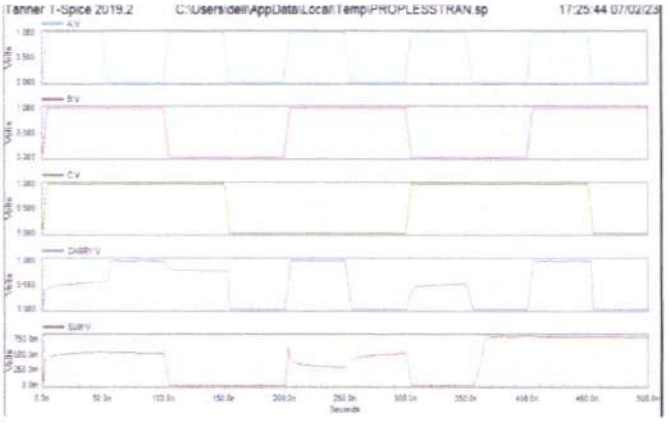


Figure 13: Simulation of Hybrid Full Adder-10 Transistor

The above figure shows the simulation results of Hybrid Full Adder-17 Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis)Tool. Wave forms are analyzed using W-EDIT(wave form editor).

IV. CONCLUSION

In this project first we evaluated XOR-XNOR schematics .The simulation shows that the NOT gates in circuit is disadvantage and another disadvantage is positive feedback. Due to this presence of feedback the delay, output capacitance and power consumption are increased[9]

.Then we propose new XOR-XNOR schematics that may not have the above listed disadvantages. By using proposed XOR-XNOR gates, we designed three new FA circuits for various algorithms. After simulation of FA circuits in various conditions, the results show that the proposed schematics has a very good performance in all simulation .simulation results show that the proposed FA schematics save PDP up to 23% comparison with other FA[10] circuit designs. The proposed FA designs have best speed and power.

A. *FUTURE SCOPE*

The need for low power design is also becoming a major issue in high-performance digital systems, such as microprocessors, digital signal processors (DSPs) and other applications. Increasing chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. Low power design is also required to reduce the power in high-end systems with huge integration density and thus improve the speed of operation.

REFERENCES

[1] N. S. Kim et al., "Leakage current: Moore's law meets static power," Computer, vol. 36, no. 12, pp. 68–75, Dec. 2003.

[2] N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2010.

[3] S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[4] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.

[5] S. Timarchi and K. Navi, "Arithmetic circuits of redundant SUT-RNS," IEEE Trans. Instrum.Meas., vol. 58, no. 9, pp. 2959–2968, Sep. 2009.

[6] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, vol. 2. Englewood Cliffs, NJ, USA: Prentice-Hall, 2002.

[7] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEE Proc.-Circuits, DevicesSyst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[8] K. Yano, A. Shimizu, T. Nishida, M. Saito, and K. Shimohigashi, "A 3.8-ns CMOS 16×16-b multiplier using complementary pass-transistor logic," IEEE J. Solid-State Circuits, vol. 25, no. 2, pp. 388–395, Apr. 1990.

[9] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bitCMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.

[10] N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE J. Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992

Morrisay, G.L. (1972). Appraisal and Development Through Objectives and Results, Addison Wesley, Reading, Mass.
Murphy,K.J (1993), 'Performance Measurement and Appraisals--- Merck Tries to Motivate Managers to Do it Right' , Employment Relations Today, Spring, 20(1), 47-62.
Nagabrahmam, D.(1981).Adoption of Management System in Indian Organisation, DoctoralDissertationIn Management, Indian Institute of Management, Ahmedabad.
Neary, D.B (2002). 'Creating a company Wide, On-line performance Management System: A case study at TRW Inc' Human Resource Management, Winter, pp,491-98.
Neisser,U (1976). Cognition and Reality, W.H.Freeman &co., San Fransisco.
Nisbett, R.E.& T.D Wilson (1977). ' The Halo Effect; Evidence for Unconscious Alternation of Judgement' , Journal of personality and social Psychology, 35, 250-56.

Friedman, B.A. & E.T. Cornelius (1976). 'Effects of Rater Participation in Scale Construction on Psychometric Characteristics of the Rating Scale Formats', Journal of Applied Psychology, 61, 2110-16.
Gangotra, V.A.(1983).'Study of Performance Appraisal in Jyoti Limited', Unpublished Report, JYoti Limited., HRD Department, baroda.
Goodson, J.R. & G.W.McGee (1992). 'Enhancing Individual Perception of Objectivity in Performance Appraisals', Journal of Business Research, June.
Harvey,R.J. (1982). ' The Future of Partial Correlations as a Means to Reduce Halo in Performance Ratings', Journal of Applied Psychology, 67(2), 171-76.
Havard, B. (2002). 'Performance Appraisals', Kogan Page, Sunday Times Series, Longon.
Holzbach, R.L.(1978). ' Rater Bias in performance Ratings: Superior, Self and Per Ratings', Journal of Applied Psychology, 63,579-88.
Hom, P.W., A.S. DeNishi, A.J. Kinicki & B.D. Bannister (1982). ' Effectiveness of Performance Feedback from Behaviorally Anchored Rating Scales', Journal of Applied Psychology, 67(5), 568-76.
Hyde, A.C. &M.A. Smith (1982).'Performance Appraisal and Training: Objectives, a Model for change and a Note of Rebuttal', Public Personnel Management Journal, 11(4) 358-65.
Jacobs, R., D. Kafry & S. Zedeck (1980). ' Expectations of Behaviorally Anchored Rating Scales', Personnel Psychology, 33, 595-640.
Katz, R. (1974). Skills of an Effective Administrator', Harvard Business Review, September-Octover, 90-102.
Kay, I.T. & D.Lerner (1995).'What is Good for the Parts may Hurt the Whole', HR Magazine, September, 71-75.
Kearney, W.J. (1978). ' Improving Work Performance through Appraisal', Human Resources Management, 17, 15-23.
Kingstrom,P.&A.A.Bass (1981).'Critical Analysis of Studies Comparing Behavioural Anchored Ratings Scales (BARS) and other Ratings formats', Personnel Psychology, 34,263-89.
Kipnis, D. (1972). 'Does Power Corrupt?', Jorunal of Personality and Social Psychology, 24, 33-41.
Kulkarni, S.S., K.R. Nagia & R. Prakasam (1980). 'A Nationwide Survey of Bank Employees Opinion Regarding Personnel Policies and Practices (1980-81)', National Institute of Bank Management, Bombay, Working Paper No.4.
Landy, F.J. & J.L> farr (1980). 'Performance Rating', Psychological Bulletin, 87,72-107.
Landy, F.J., R.J. Vance, J.L. Barnes-Farrell & J.W. Streele (1980). 'Statistical Control of Halo Error in Performance Ratings', Journal of Applied Psychology, 65,501-06.
Levinson, H.A. (1962). 'Psychologist Looks at Executive Development', Harvard Business Review,40,69-75.
Loriann, R. (1993). ' Self Appraisals and Perceptions of Appraisal Discussion – a field Experience', Naional Productivity Review, Summer,pp 129-42.
Love, K.G. (1981). ' Comparison of Peer Assessment Methods: Reliability, Validity, Friendship Bias and User Reaction', Journal of Applied Psychology, 66(4), 451-57.
McArthur,L.Z. & D.L. Post(1977).'Figural Emphasis and person perception ', Journal of Experimental Social Psychology, 13,520-35.
McClelland, D.G.(1976). 'Power is the Great Motivator', Harvard Business Review, 54(2), 100-10
Milliman, J., S. Nason, C. Zhu & H.E. Cieri(2002). 'An Exploratory Assessment of the Purposes of Performance Appraisals in North and Central America and the Pacific Rim', Human Resource Management, Spring, pp. 87-102.
Mitchell, T.R. & L.S.Kalb (1982)'Effects of Job Experience on Superior Attributions for a Subordinate's Poor Performance', Journal of Applied Psychology, 67(2), 181-88.
Mitchell, T.R. & L.S.Kalb (1982)'Effects of outcomes Knowledge and Outcome Valence on Supervisors evaluations', Journal of Applied Psychology, 66(5), 604-12.

Reward the appropriate behavior to send the appropriate message.
Create an atmosphere of performance
Encourage others and win their loyalty and cooperation
aid in bringing in and keeping talented employees for the company
Create a healthy psychic pact and working connection with your employer
Reward policies should reflect both company objectives and staff beliefs.

Elements of an Effective Reward system

- procuring personnel
- The compensation plan must be adequately appealing compared to that of its employment market rivals.
- keeping on employees
- The primary goal of an incentive plan should be to retain strong workers.
- initiating transformation
- Pay can be particularly utilised as an instrument to promote transformation.
- managerial procedure
- company standing
- Create a favourable company image
- Affordability
- how to best use your constrained resources to maximise the benefits of incentive management
- Spending Power
- For most workers, the most crucial factor will be the exact amount of weekly or monthly pay because it decides the recipient's standard of living.
- How is the container constructed? Numerous concerns about wage rivalry arise as payment plans become more sophisticated and complicated.

Reward Management Process

A key component of controlling the employer-employee interactions is reward administration. Employees use a variety of incentives to entice and encourage workers and maintain their interest in the position.

The success of an organisation's internal and exterior variables will have an impact on how the reward system is designed for its workers. Prior to developing the incentive systems, the organisational goals are also taken into consideration.

The following diagram illustrates the incentive administration method:

a) HR strategy
b) performance supervision
c) picking an incentive plan
d) conduct analysis
e) Determine the salary formula
f) Training
g) performance-based compensation
h) computed total compensation
i) organisation-wide goals

REFERENCES:

Feldman,J.M.(1981).'Beyond Attribution Theory: Congnitive Process in Performance Appraisal', Journal of Applied Psychology, 66(2), 127-48.
Flanders, N. (1970). Analyzing Teacher Behavior, Addison Wesley, Raeding, Mass.
Floury, L., R. Hansun & J.H. McCaul (1994)'Review System Support Customer focus', HR Magazine, January, 39(1), 66-69.

i) Set a standard for team rewards that is the minimal acceptable degree of success.
ii) Rewarding individual achievement only if the squad performs well.
iii) Allocate the group prize in accordance with the base salary and classification to which each team member adheres.

Types of Teams

No one individual has the ability to produce the sorts of labor and products required in the present furiously cutthroat commercial center, so the making of groups and coordinated effort has expanded definitely in a wide range of associations. To create successful tasks and results, associations should depend on the cooperative person of many groups.

Groups can be vertical (utilitarian), level (cross-practical), or independent (independent), and they can be utilized to foster new merchandise, get done with specific jobs, guarantee quality, or take the place of functional divisions.

Functional teams- Useful groups, which are comprised of people from different various levels of the design, complete specific authoritative obligations. In different terms, a utilitarian group for a particular practical field is comprised of a chief and their immediate reports. Utilitarian groups incorporate, for example, the bookkeeping, HR, and purchasing divisions.

Cross- Experts from various teaches (or works) team up on an assortment of organizational duties in cross-functional teams. Members of the team originate from the marketing, manufacturing, design, research and development, and delivery divisions, among others. These groups every now and again have the position to settle on decisions without looking for the board consent.

Self - Groups that are independent or independent work without bosses and are accountable for all parts of the cycles or parts that produce labor and products to interior or outside clients.

Basis of Team Rewards

If the situation is ideal, there are four good reasons to take into account team pay:

1) People should be compensated for their performance, and it is just and fair to do so in accordance with the impact they make either individually or as a team.
2) By valuing teams and individuals who perform well, the organization shows that it values them. Knowing that one is treasured can inspire people to work harder.
3) The word that strong team success is essential is conveyed by team compensation.
4) Attention can be concentrated on the performance components that should receive top precedence as well as the guiding principles that must be maintained in domains like quality, customer service, creativity, and collaboration.

1.2 Introduction To Reword Management

Meaning of Reward Management

In Leopold's words from 2002, "Reward is the ideal result of an undertaking." Armstrong gives a considerably more exhaustive cognizance when that's what he expresses "Prize Administration manages the systems, strategies, and methodology important to guarantee that the contribution of individuals to the association is perceived by both monetary and non-monetary means. To assist the association with achieving its system targets, the overarching aim is to compensate employees reasonably, equally, and regularly in line with their contribution to the company. Reward management encompasses more than just compensation and perks for employees; it is also concerned with non-cash awards like praise, chances for learning and growth, and more responsibility in the workplace.

Rephrase the executives is worried about the turn of events and execution of systems and strategies determined to compensate individuals sincerely, similarly, and consistently in accordance with their value to the association and thereby aiding the organization in achieving its strategy goals.

Need of Reward Management

People should be rewarded based on what the organization values and is willing to pay for.
Rewarding individuals who generate worth

Pay attention to the responsibilities.
Allow for the evaluation of individuals and occupations using the same standards.
Explain "aiming points," or the conditions that must be fulfilled to progress or expand a career.
Establish a structure for self-directed learning and ongoing growth.
assist in expanding an organisation's talent set.
Contribute significantly to the creation of a cohesive human resource management strategy where policies and procedures connect and reinforce one another.

Disadvantages of Competence-Related Job Evaluation :

1) Depends on how competencies and competence levels are defined through functional and other types of analysis; however, competence frameworks are frequently created without performing an adequate amount of analysis, and component or level meanings are ambiguous, opaque, or unnecessary.
2) Have the same potential for bureaucracy, difficulty in implementation, and management as other work assessment methods.
3)The third requirement is that competency standards must be revised frequently, which takes time and is easily ignored.
4) Could cause issues with equal value. Orientation predisposition can crawl into a skill based pay framework similarly as effectively as it can into some other framework, and there could be genuine difficulties in deciding near worth except if a more customary component examination conspire is utilized to enhance it. For what reason should the course of occupation assessment be made considerably more troublesome along these lines? It's additionally conceivable that nonexclusive job definitions could be biased. relies upon a careful handle of the foggy and habitually bewildering jargon of abilities.
5) It may have language and complications that too easily turn into a "over-designed" framework that is unaccepted by line directors (leaving it the property of individuals division).
6) May cause a focus to be placed excessively on inputs rather than outcomes, knowledge, skills, and behaviour rather than outcome

TEAM REWARDS

Introduction

Employers honour workers who accomplish yearly outcomes. The recurring goals are followed up on to recognise and promote increased output. Each team member has the chance to earn an incentive based on the group's overall performance thanks to team awards. When tasks are closely linked to one another, team rewards are most suitable.

Team camaraderie can be fostered through the use of incentive programmes. Building a high-performance team and encouraging cross-organizational collaboration are both possible with the correct implementation of an award and commendation programme. However, team incentives should not be used haphazardly as a poor implementation could result in toxic rivalry, a lack of teamwork, and eventually dire financial repercussions for the company.

Where businesses depend on teams to complete the job, team incentives are typical. If a squad as a whole accomplishes certain objectives, they may receive unique incentives or presents. Once more, a sharing plan is a form of group incentive that encourages team members to cut expenses and improve labour productivity in their work process. Gain pooling programmes compute cost reductions and distribute bonuses to all team members using a preset algorithm. Usually, the business distributes the cost savings to the staff.

Steps for Team- Based Reward System

The following stages are included in the team-based reward scheme:
1) Teams Evaluation
i) Assess how well the team performed in relation to predetermined goals.
ii) Share the findings in order to promote openness.
2) Rewarding Teams

Basis of Scheme : According to the degree of proficiency they exhibit in performing their duties, people are given money incentives in the form of raises to their basic salary. It is a means of compensating individuals for their capacity to deliver both now and in the future.

Consolidated Pay Increases : Similar to PRP, there is room for combined pay advancement within pay bands linked to levels or levels in a lifelong family or limited reviewed construction, or zones in an expansive grouped structure (skill pay is regularly seen as a trait of such designs).

Pay Progression : The rate and the limits of headway through the compensation categories may be determined by more broad evaluations of competence growth, but they may also be based on competence estimates made with a PRP-type metrix.

Competence- Related Job Evaluation

Competence- based job evaluation can work in any type of business, but it is particularly appropriate in organizations with numbers of knowledge workers where the emphasis is on people in flexible and developing roles rather than on rigid job hierarchies. It can be relevant in project and process- based organizations in which this type of role flexibility is important and where the contribution of people can be significantly under measurably enhanced* if they acquire additional skills and competences and are able to use them to good effect. It can work well in job families.

Approaches Competence- Related Job Evaluation

Competence- based job evaluation concentrates on people in their roles, not jobs . There are three varieties, as explained below :

1)Point- Factor : assessment of jobs based on competence The most typical strategy is this one. It is, broadly, the one adopted by the National Provincial Building Society and currently being developed at Triplex Safety Glass. The headings in the factor plan consist entirely are mainly of core or generic competence is included in your competence framework. This levels at a which the generic competences included in a competence framework. The levels at which the generic competence can be applied in roles are defined and scores are allocated to each level .

The competence- based factors may not be weighted. Individual role competence profiles are defined, and are compared with the generic competence level definitions and scored in exactly the same way as in a conventional point- factor scheme.

A broad banded structure is likely to be adopted, the bands defined in points terms and roles allocated to bands accordingly. Within the bands pay is related to market rates, and progression depends on individual levels of competence and the contribution. There may be no upper limits- progress is governed by the capacity of individuals to develop their competencies, expand their roles by taking on new responsibilities, and it deliver performance to meet or exceed expectations.

2)Role Classification : Competence-Related Job Evaluation : In this approach the grades in a broad-banded structure are defined generally as in a job classification scheme, but the grade definitions are expressed in terms of the organization's com or generic competence. Roles are slotted into bands on the basis of comparisons between individual competence profiles and the band definition.

Progression within and between the bands takes place as described above. Alternatively, a job family structure is adapted in which the levels in the job family are defined in competence terms. Pay progresses within the job family along curves related to individual com- petence and contribution.

3) Individually Based : Competence-Related Job Evaluation : This approach is based on a broad banded or job family structure. The bands may be designated very broadly by reference to generic roles- e.g. process direction, process management, team leaders, and process implementation - but no attempt is made to define them in competence terms.

Progress within and between bands is related to individual competence and contribution, as demonstrated by the capacity to take on additional responsibilities and new roles.

Advantages of Competence- Related Job Evaluation

The benefits of competency-based employment assessment include:

Pay close mind to the performance-related factors that really count.

Motive Theories and Skill-Based Compensation Plans

Many incentive theories are compatible with skill-based compensation structures. They are in line with FRG theory because they support workers' efforts to develop, learn, and extend their skill sets. The chance to develop can be an incentive for workers whose lower-order requirements are already largely met.

Additionally, study on the success need supports paying individuals to increase their talent levels. High performers are driven to perform tasks more effectively and better. High performers will find their tasks more difficult by acquiring new skills or honing the ones they already possess.

Also connected to skill-based compensation is the reward hypothesis. Employees are incentivized by skill-based compensation to become more adaptable, keep learning, switch up their roles, become generalists as opposed to experts, and cooperate with higher-ups in the company. Employers should use skill-based compensation as a reinforcer if they want their staff to exhibit certain behaviours.

Furthermore, fairness issues may be raised by skill-based compensation. Skills may offer a better input measure for compensation determination when workers compare their input-outcome ratios than variables like tenure or schooling. When skill-based compensation is used, it may raise the impression of equality and improve employee incentive to the extent that workers view skills as the most important factor in job success.

Due to their belief that unanticipated issues with trade unions may emerge, management or companies in India are not particularly fond of this. However, management is enticing their most favoured and capable workers to pursue lengthy training or study by giving them paid time off. Once their training or studies are successfully completed, they are watched in the workplace and prepared for more senior roles.

Plans that are founded on skills do not take achievement levels into account, among other things. Only the question of whether or not someone can execute the ability is addressed. The degree of success may be ambiguous for some abilities, such as quality control or team leadership. Although it is feasible to evaluate how well workers execute each of the skills and combine with a skill-based plan, this is not a fundamental component of skill-based compensation.

COMPETENCY RELATED PAY

Meaning of Competency- Related Pay

Hypothetically, skill related remuneration is engaging in light of the fact that it very well may be a part of a complete capability based HRM strategy and it aligns with the notion of human capital management, which places an emphasis on the skills and abilities that employees bring to the workplace. The excessive focus on quantifiable, and frequently irrational, goals in PRP plans is avoided by pay based on ability. It is attractive because it awards people for their abilities rather than for outcomes that they may not have much control over.

By tying pay advancement to evaluations of the skill levels individuals have attained, competency-related compensation is made possible. The evaluation is conducted using a competency profile or structure. A completely successful person in a position is anticipated to possess a certain degree of ability, and the levels actually attained are contrasted with the necessary standards.

According to Brown and Armstrong , "Paying for the turn of events and use of essential abilities, ways of behaving, and activities that help elevated degrees of individual, group, and hierarchical execution is what is meant by 'competency-based pay,'" according to one definition of it.".

Features of competency- Related Pa

Competency-based compensation has some unique characteristics, including:

Based on Agreed Framework : It is preferable to operate within an authorised framework, or a determined system of skills.

Based on Agreed Standards : It is not predicated on the accomplishment of particular outcomes, like goals or finished tasks. However, it is focused on meeting established achievement criteria.

SBP has benefits over other compensation methods, which is why it is used. The benefits sought are correlated with both company success and staff happiness.

Intended advantages include :

a) increased capacity to direct employees towards areas of difficulty and prevent useless time spent waiting for other people to solve issues;
b) flexibility in position covering allowing teams to fill in for members who are only temporarily missing;
c) larger skill foundation leads to quicker response to shifts in technology and product blend;
d) broader view on overall process leads to increased involvement in problem-solving and other collaborative activities;
e) decreased total employment due to the inclusion of specialised tasks (such as upkeep, quality control, and oversight) into team skill requirements;
f) greater dedication to organisational objectives as a result of a wider outlook;
g) increased self-esteem as a result of particular skill growth;
h) increased minimal employment standards due to the need for workers to advance through multiskilled positions;
i) improvements in overall output.

Businesses that use skill-based compensation report improvements in freedom and adaptability as well as improved employee engagement and team performance. An rise in technology use and production per hour go hand in hand with this. In the ACA survey, about two thirds of the companies reported having some progress in lowering total pay expenses.

Successful systems have strong local management backing and frequently start in the local business rather than being imposed by the company. They prioritise the professional advancement of their staff members and uphold their training commitments.

Disadvantages

Additionally, skill-based compensation entails additional criteria that are occasionally seen as drawbacks. They are unintentional as drawbacks, but some of them are inevitable as necessities.
Higher ability levels might request higher market wages, and they without a doubt do in specialists' viewpoints. These can be countered by lower complete unit costs because of diminished work force and additionally higher generally yield;
a) higher individual pay rates; and b) higher market wages;
b) Time and money spent on training for students, teachers, programme design, resources, management, lost output, and mistakes brought on by numerous learning curves;
c) Difficulties with skill evaluations, such as time required for assessments, evaluator expertise and training, insufficient peer feedback, and review speed;
d) The challenge of finding similar positions and pay scales with other companies;
e) The time and administrative effort needed to keep track of training and assessment start and finish times;
f) Organizing shifts within teams to promote cross-training and maintain abilities;
g) To accommodate the time needed for instruction and learning, extra workers must work late;
h) Learning for the purpose of increasing compensation without considering real ability;
I) A lack of motivation to study;
j) Replacing obsolete abilities with new ones after completing the initial learning process and receiving payment;
k) "Topping out" at the greatest amount of salary and receiving no further raises;
L) The wish of employees to participate in the benefits of good organisational success brought on (in part) by improved employee abilities.

Raise the Skill Base : The skill possessed by the employees should be raised by the organization through effective working atmosphere. Organizations using (JIT) just-in-time technique and customer handling have different teams for such activities and these organizations require to enhance the skills of their employees. Employees are expected to have multiple talents and are able to change their skills with other team members.

Flexibility : Skill- based pay provides flexibility in the organization's work Force. Workers are more flexible regarding working conditions . They can be transferred from one place to another , i.e., skilled workforce means to act as company wants. The company can increase or decrease the production as per the customers demand and so is the change in working of the employees. By having the skill- based workforce the organization can go through smooth working whether it is technical work or non technical work. These types of activities can be performed by the same team members.

Operating with a Leaner Workforce : In the earlier surveys, researchers found that companies with their leaner workforce provide better outputs than with the traditional workforce. The employees acting as a leaner workforce is more efficient and performance driven.

Types of SBP Plans

There are five different SBP programs, which can be divided into groups based on the kinds of abilities that are measured and recognised.

- Vertical skill plans track the development of input/output skills within a particular position, such as a drill press technician learning preventive maintenance and in-process examination.
- Horizontal skill plans encourage the development of complimentary skills across a variety of occupations, such as learning how to handle both accounts payments and accounts debts.
- Depth skill programmes encourage specialised skill use. (e.g., computer programmer specializing in database programming).
- Employees who master the fundamental skills are rewarded by basic talent frameworks. (four function math; reading, writing and speaking English). This kind of strategy is ideal for businesses with a sizable population of workers who speak English as a second language.
- Combination designs honour any of the previously mentioned abilities. According to our expertise, this kind of SBP plan is the most popular.

Designing Skill- Based Pay /How Skill- Based Pay Works

Following are the most important steps in administering skill- based pay :

Determination of- Skills needed by Organization : First, the organisation needs to assess the gap between the goals it needs to reach and its resources to do so. The second step is to ascertain the organisation's present skills. The necessary capacities can be deconstructed from that gap analysis and turned into individual behaviors, knowledge, and skills.

Creating Skill Blocks : Based on the aforementioned abilities, a skill block is a group of abilities gained to carry out a range of tasks, obligations, and/or duties and that serves as an organizationally valuable bundle upon which to base compensation choices.

Praising and Progression through Skill Blocks : In a skill-based compensation system, rather than a specific position, the beginning point for remuneration is based on the variety and breadth of a person's abilities. Employees are paid according to the connected talent block if they have proven their proficiency in it.

Skill Certification : The method of assessing an employee's skill development and degree is called skill accreditation. In general, groups, management, team members, leaders, bosses, and managers can all contribute to the accreditation process. Several methods, including work examples, written exams, boss observations, team assessments, and individual assessments are used to conduct the assessment.

Advantages

Shodhasamhita : Journal of Fundamental & Comparative Research
Vol. IX, Issue I, Book No.5, January – June: 2023
ISSN: 2277-7067

SUCCESS OF SKILL BASED PAY PLANS

Dr. Y Jayaprada, Research Scholar, DR. A P J ABDUL KALAM UNIVERSITY, INDORE
Assoc. Prof. at Avanthi Institute of Engineering & Technology, Hyderabad
Dr. Sushil Beliya, Prof. DR. A P J ABDUL KALAM UNIVERSITY, INDORE

Abstract
Factors related to the success and survival of skill-based pay (SBP) plans are addressed in a longitudinal study of 97 facilities. Results indicate that certain design features and support variables relate to increased workforce flexibility and to SBP survival, and supervisor support also relates strongly to SBP survival. The results also show that SBP plans are more successful and sustainable in manufacturing facilities than in service facilities, and SBP survival is less likely in facilities pursuing a technical innovation strategy. Implications of the research for theory and practice regarding SBP plans, compensation systems, and human resources management innovations are addressed.
Keywords: skill-based pay; survival; innovation; job design.

Introduction

Similar to snowflakes, skill-based pay (SBP) schemes have some similarities but also differ from one another in important ways. We'll look at the underlying principles of skill-based compensation and many of the accessible choices.

It is not possible to design skill-based compensation by emulating another system's structure. Each business has its own distinctive work practices, employees, and goods. What is successful in one company might or might not be successful in another. Although there is much to be learned from researching what has worked and what hasn't for other businesses, a solid grasp of the various factors and SBP concepts is crucial to the creation of an SBP strategy.

Reasons Given for Installing a Skill- Based Pay Plan

A skill-based compensation plan has been implemented for a variety of causes:

Employee Flexibility : Most people would agree that this benefit of skill-based compensation is the most significant. The utilisation of the workforce is improved as a result. In organisations that are evolving quickly, there is definitely benefit in having workers who can perform a range of duties.

"Leaner" Organization : The organisation can function with fewer workers because each can be used more effectively when they are able to perform more duties.

Improved Competency : As we shall see, skill-based compensation necessitates ongoing, intensive training.

Support for New Organizational Forms : The ability of team members to put themselves in others' positions and comprehend more of the overall process is beneficial as organisations transition to working in teams.

New Technology : The technology used within organisations is evolving, in addition to hierarchical designs. With the presentation of new innovation, workers must alter both what they do and how they carry it out. In this situation, paying to acquire new abilities makes sense.

Employee Desires : Employees prefer to be compensated for their abilities and ability, which are fundamental to who they are. They invest more into this than just receiving compensation for the job's worth to their employer.

Employee Involvement : The result is a greater level of employee participation in the team's job as a result of working in teams, enhancing one's skill, and receiving compensation for doing so.

Objectives of Skill- Based Pay

There are various aims of skill based pay as described under: